

Wednesday, Thursday and Friday—February 14, 15, 16, 1962

1962 INTERNATIONAL

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**DIGEST of  
TECHNICAL PAPERS**

Irvine Auditorium and University Museum, University of Pennsylvania

Sheraton Hotel, Philadelphia, Pa.

**SOLID-STATE CIRCUITS CONFERENCE**



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# 1962 INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE DIGEST of TECHNICAL PAPERS

*First Edition*

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1962 International Solid-State Circuits Conference

DIGEST OF TECHNICAL PAPERS

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**Volume V**

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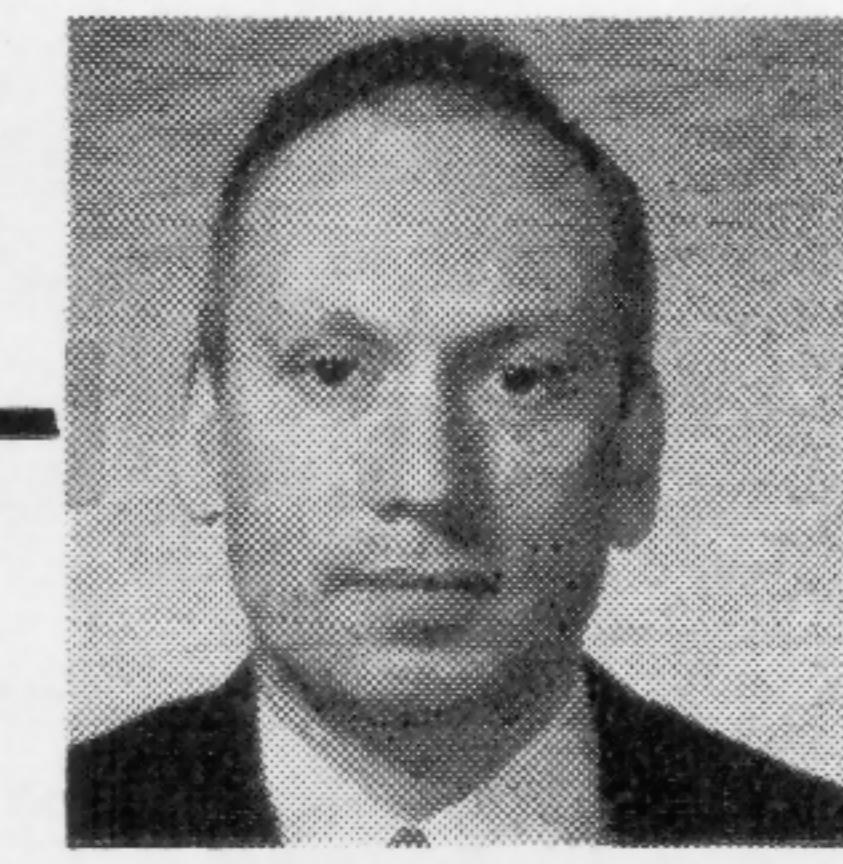
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# Foreword



## ***Cap and Bells or Shovel Hat***

THE MANY FACETS of technical conventions indicate that they provide opportunities for education, social gatherings, technical discussion, commercial exhibits, awards to colleagues for professional accomplishments and recruiting. Whether or not all or even more of these activities meet legitimate professional needs could be the subject of considerable discussion; it is proper here to consider only the two objectives which the Committees of the 1962 International Solid-State Circuits Conference have tried to emphasize, viz. education and discussion. (To preserve the honesty of the Committees, it should be added that they are all in favor of social gatherings, particularly between sessions!)

Education is the primary goal of the day sessions. The Program Committee has tried to hold the number of papers to a minimum to maintain high degrees of excellence (the acceptance rate is typically one per four submitted) and, by thus doing, has simultaneously held the number of parallel sessions required to a minimum. Since education is intended not only for *beginners*, or for those with only a casual interest in the technical subjects presented, but also for experts in the field, it is hoped that all who attend will be stimulated by some of what they hear and that some who attend will find all of the papers interesting and informative. Should this be realized, then part of the Conference will have achieved success.

However, education at the forefronts of knowledge seldom comes easily. If it did, *breakthroughs* (or more properly, *oozethroughs*) would not be so expensive. There is a certain amount of labor, disagreeable introspection, wrong starts and restless nights which seem to be the price of technical progress at the contributor's level. Technical conferences can materially ease the paths to progress and greater understanding by providing forums for discussion on technical topics which are still the subjects of differing opinions or uncertain interpretations. The 1962 Conference offers eleven evening sessions providing an opportunity for such discussions.

In times of considerable commercial competition, such as the present, when superlatives are commonplace and the commonplace is often bathed in superlatives, it is more essential than ever to preserve the integrity of the scientific and engineering communities by forthright and open discussion of *controversial* subjects. Such discussion generally implies the existence of *critics* and *creators*, of antagonists and protagonists. It is undoubtedly difficult for the authors of creative ideas to accept criticism without some adverse reaction, but while *under fire* in technical discussion sessions they should remember that the final arbiters are experiment and time; if they are right, both nature and progress are on their side, and the truth will prevail sooner or later.

The role of the constructive critic is equally as difficult. He is seldom as well prepared at the moment as the author who invokes his comments, and if he overstates his case the sympathy of the audience will probably be with the *underdog*. But his role is essential in all scientific progress and unless he is heard, the profession as a whole will suffer from hoaxes or honest errors which may be perpetuated at considerable expense and loss of time. Both author and would-be critic should remember the advice of *Thackeray*: "Yet, look you, one is bound to speak the truth as far as one knows it, whether one mounts a cap and bells or a shovel hat; and a deal of disagreeable matter must come out in the course of such an undertaking."

The members of the various groups responsible for the preparation of this Conference hope that those authors who have been selected for technical presentations do, in fact, represent work which is at the forefront of the solid state field. It is also hoped that a large number in the audience will participate actively in the evening discussion sessions. To this end, we wish all attendees a most enjoyable time at the social gatherings, a most instructive and thought-provoking time during the formal technical presentation and a not-altogether agreeable experience at the discussion sessions.

***J. J. Suran***  
***Conference Chairman***

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## SESSION I: Logic

Chairman: A. W. Lo

IBM Corporation, Poughkeepsie, N. Y.

## WM 1.1: Nonlinear Devices for Threshold Logic

E. P. Stabler

Electronics Laboratory, General Electric Company  
Syracuse, N. Y.

IN RECENT YEARS threshold logic synthesis procedures have received much attention. These synthesis procedures assume the existence of an idealized threshold device which responds to weighted, additive input signals. Many examples are available of efficient realization of specified logical functions with threshold logic gates.

A relationship can be found between the degree of nonlinearity of a threshold device and the logical functions which the device can generate. The ambiguity of the excitation level in an input channel is a function of the complexity of the logical gate from which the input is derived. This ambiguity must not be allowed to propagate or to increase through the several levels of logic. This restriction establishes a maximum functional complexity as a function of the nonlinearity of the threshold device.

The analysis makes use of a three-segment approximation for the nonlinear characteristic, as shown in Figure 1. It is assumed that the threshold device is the only nonlinear element in a logic gate. One segment describes the element below threshold, one segment describes threshold region, and the third segment characterizes the behavior above the threshold. The results obtained for this model can be used to measure the approximate logical capability of a wide variety of threshold devices. Two-terminal, negative resistance devices such as tunnel diodes, and transistor flip-flop elements and magnetic cores can all be brought within the scope of the analysis without major modification. The relationships, which are derived for this model, provide a guide to the logical designer regarding the approximate practical limits on the functional complexity, which can be obtained with a single threshold element.

In Figure 2 the nonlinear element is combined with a summing network and an amplifier-isolator to form the basic logic building block. The signals provided at the input are digital in nature having nominal values  $a, b$ . The actual input excitation level will often be different from the nominal value. A tolerance range must be established about the two nominal levels. Signal inputs in the range  $a$  to  $(1 + \delta)a$  are interpreted as binary 1, while inputs

in the range  $(1 - \Delta)b$  to  $b$  are interpreted as binary 0. The configuration of Figure 2 can be analyzed for a variety of threshold functions. The essential restriction imposed is that the signal amplitude ranges of the output signal must be compatible with the tolerance ranges imposed on the input signals. When this condition is satisfied the signals remain within the specified tolerance range for all possible logical operations.

The results of this type of analysis are given in Figure 3. The permissible number of input variables (fan-in) is  $n$ . The range of the excitation amplitude is a limitation in many technologies so this range is indicated.  $P_T$  is the minimum allowable change in input excitation to the threshold element. It must be sufficient to switch the threshold element through the entire threshold region.  $R_T, R_N$ , and  $R_S$  are the inverse slopes of the three segments.

It is notable that the fan-in is determined entirely by the nonlinear element independent of the linear components of the logic building block. Since a fan-in of two is a minimum for data reductions, it is possible to determine a minimum degree of nonlinearity. If the threshold element does not have a nonlinearity as great as the minimum, some of the elements must be operated with a fan-in of unity to stabilize the signal levels.

In Figure 4 a tunnel diode  $v-i$  characteristic is shown. The slope in the transition region is determined by the tolerance on the threshold current. Assuming a  $\pm 5\%$  tolerance on the threshold level, a 10-ma nominal peak current germanium unit would be limited to a fan-in of six.

The complexity of the logic function, which can be generated by a given nonlinear element, is limited by the degree of nonlinearity of the element, by the accuracy with which the excitation-response relationship is known, and by the range of the excitation which can be tolerated by the element. The relationships given in Figure 3 indicate that the demands made on the threshold element increase very rapidly as the number of input variables is increased.

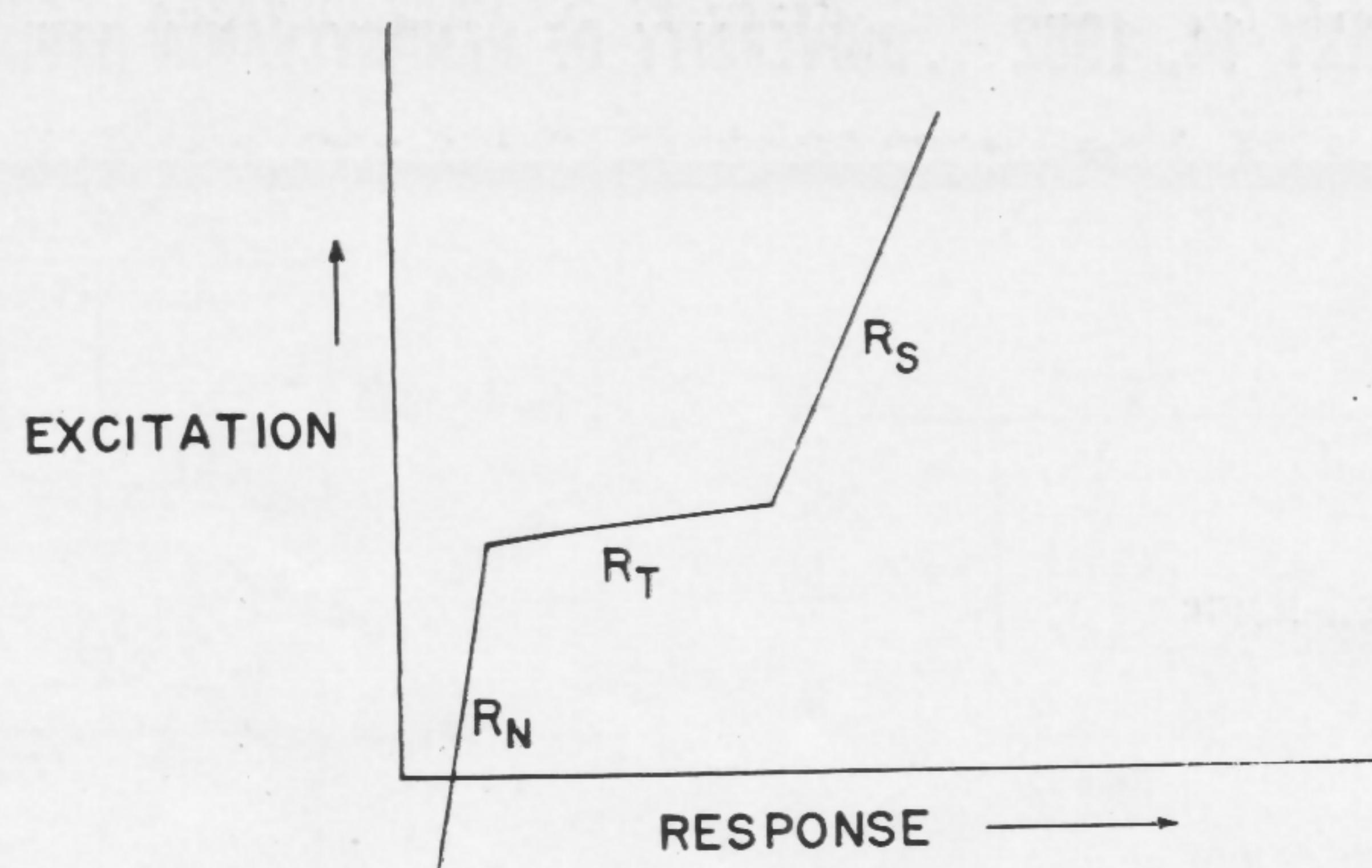


Figure 1—Nonlinear characteristic.

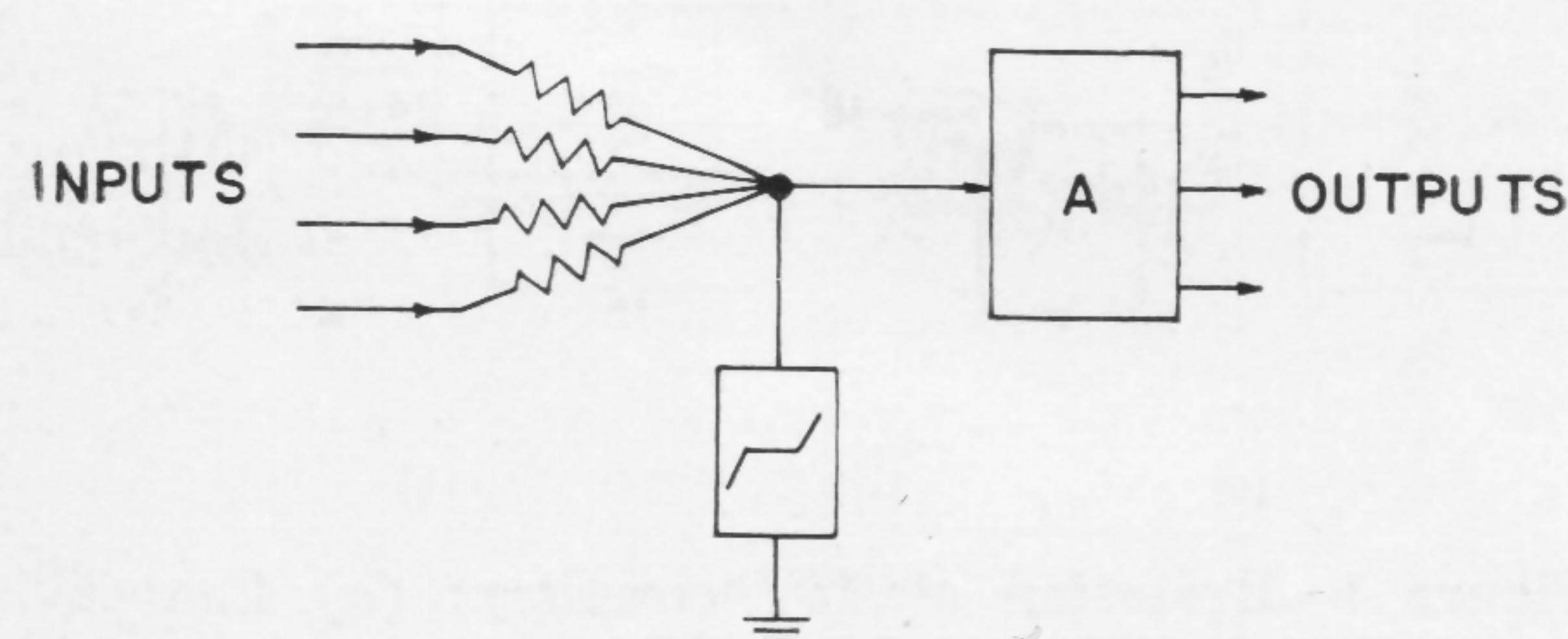


Figure 2—Logic gate model.

$n$  = NUMBER OF INPUT VARIABLES  
 $P_T$  = MINIMUM PERMISSIBLE CHANGE IN EXCITATION  
 $(2^{n-2} + 1) \left( \frac{R_N}{R_T} + \frac{R_S}{R_T} \right) < 1$  (1)  
 RANGE OF EXCITATION  $\cong (2^{n-1} + 1) P_T$  (2)  
 FOR THE SPECIAL CASE IN WHICH ALL THE INPUT  
 VARIABLES ARE EQUALLY WEIGHTED  
 $n \left( \frac{R_N}{R_T} + \frac{R_S}{R_T} \right) < 1$  (3)  
 RANGE OF EXCITATION  $\cong (2n - 1) P_T$

Figure 3—Basic relationships.

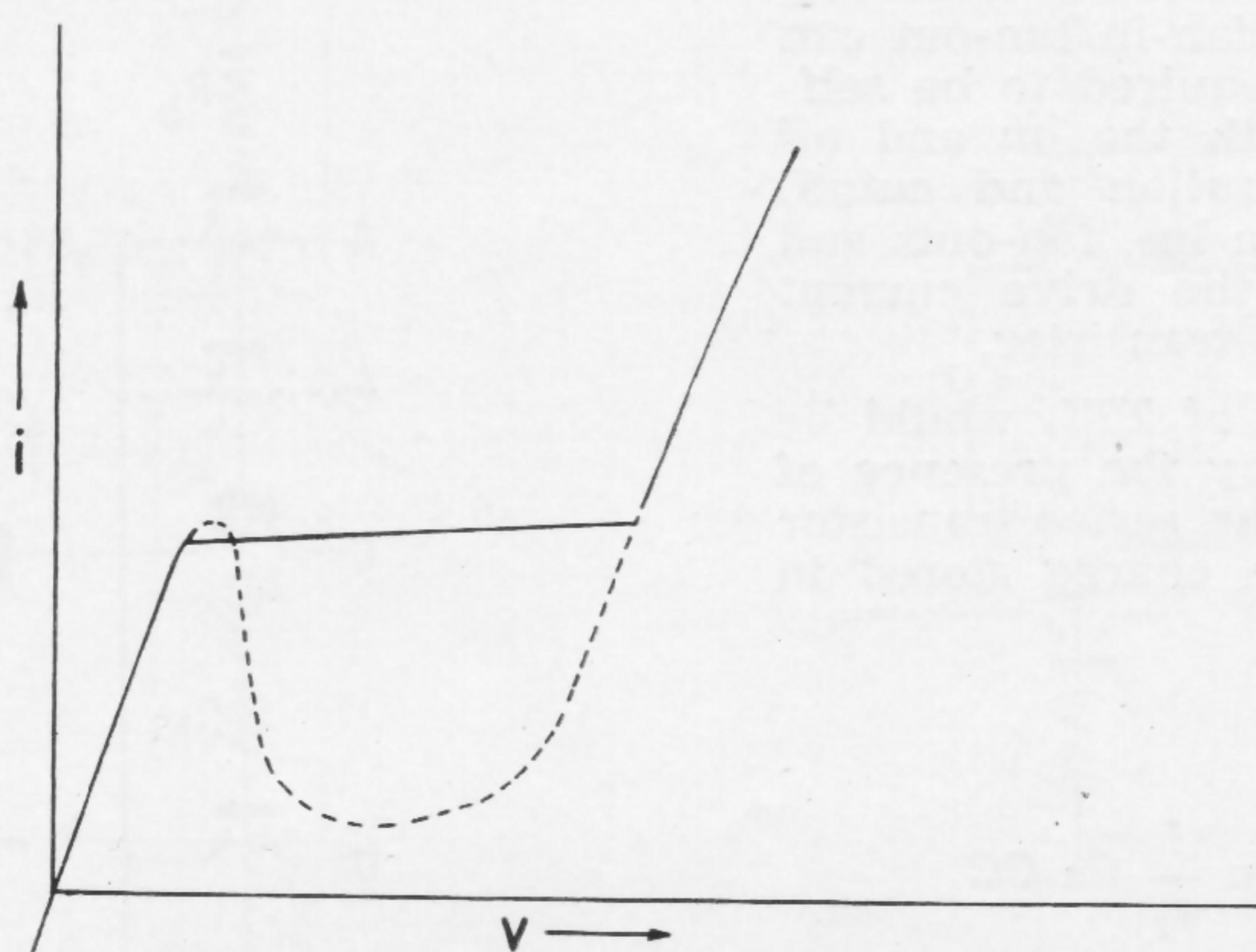


Figure 4—Tunnel-diode characteristic.

## SESSION I: Logic

### WM 1.2: New Forms of All-Transistor Logic

R. H. Beeson and H. W. Ruegg

Fairchild Semiconductor, A Division of Fairchild Camera and Instrument Corporation  
Palo Alto, Calif.

THE NEED for a logic technique having good design flexibility, including system simplicity requiring but one power supply, and operable over a very wide current range, has served to develop new forms of *all-transistor* logic offering a direct tradeoff of power and speed with only one element varying.

From a familiar form of low-level diode-transistor logic (DTL), well known for its fan-in/fan-out and high speed, a new logic circuit, dubbed *transistor-transistor logic* (TTL or  $T^2L$ ), has been derived. As illustrated in Figure 1a, the diode  $D_4$  causes a voltage drop, compensating for the drop across anyone of the diodes  $D_1$  through  $D_3$ , thus assuring that the transistor will be off, when one of the preceding transistors is on. Compensation can only be achieved if a fair amount of current is drawn through  $D_4$  which, under *worst-case* conditions, significantly limits fan-out. A current generator, as shown in Figure 1b, would achieve this compensation ideally without loss of drive current and at the same time eliminate the need for a second supply.

The possibility of replacing the double-diode and generator combination by a series transistor immediately suggests itself, as well as two possible ways of connection; a contiguous collector (CC) and a contiguous emitter (CE) configuration. Since the series transistors can either have their bases in common or be provided with different base resistors, four basic TTL circuits are possible. Six *all-transistor* configurations are possible if *DCTL*-type parallel and series gates are also allowed; Figure 2.

The circuits are not perfectly ideal, however, in that some leakage can occur to reduce fan-out below what might be expected in the *ideal DTL* case; Figure 3. Fortunately, it has been found that *worst-case* leakage currents can be controlled. For most configurations this requires the inverse current gain of the series transistors,  $\beta_I$ , to be low.

By utilizing a generalized *worst-case* circuit, consisting of a chain of two stages, a measure of fan-in/fan-out can be obtained; Figure 4<sup>1</sup>. The chain is required to be self-stable over the temperature range with the *on* and *off* transistors at specified levels of saturation and cutoff, respectively. In general, the various fan-ins, fan-outs and leakage currents combine to reduce the drive current and increase the load current of the *on* transistor.

It might be expected that the speed of TTL would be greatly reduced below that of DCTL by the presence of the series transistors. However, since the series transistor is highly saturated in both states, the charge stored in

the base is required to rearrange itself only slightly. Moreover, since only the emitter diode is required to

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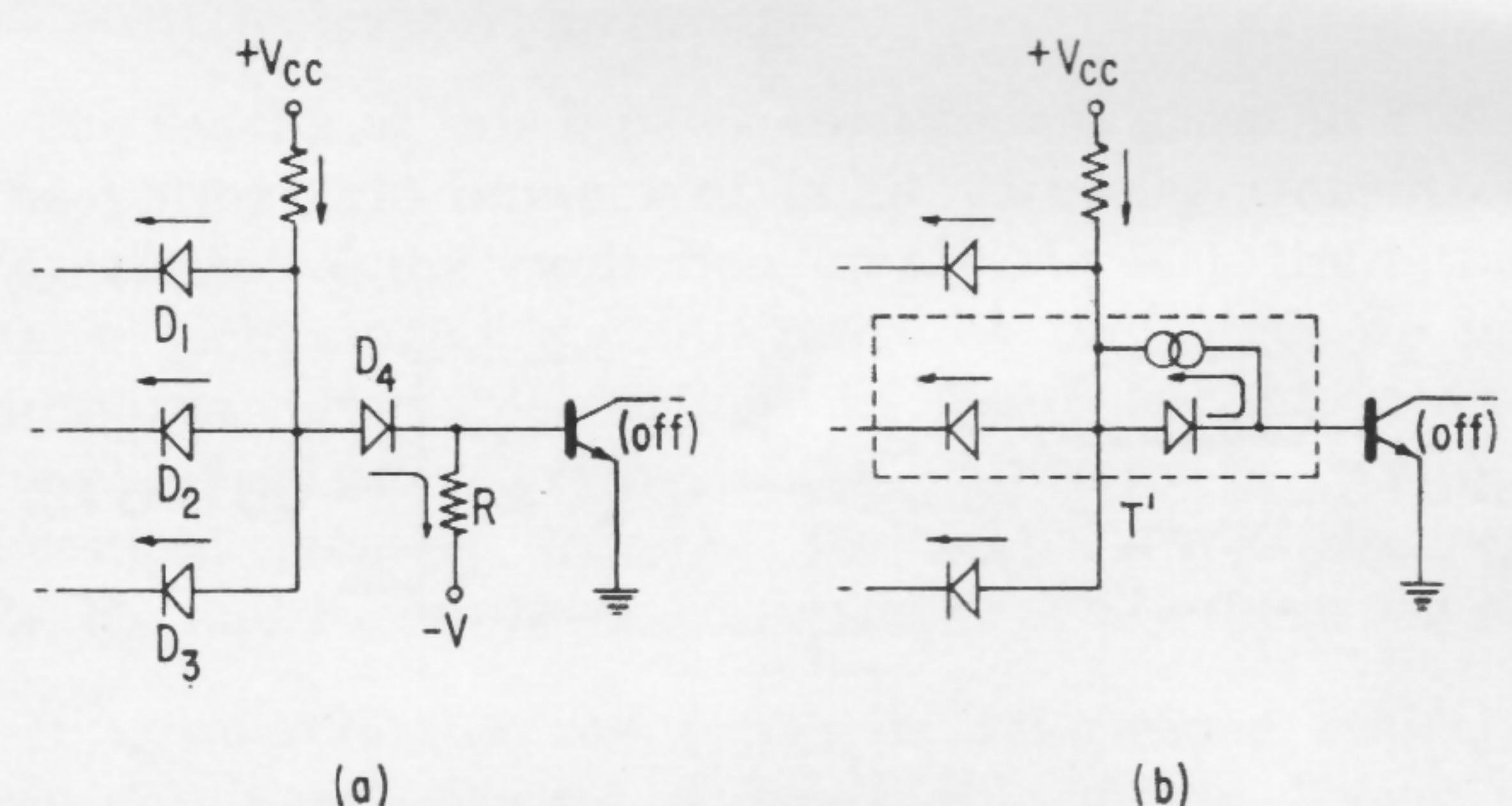
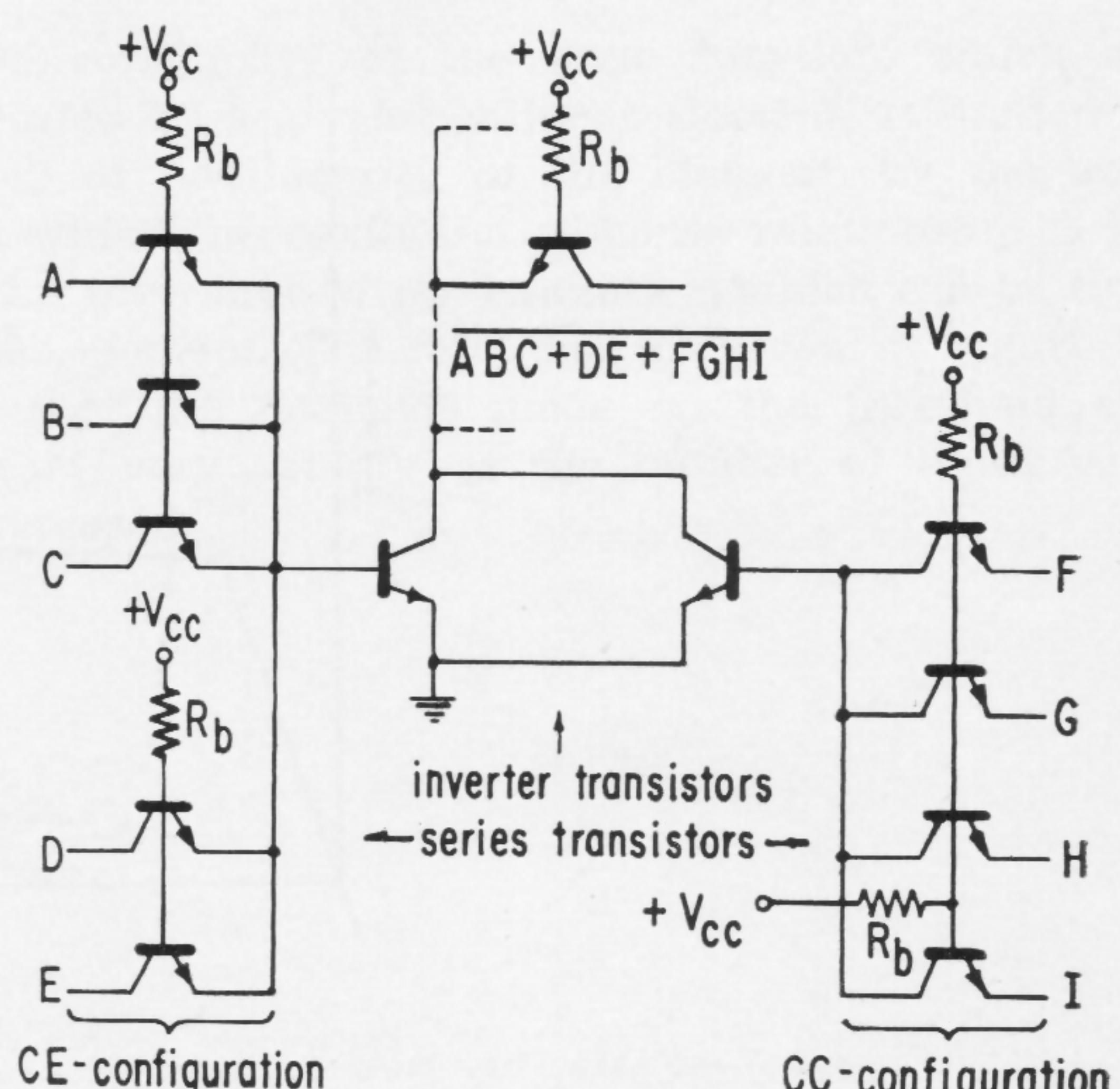


Figure 1—Evolution of TTL-circuitry: (a) Conventional DTL-NAND. (b) Ideal DTL configuration with a current generator to reroute the available current.

(Below)

Figure 2—Example (for illustrative purposes only) of all-transistor logic circuitry, showing the four possible TTL configurations along with the DCTL type NOR. CE series blocks connected to different resistors mechanize the NOR function, the other circuits give the NAND.



<sup>1</sup>  $V_{offset}$  of Figure 4 is defined as:

$$V_{offset} = \begin{cases} V_{CE} \mid I_c = 0 \approx \frac{kT}{q} \ln \frac{1}{\alpha_I} & \text{for CC} \\ V_{CE} \mid I_E = 0 \approx -\frac{kT}{q} \ln \frac{1}{\alpha_N} & \text{for CE} \end{cases}$$

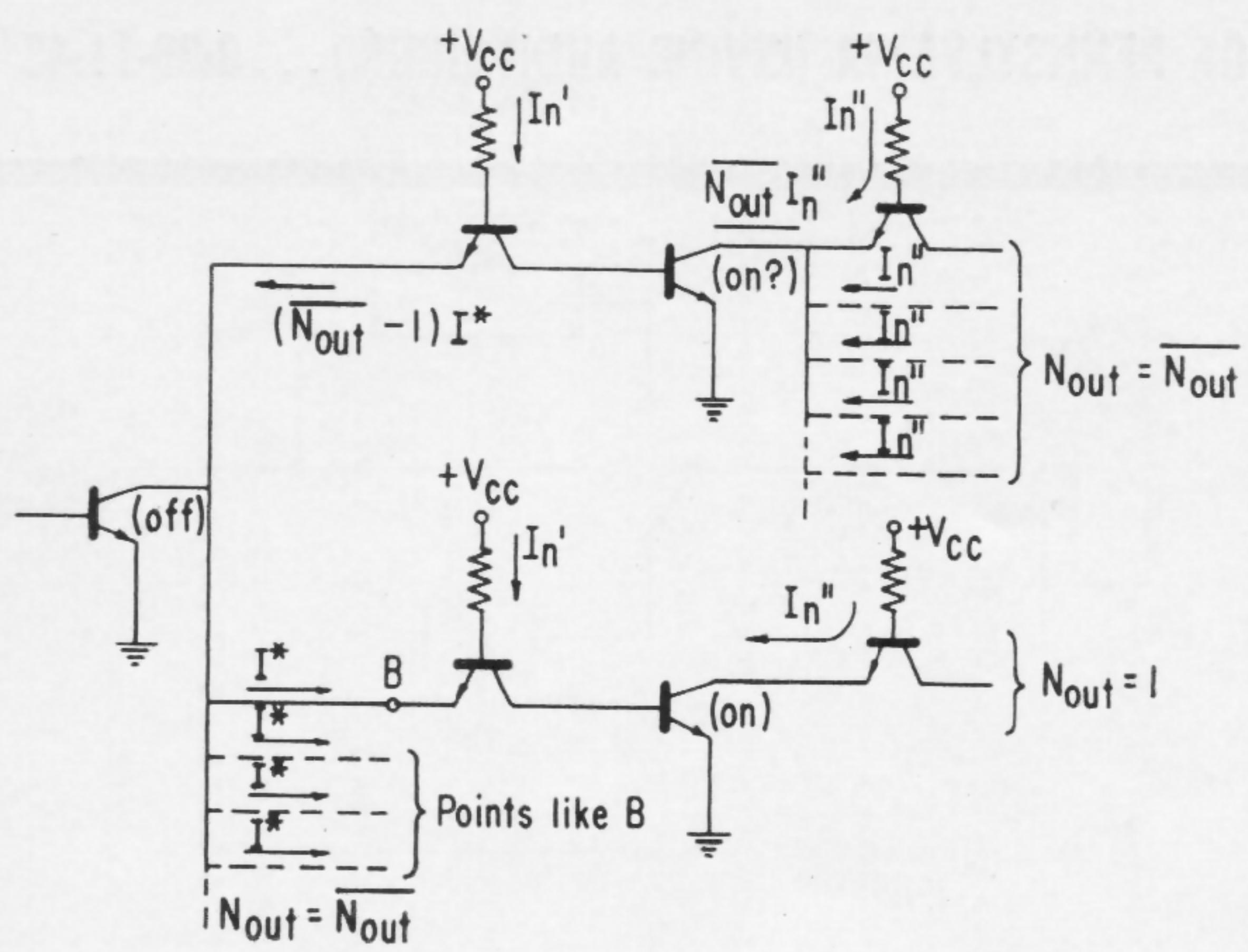


Figure 3—An example of a leakage path in a TTL-CC circuit. Due to unbalance, leakage current  $I^*$  can flow. However, since it must flow inversely through one transistor, it cannot exceed  $\beta_I I_n'$ . Low  $\beta_I$  is therefore desirable.

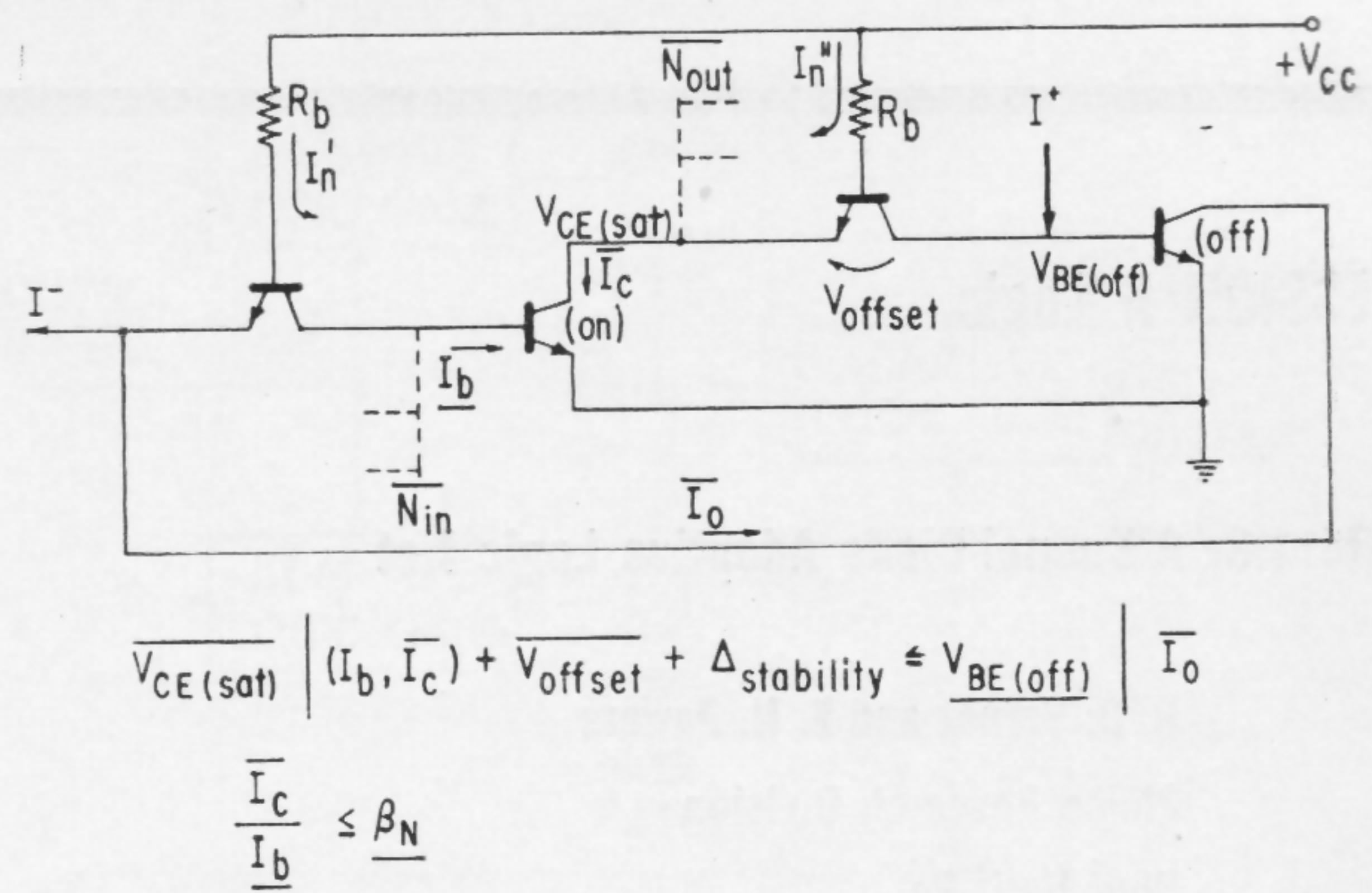


Figure 4—Generalized TTL circuit and *worst-worst* case stability condition. Leakage currents,  $I^-$ , reducing drive current, can be drained away through the fan-in transistors and a current  $I^+$ , increasing load current, can add to  $I''$  of the fan-out transistors.

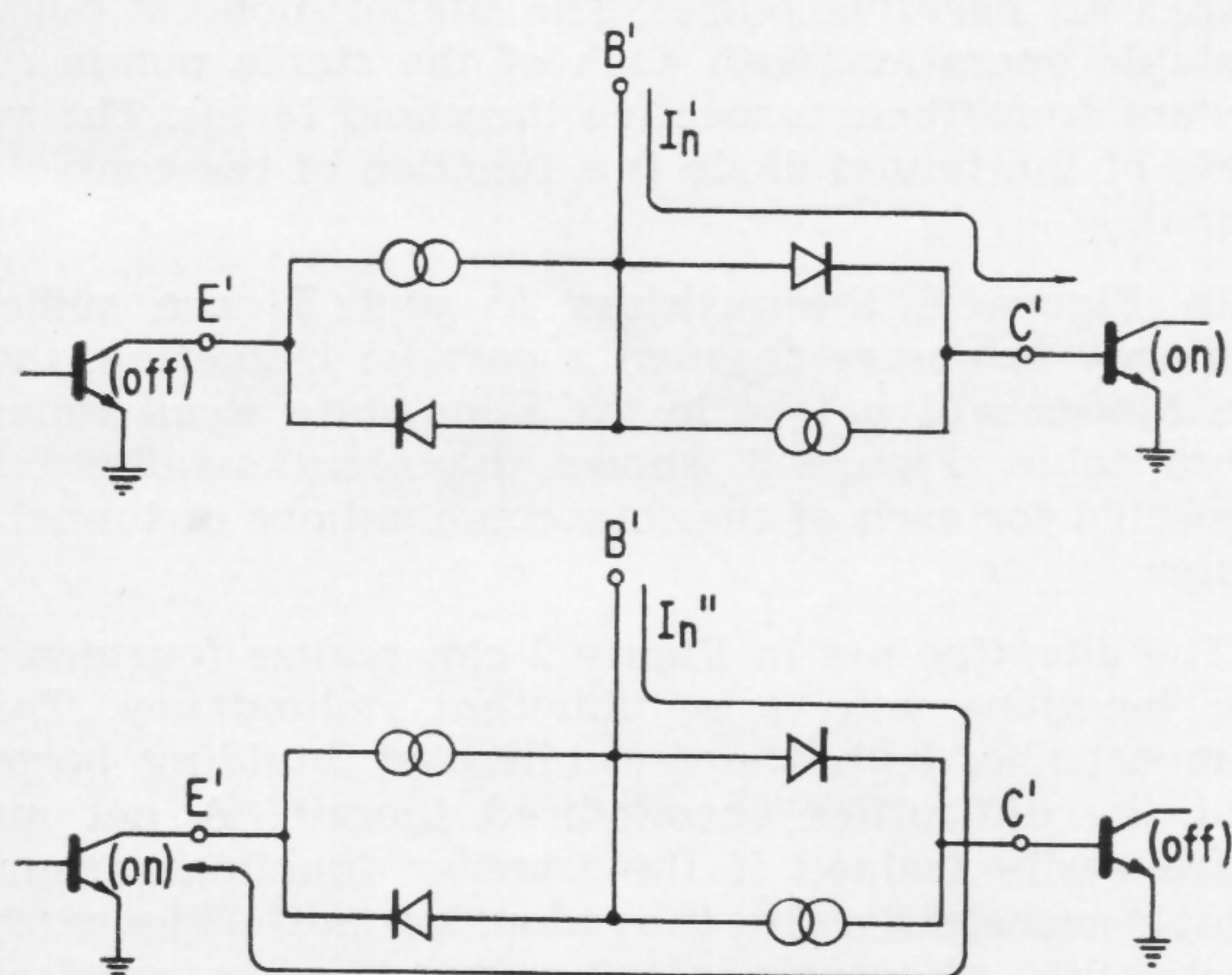


Figure 5—Main current paths in an Ebers and Moll-type equivalent circuit of the series transistor for both states of operation (assuming  $\beta_I \ll \beta_N$ ). Only the emitter diode is required to switch.

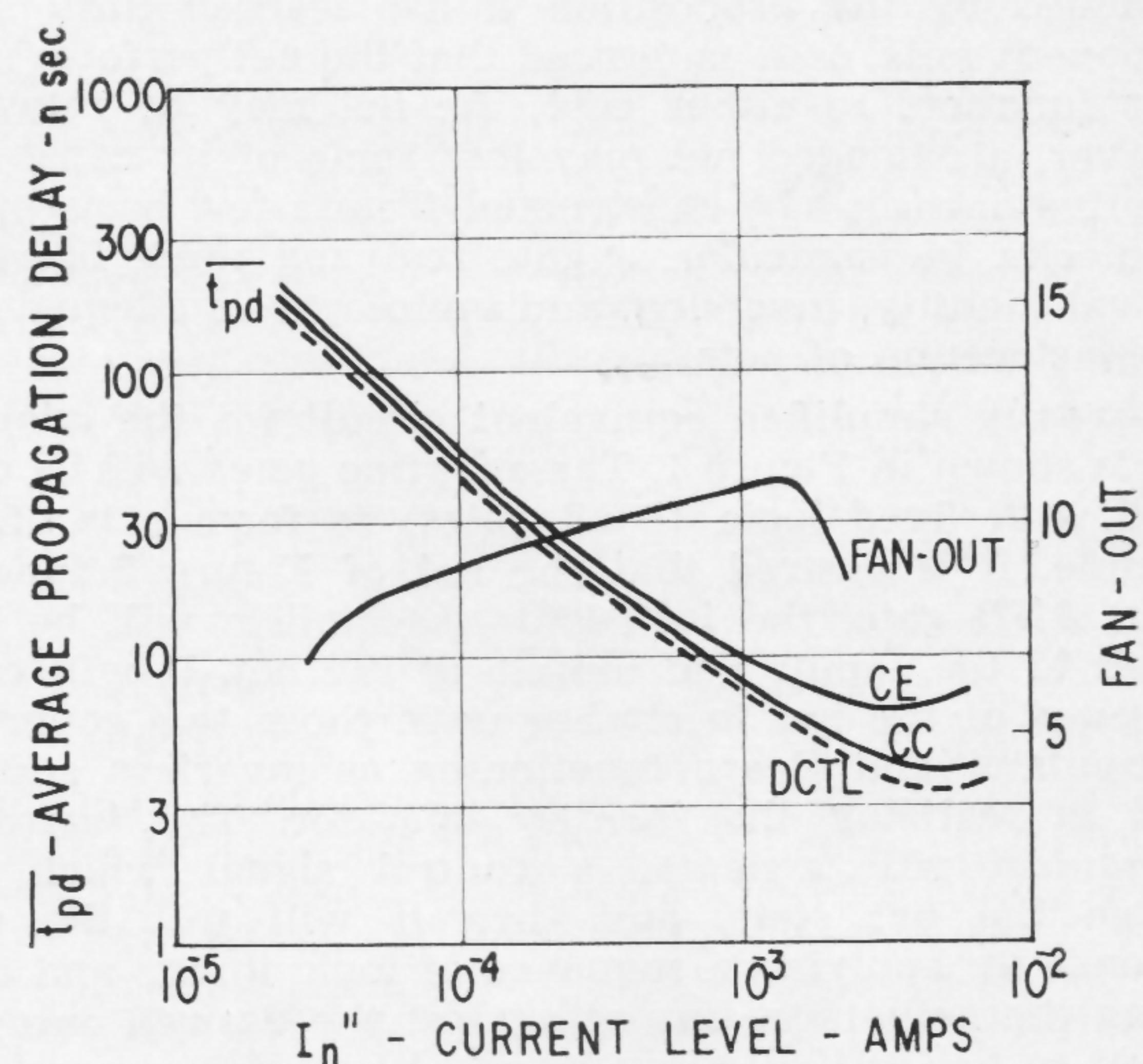
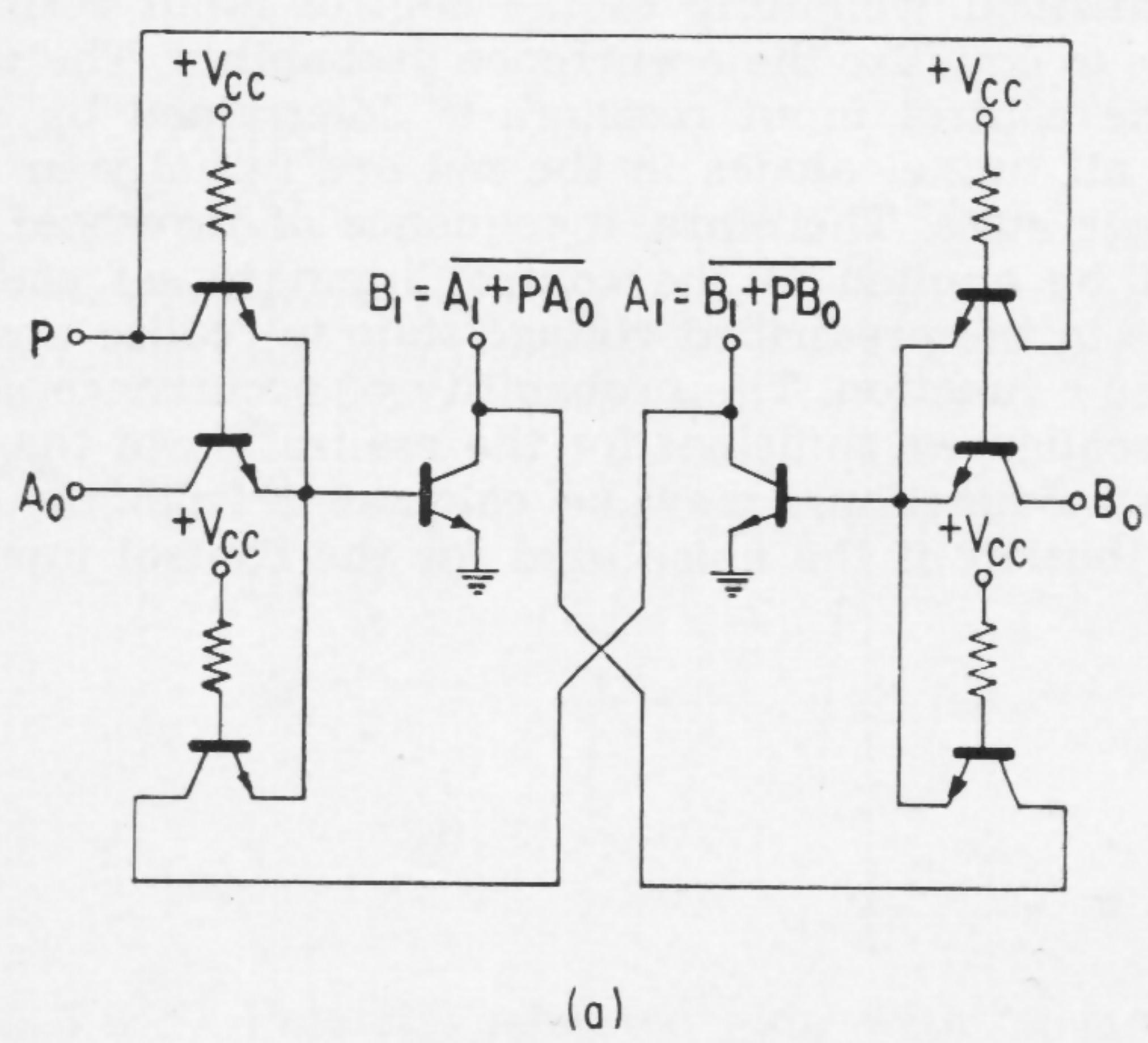
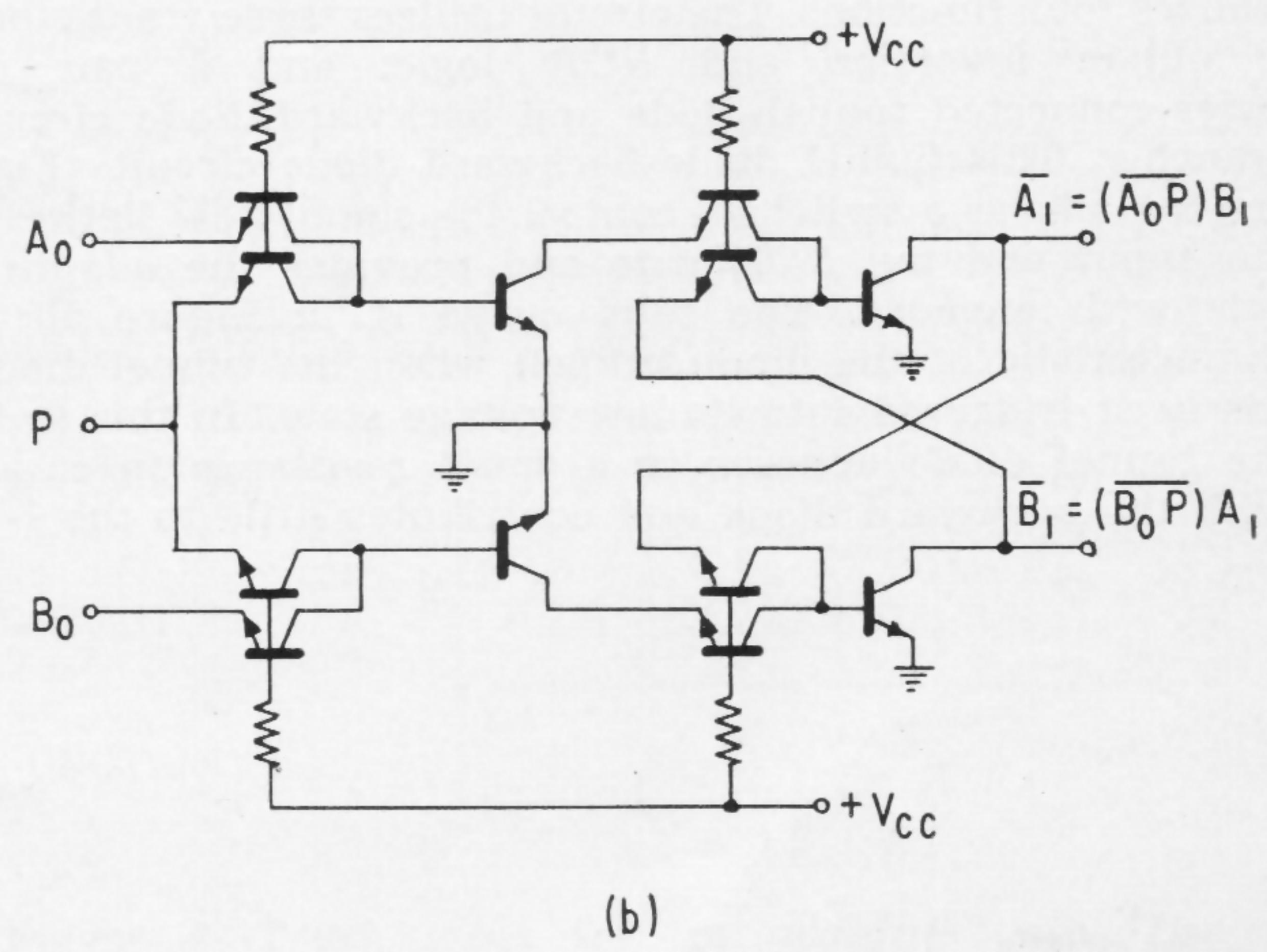


Figure 6—Propagation delays and *worst-circuit case* fan-out for the CC-NAND. Transistors: 2N709. Fan-in = 3;  $V_{cc} = 3$  v;  $T = 25^\circ C$ .



(a)



(b)

Figure 7—Gated flip-flops: (a) Using TTL-NOR and NAND and (b) using the TTL-NAND only.

## SESSION I: Logic

## WM 1.3: A Tunnel-Diode Adaptive Logic Net

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ADAPTIVE LOGIC NETS can be trained to realize any of the functions performed by conventional logic nets. These digital nets may be connected to an *instructor mechanism* and trained; the trained net will respond to stimuli as demanded by the proposition it has learned until some component fails, or it is desired that the net perform some other function. In either case, the net may be retaught; however, a damaged net may lose some of its capability. Adaptive nets may be constructed from a few basic building blocks. In particular, a gate realizing three functions (logical identity, inversion, and tautology) is adequate for the construction of nets.

A grossly simplified equivalent circuit for the *adaptive gate* is shown in Figure 1. The *adaptive gates* will be combined with fixed logic (*NOR* gates) to form nets. If, for example, it is desired that the net of Figure 2 function as an *AND* gate, the *instructor mechanism* will be connected to the inputs and output of the net. It will cause the gates of the net to change until those two connected to inputs *A* and *B* are functioning as inverters and the third is realizing the identity operator. The *instructor mechanism* will generate a control signal which will change the net state, and then it will test the net's response by applying a sequence of logic inputs and comparing the actual net output against the desired one.

*Adaptive nets* may be made as large as desired; a lattice-like structure provides a readily extendable net. As shown in Figure 3, a lattice net may have several outputs. Training will establish paths through the net. The logic inputs will control these paths. The *tunnel-diode adaptive gate* provides a basic building block; however, in larger nets it is essential to add controls which will ensure convergence of the training process.

The *tunnel-diode adaptive logic gate* shown in Figure 4 realizes four functions. The circuit utilizes three transistors to obtain inversion and *NOR* logic, and a pair of series-connected tunnel-diode and backward-diode circuit branches. This tunnel diode-backward diode circuit (Figure 5a) acts as a switch to control the signal flow between the input and the *NOR* gate and provides the *adaptive gate* with memory. The solid curve *A* in Figure 5b is characteristic of the diode branch when the tunnel diode has been triggered into its low voltage state. In this state the tunnel diode appears as a small resistance in series with the backward diode and contributes little to the *I-V*

characteristic of the branch. Negative pulses applied at the signal input are attenuated under this condition. When the tunnel diode is triggered into its high voltage state it appears as a  $.5-v$  supply in series with the backward diode and, as shown by the broken line in Figure 5b shifts the *I-V* characteristic to the left. The branch now attenuates positive pulses applied at the signal input and passes all negative pulses. The tunnel diode is biased for bistable operation with each of the stable points equally distant from their respective threshold levels. The voltage state of the tunnel diode is a function of the control input signal.

In Figure 4, the resistors  $R_1$  and  $R_2$  are sufficiently different to ensure that, with parallel triggering, the tunnel diodes will not be in the same state at all times. The truth table, Figure 6, shows the functions that can be expected for each of the four combinations of tunnel diode states.

The *adaptive net* in Figure 2 can realize fourteen transfer functions with some inherent redundancy. This net demonstrates both the feasibility of building large nets and the difficulties encountered therein. A net may be more easily trained if the transfer functions occur with equal probability. In the *adaptive net* (Figure 2) the probability of occurrence of any particular transfer function is related to the redundancy and the relative magnitude of the weighted resistors at the control input. The redundancy may be reduced at the cost of losing some of the homogeneous structure by eliminating the tautologous functions of the output *tunnel-diode adaptive gate*. This may be accomplished by replacing one of the tunnel diodes with an inverter which is driven by the remaining tunnel diode.

Statistical weighting of the control input resistors also tends to equalize the occurrence probability. The weighting of the control input resistors is determined by assuming that all tunnel diodes in the net are initially in the low-voltage state. Therefore, a sequence of threshold voltages must be applied at the control input to set each tunnel diode in the prescribed voltage state to realize a particular transfer function. The probability of occurrence of each of the sequences, sufficient for the realization of the fourteen transfer functions, may be calculated from the *gaussian* distribution of the noise used for the control input signal.

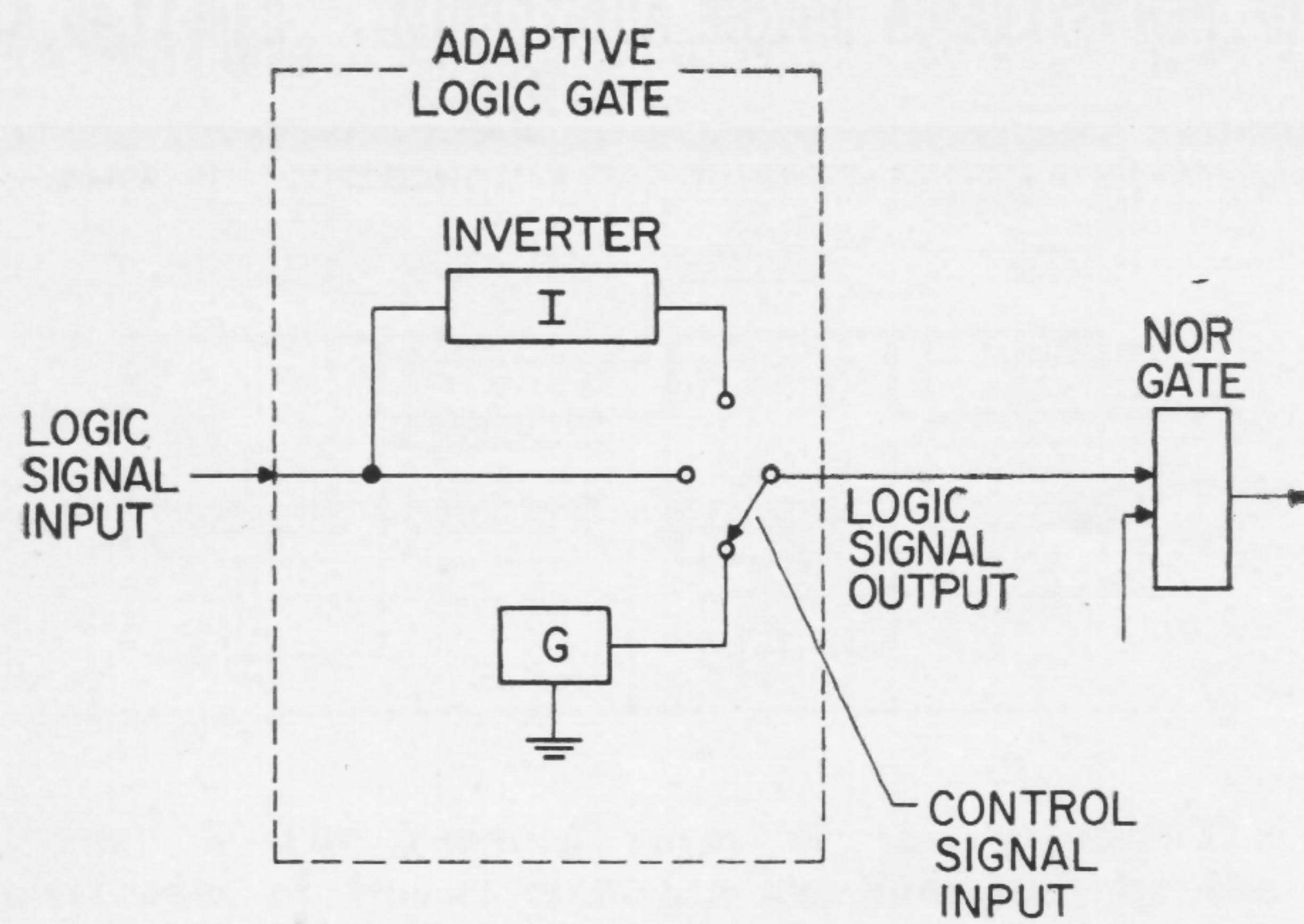


Figure 1—An equivalent circuit for an *adaptive logic gate*. The *adaptive gates* will be combined by using fixed logic in the form of *NOR* gates.

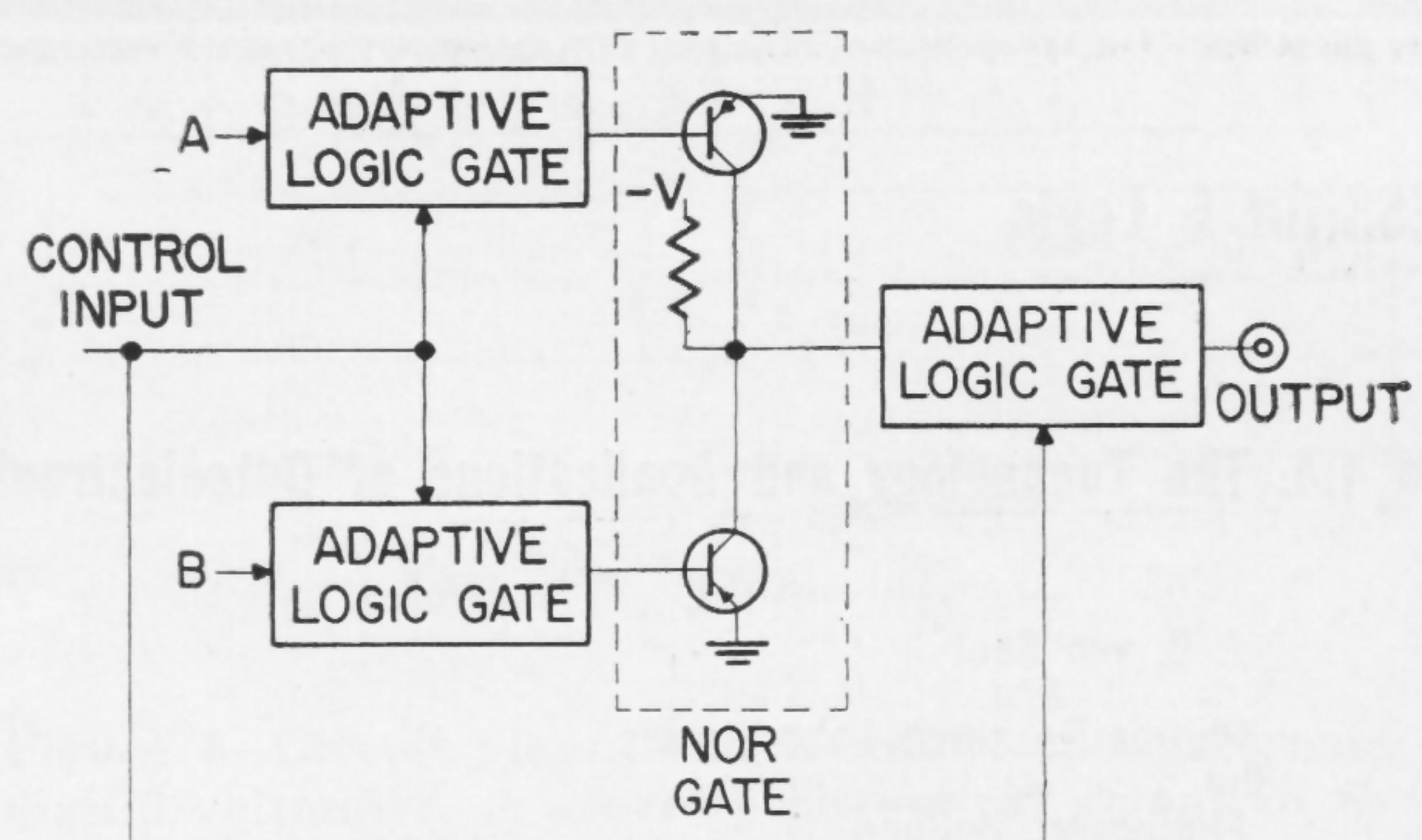


Figure 2—A two input-one output *adaptive logic net* containing three *tunnel-diode adaptive logic gates*.

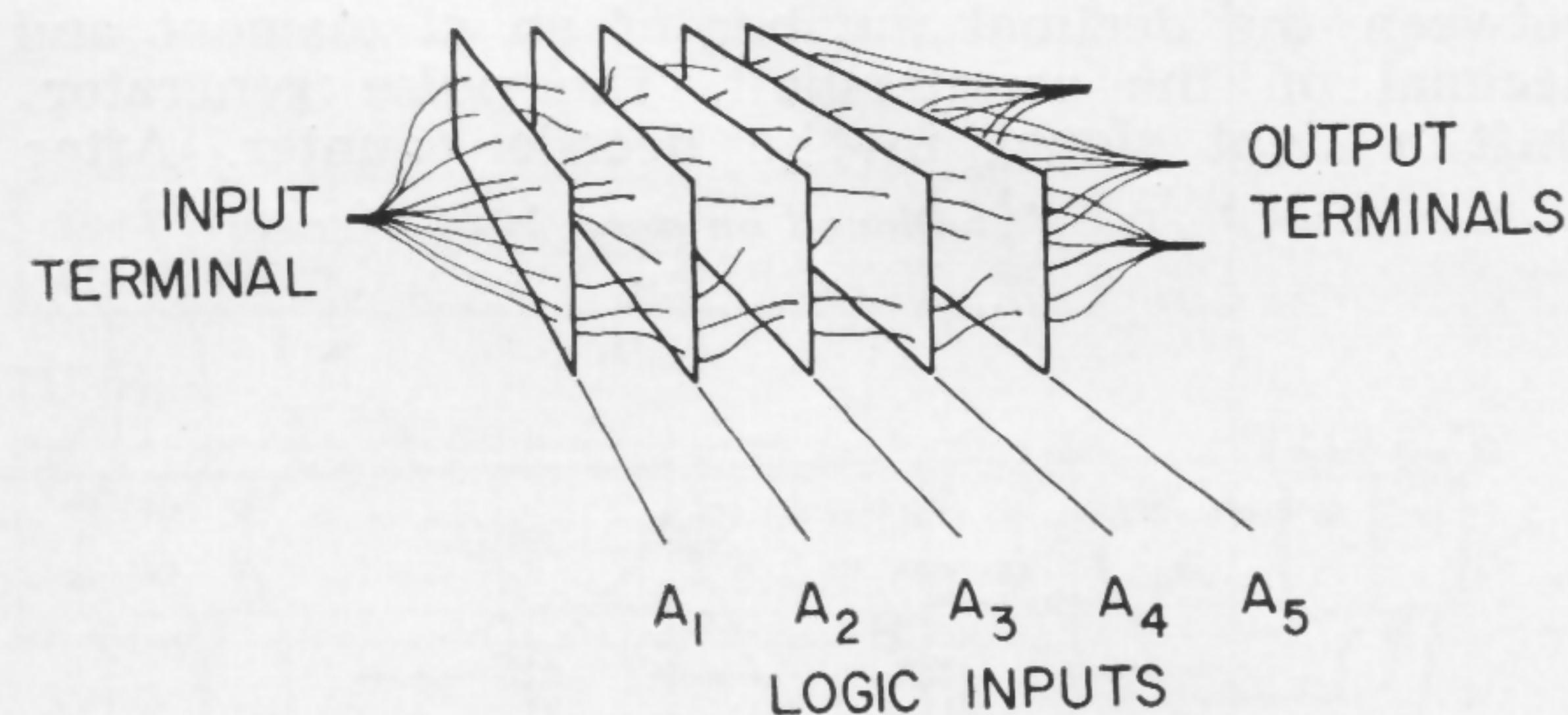


Figure 3—A five input-three output *adaptive logic net*. Each plane of the lattice structure contains *adaptive gates* and fixed logic.

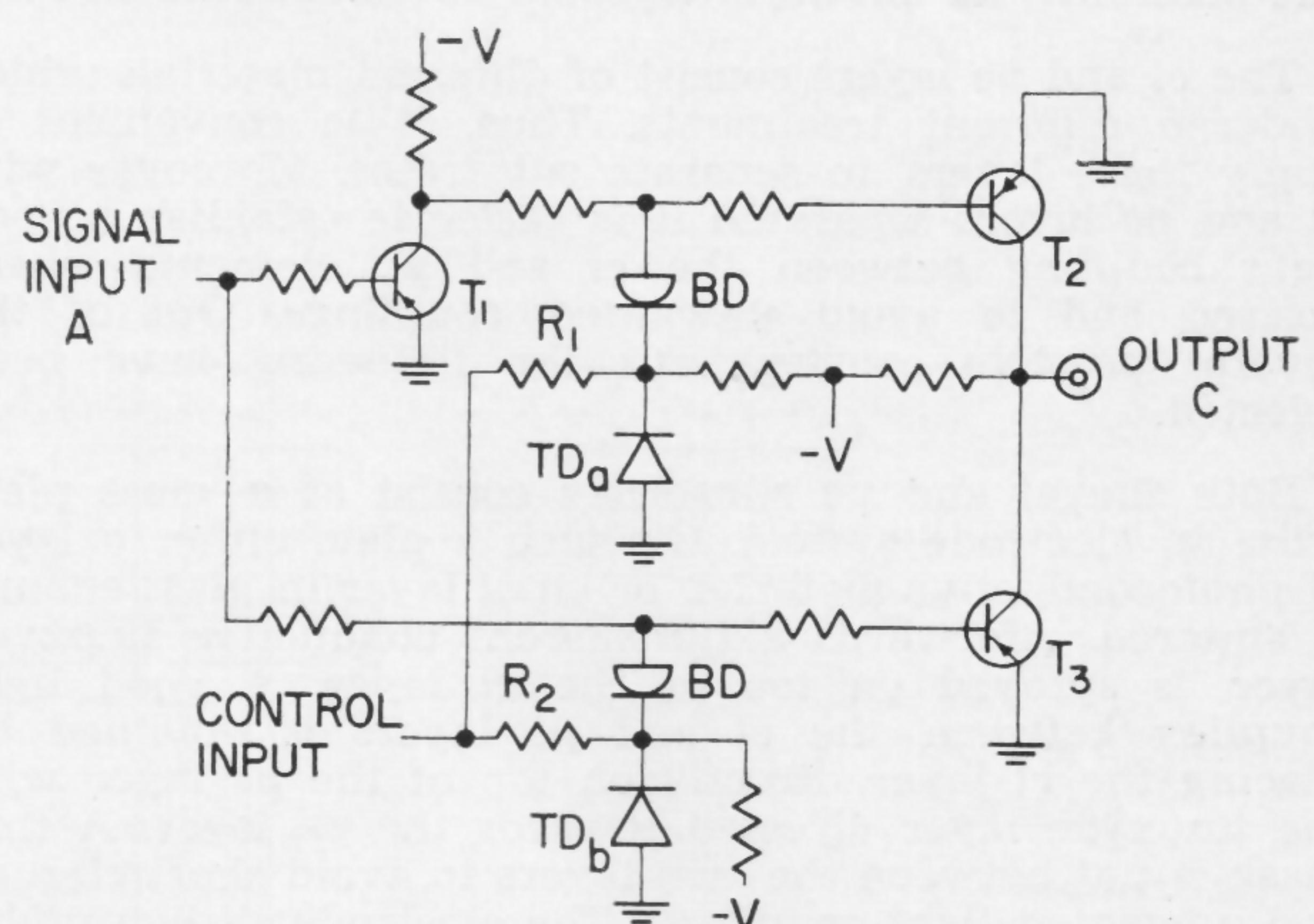


Figure 4—*Tunnel-diode adaptive gate*. The tunnel diodes are triggered by bursts of noise applied at the control input.

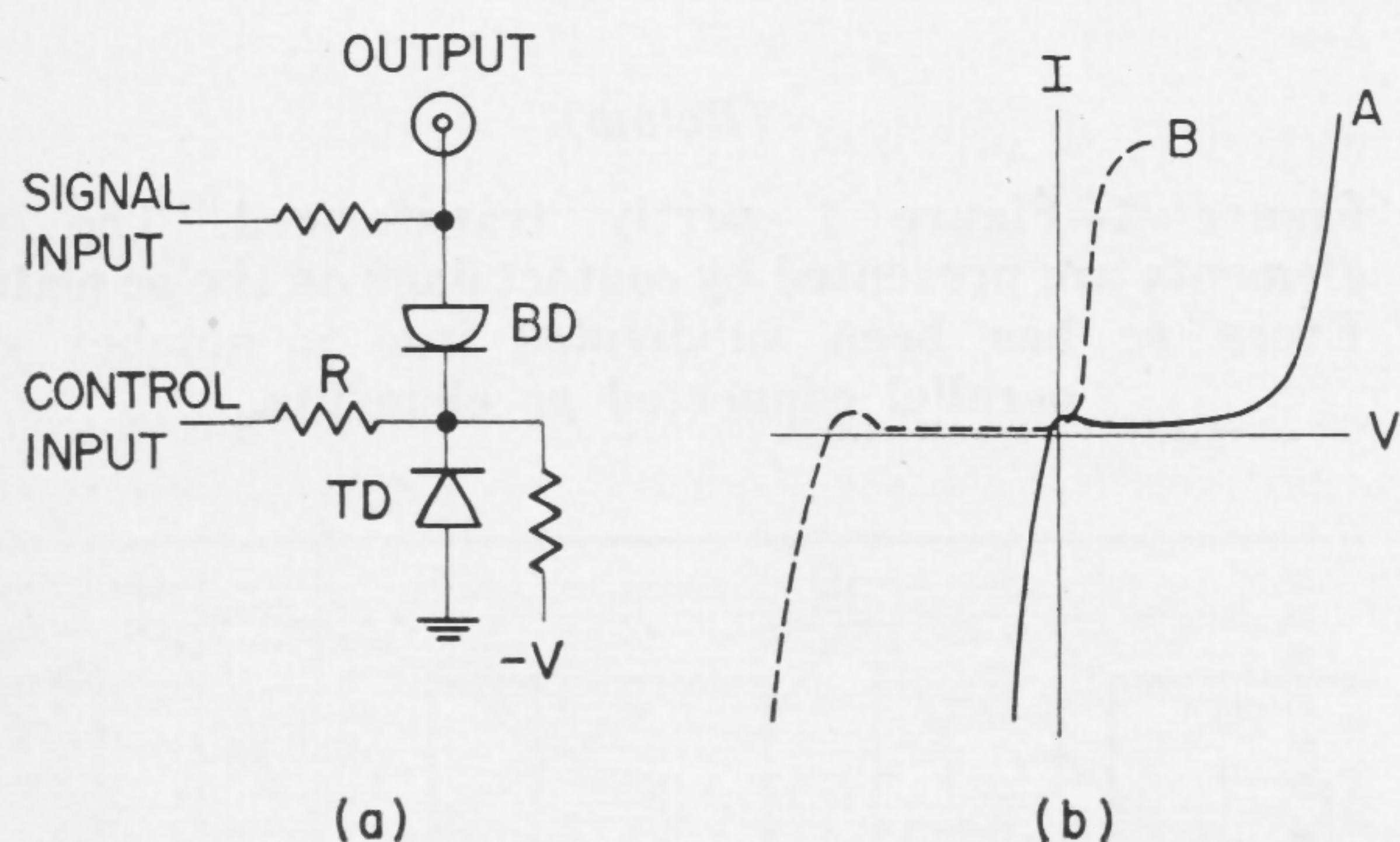


Figure 5—(a) Polarity selective gate with memory. (b) The  $I$ - $V$  characteristics of the diode branch for each mode of operation.

SIGNAL INPUT (A)	0	1	0	1	0	1	0	1
VOLTAGE STATE (TD <sub>a</sub> )	Lo	Lo	Hi	Hi	Hi	Hi	Lo	Lo
VOLTAGE STATE (TD <sub>b</sub> )	Lo	Lo	Hi	Hi	Lo	Lo	Hi	Hi
OUTPUT	I	I	0	0	0	I	I	0
FUNCTION	I	0	A	A'				

Figure 6—Truth table for an *adaptive gate*. The binary constants 1 and 0 denote voltages less than zero and equal to or greater than zero, respectively.

## SESSION I: Logic

## WM 1.4: The Technology and Applications of Optoelectronic Circuits

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ALTHOUGH OPTOELECTRONIC LOGIC circuits are rather slow, they offer attractive solutions in those cases where use can be made of their specific advantages. An important advantage of circuits consisting of a combination of electroluminescent (el) and photoconductive (pc) elements is the possibility of having integrated optoelectronic circuits.

The el and pc layers consist of different materials which undergo different treatments. Thus, it is convenient to apply these layers to separate substrates. Moreover with el and pc layers separated it is easier to establish a good light coupling between the el and pc elements where desired and to avoid unwanted couplings. Out of the several possible constructions the following have been selected.

Both the el and pc substrates consist of a glass plate with an electrode system. On such a plate either a layer of photoconductive material, or an el layer in glass enamel is sintered. Afterwards a transparent conductive tin oxide layer is sprayed on top of the el layer. A good light coupling between the el and pc layers is obtained by placing the el layer directly on top of the pc layer with the tin oxide layer directed towards the pc layer. A thin mask is put between the two layers to avoid short circuits and unwanted light couplings. The electrode system under both the el and pc layers, which divide these layers into a number of discrete elements are obtained by photoetching of the gold-plated glass substrates. The use of the photoetching technique ensures well-defined electrode systems. The use of gold gives the pc elements a good electrical characteristic. To design the prints for photoetching from a given optoelectronic circuit design on paper, certain transformations in the topological arrangements of the elements have to be carried out to realize the described construction. As an example, such a transformation of the pc ringcounter of Figure 1 is illustrated in Figures 2 and 3.

Knowing the sensitivity of the photoconductive material and the brightness-voltage characteristic of the electroluminescent layer the dimensions of the individual elements can be determined and the final print can be now constructed. It can be shown that for every given design on paper a transformation can be found, resulting in the wanted two-dimensional arrangements of elements plus electrode systems without any intersecting connections. It has been found that the removal of crossing electric connections, which implicates the introduction of an extra el-pc combination, leads to a slower response. In some cases a change of the designed circuit on paper, without changing its function, offers a better solution. This will be illustrated for a circuit applicable in a telephone exchange.

Some other applications will be discussed. The pc potentiometer of Figure 4 can be applied in a digital voltmeter because in a darkened area a pc is an isolator and the ratio between light and dark resistance can be large. The output voltage of the pc potentiometer is fixed by the illuminated pc's. The pc elements are rather slow. To speed the response of the pc potentiometer the two ringcounters  $R_1$  and  $R_2$  are shifted simultaneously. The amplifier also determines the direction of the shifting

depending on the sign of the difference between  $V_p$  and  $V_x$ .

The remote readout of meters (e.g., for electricity, gas and water) is attractive, but the feasibility depends to a large degree on the practical solution of the readout circuit for the mechanical counters, because this unit is present in every meter. A solution for this is the optoelectronic circuit shown in Figure 5. Only the simplified readout circuit has been given. The methods of selection and data transmission will not be considered in this paper. For the readout one of the counter shafts  $c_n - c_1$  is selected by the selector. In the decade one out of ten el elements is actuated. There exists a one-to-one correspondence between the decimal number of an el element and the decimal on the countershaft. The pulse generator will shift a light signal in the decade counter. After the

[Continued on page 104]

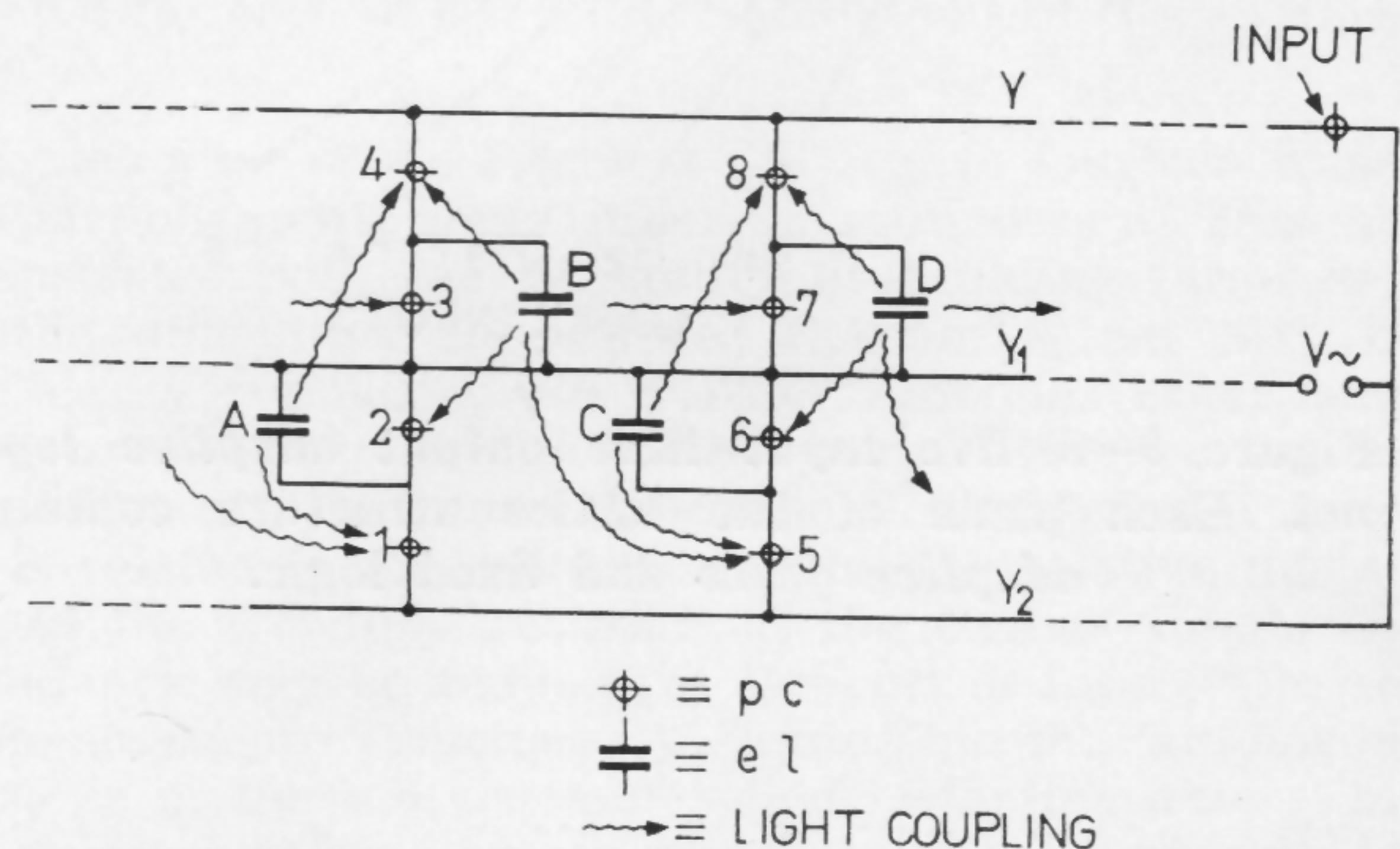
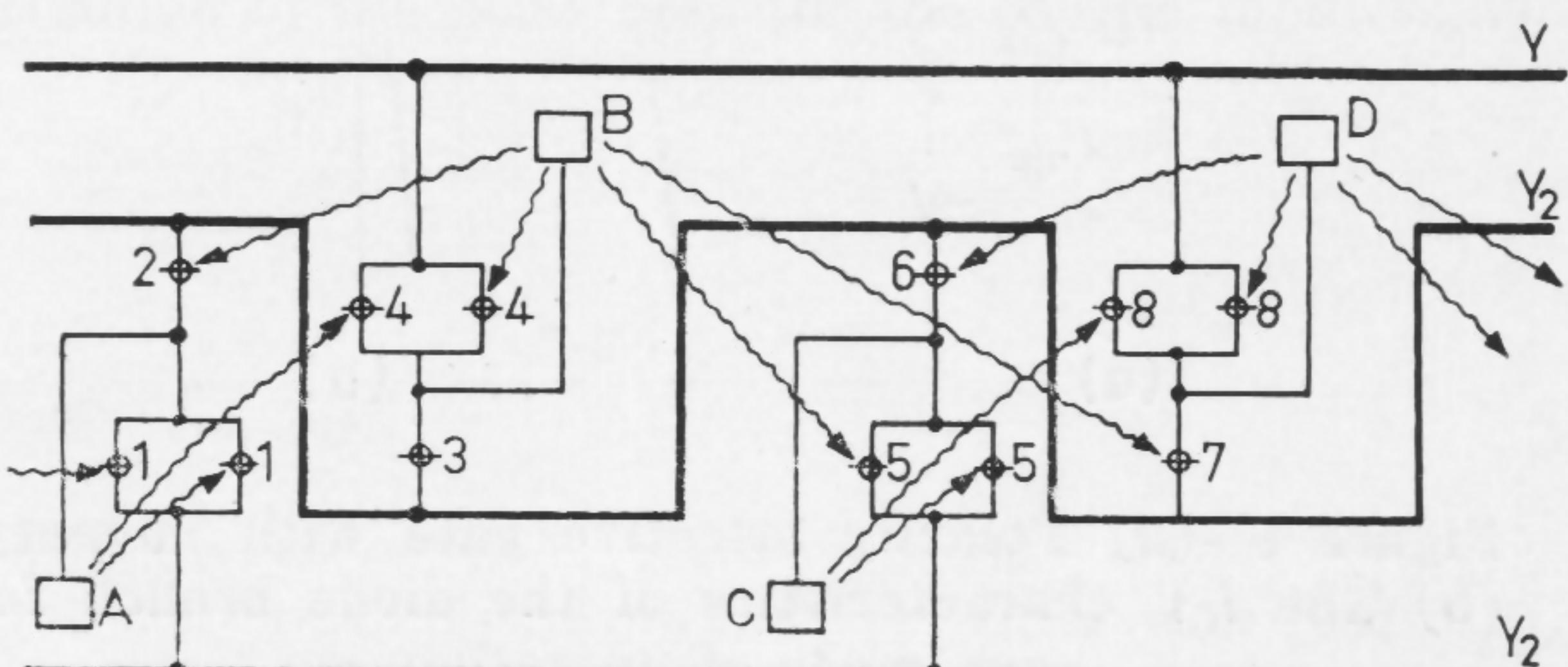


Figure 1—Part of a ringcounter. When el element A is on, this stable situation can be transferred to element C via transfer stage B by the input signal.

(Below)

Figure 2—Figure 1 partly transformed. The el elements are presented by contact flags on the pc plate. Every pc has been subdivided into a number of parallel connected pc elements.



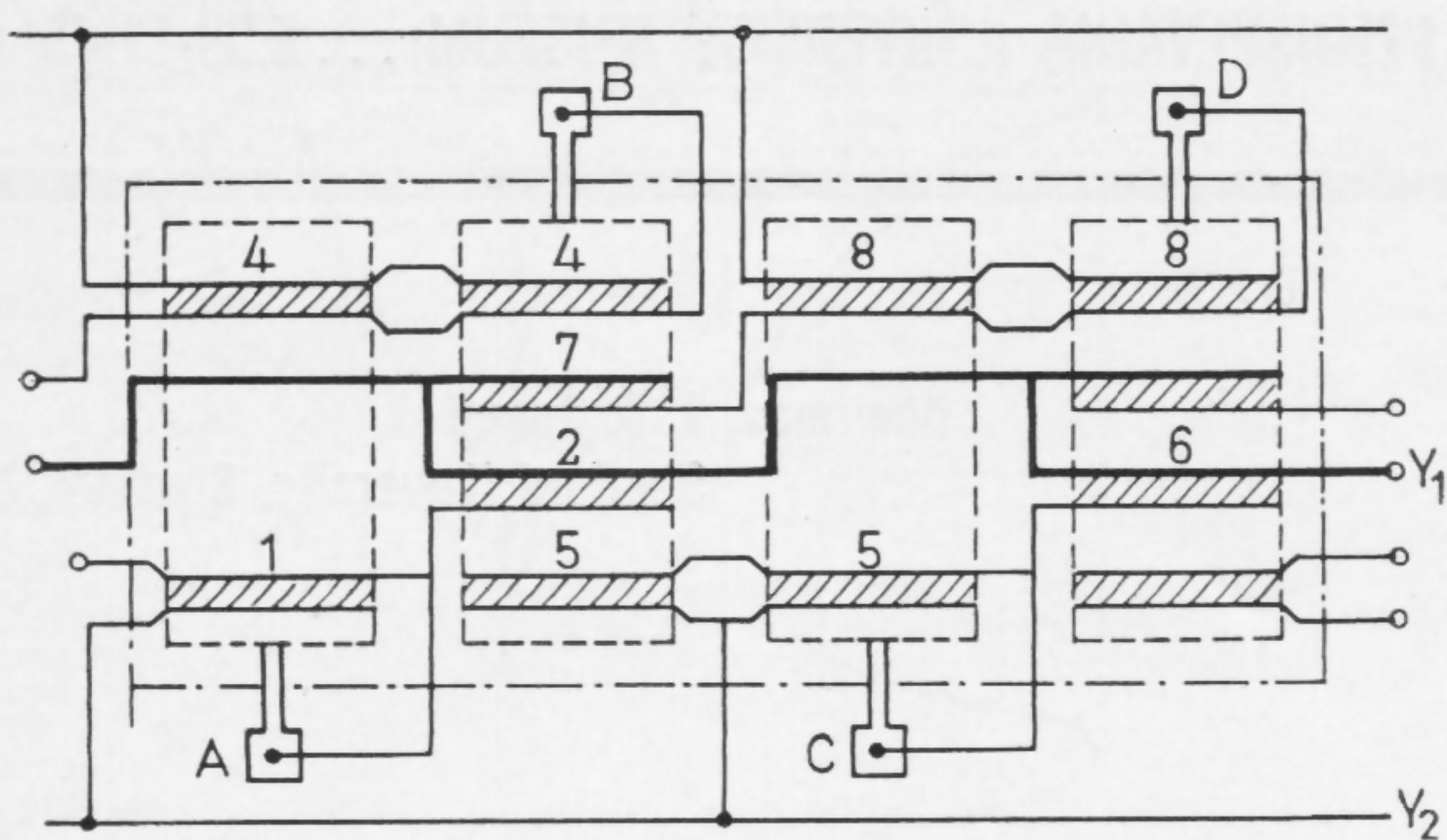


Figure 3—The reduced form of the prints. The electrodes of the *el* elements are indicated by the dashed lines. The tinoxide electrode is drawn as a dot-dash line.

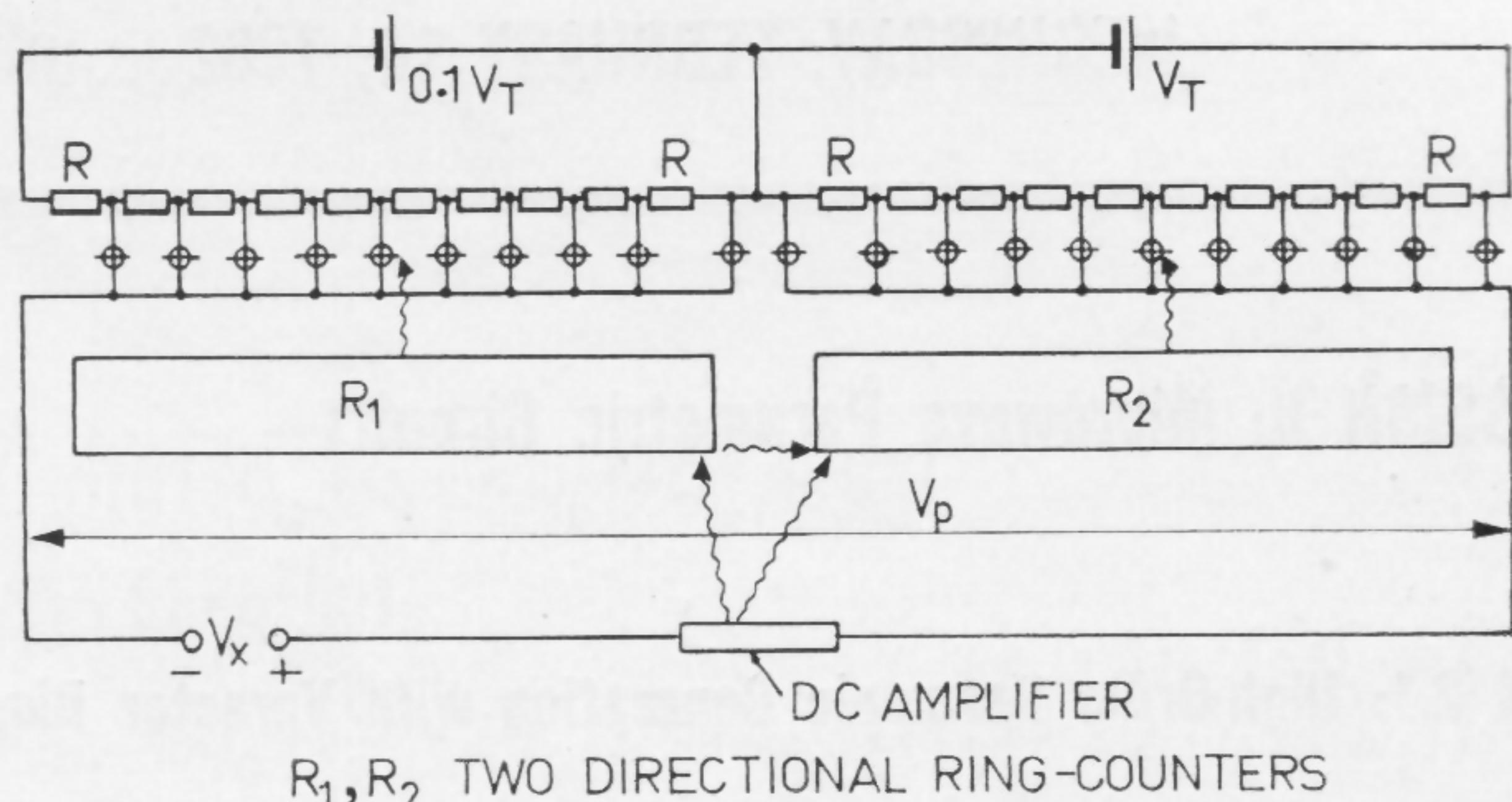


Figure 4—Circuit diagram of a simple optoelectronic digital voltmeter. *A* provides an optical signal to  $R_1$  when  $|V_x - V_p| \geq .01 V_T$ . An additional signal is given to  $R_2$  when  $|V_x - V_p| \geq .1 V_T$ .

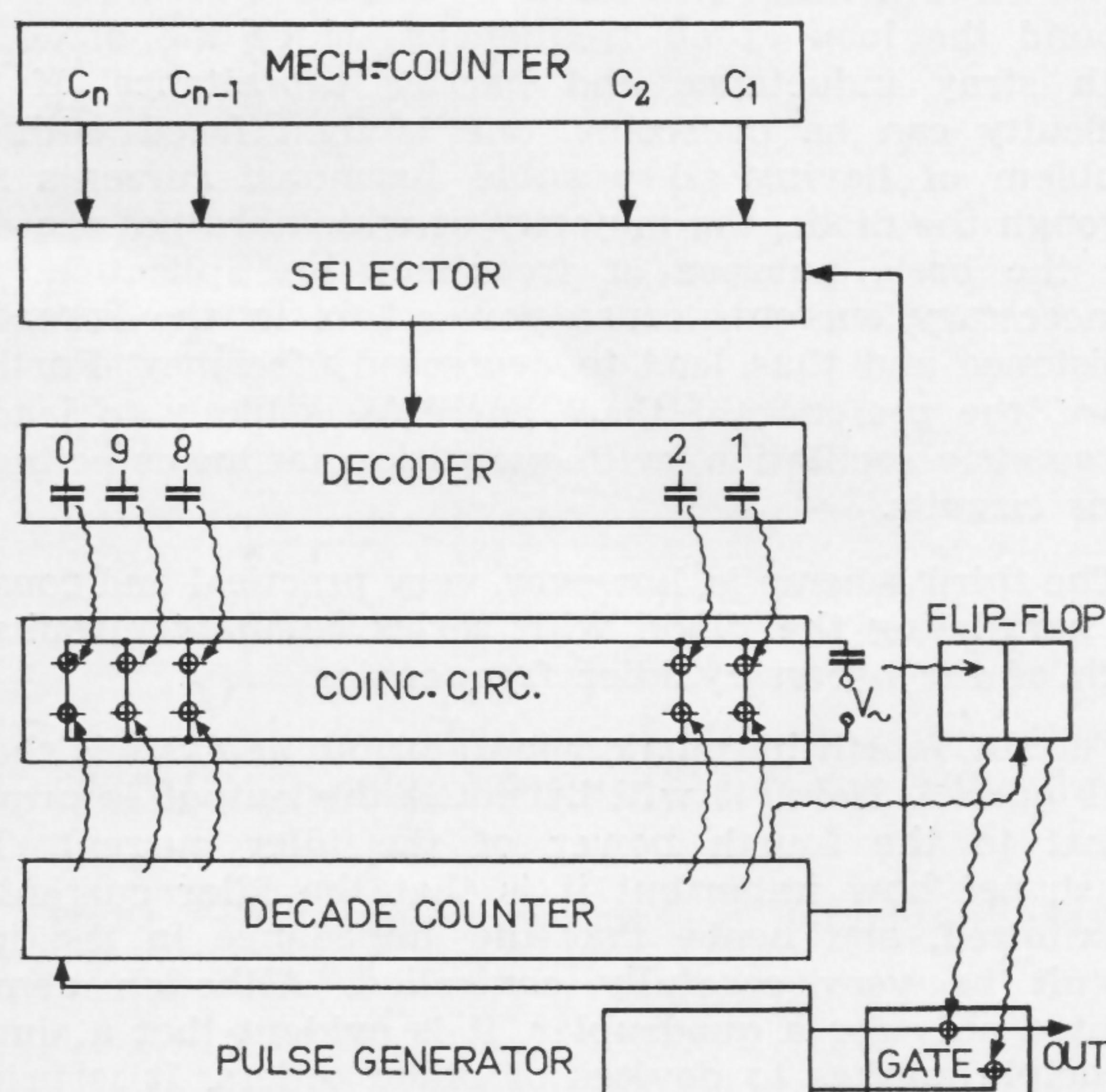


Figure 5—Simplified block diagram of an *el-pc* readout circuit. The coincidence circuit will give a signal when two in series-connected *pc*'s are simultaneously illuminated.

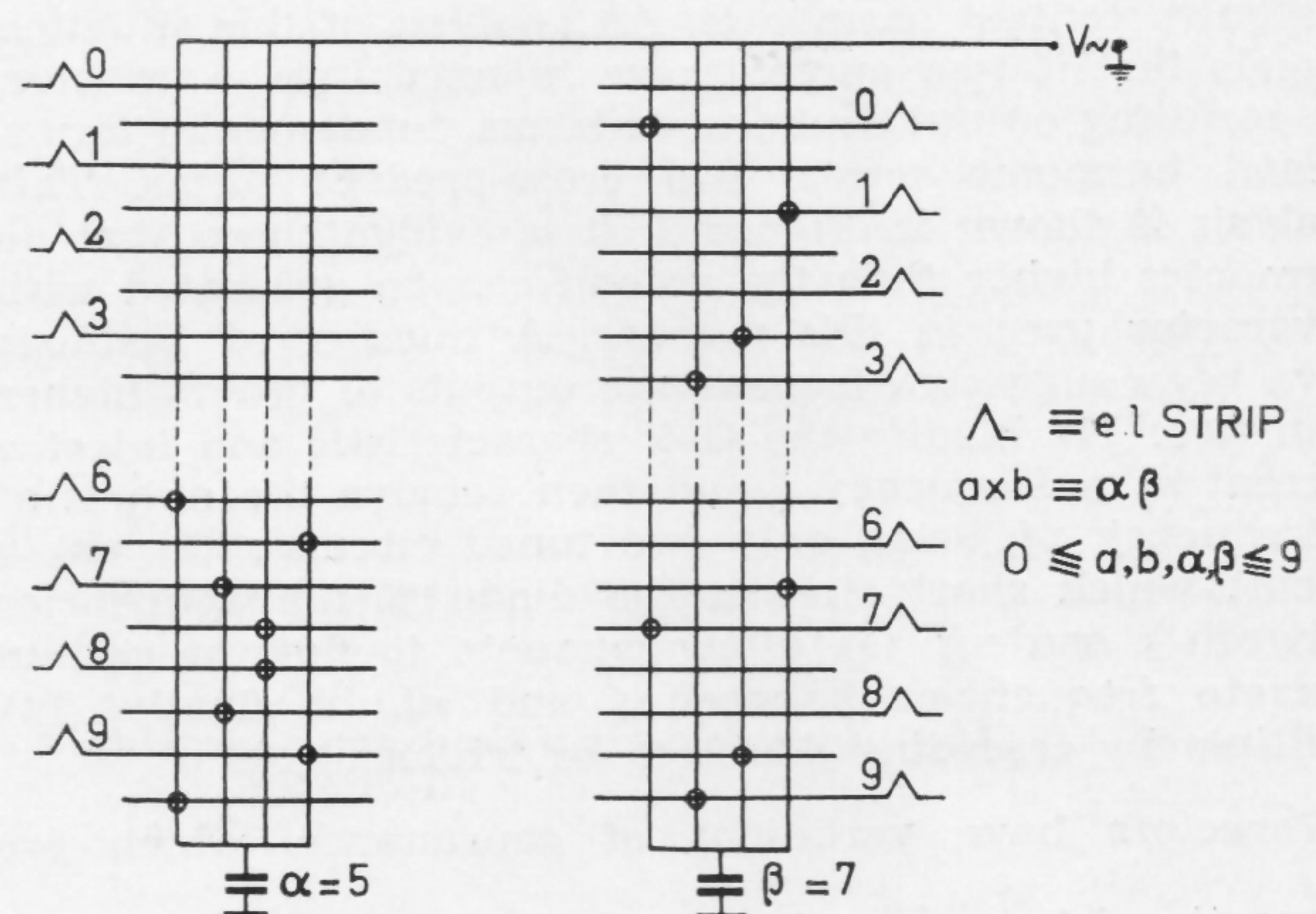


Figure 6—Scheme of an *el-pc* multiplication matrix. The connections for the multiplications giving  $\alpha = 5$  and those giving  $\beta = 7$  have been indicated.

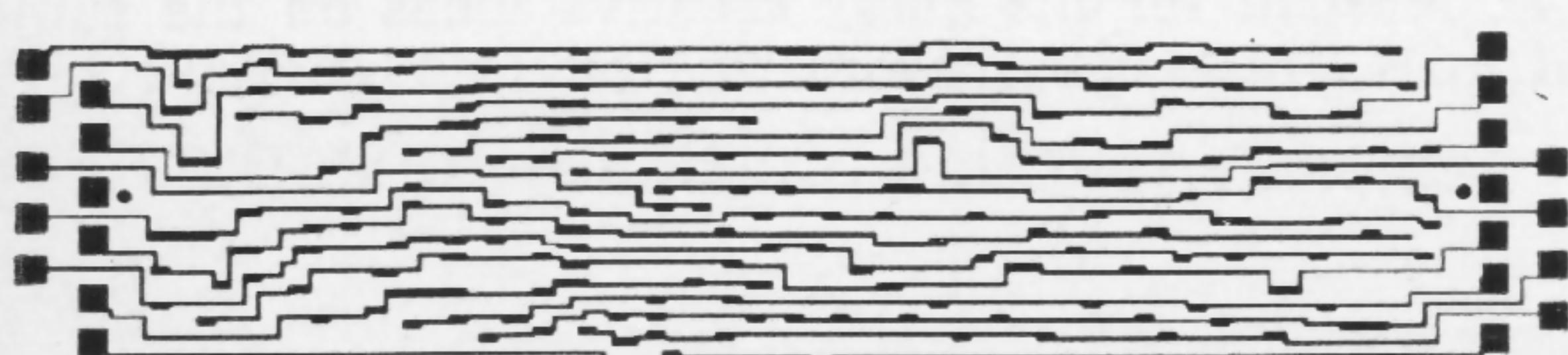


Figure 7—Print of the *el* electrode system for a multiplication matrix. The dimensions are  $10.3 \times 2.3 \text{ cm}^2$ .

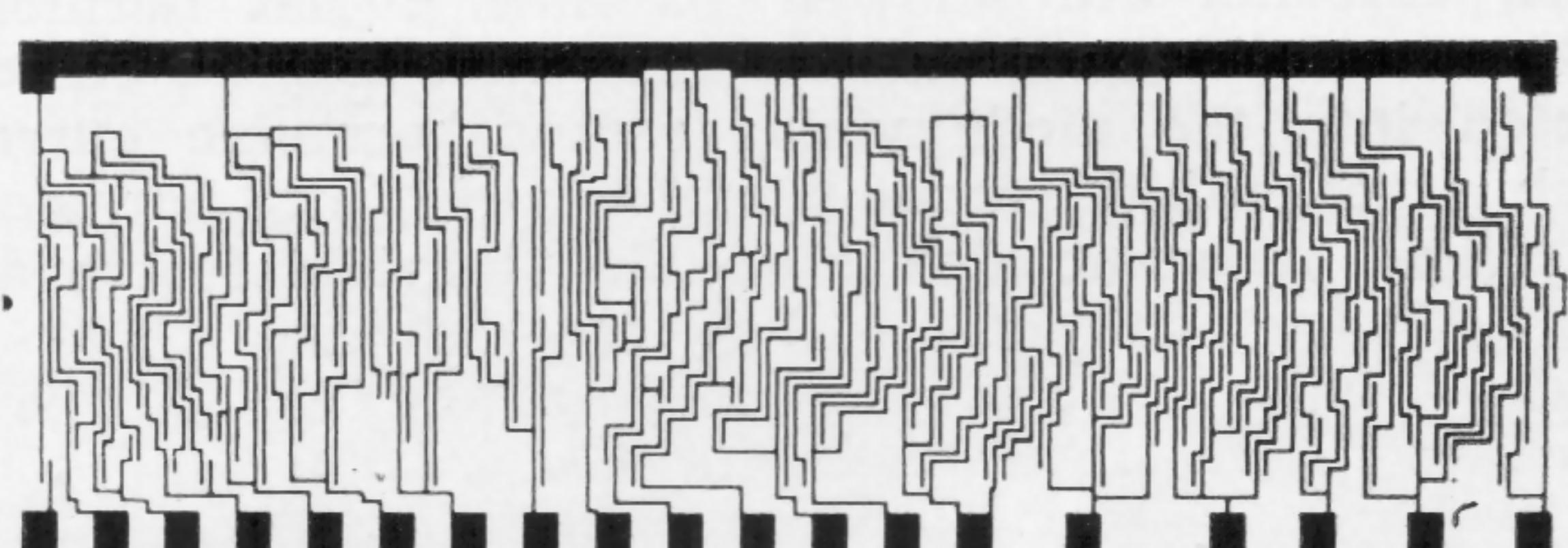


Figure 8—Print of the *pc* electrode system for a multiplication matrix. The dimensions are  $9 \times 3 \text{ cm}^2$ .

## SESSION II: Microwave Parametric Circuits

Chairman: J. B. Angell

Stanford University, Stanford, Calif.

## WM 2.1: High-Order Harmonic Generation with Varactor Diodes

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EFFICIENT PASSIVE HARMONIC generation, which have yielded the varactor, has been made possible by advancements in semiconductor technology. This device exhibits a square-law charge-voltage characteristic capable of mixing or doubling with efficiencies approaching unity.

Frequency doubling or mixing is ordinarily accomplished by injecting sinusoidal charge variation (current) and removing the resultant voltage. This is illustrated in Figure 1 which shows a sinusoidal current injected into a square-law charge-voltage device; the resultant output is seen to contain harmonics. An analysis of this situation reveals that if two currents are injected into a varactor, the resulting output contains dc terms, fundamental terms, second harmonic terms, and cross-product terms. This analysis is shown in Figure 2. It is evident here that no harmonics higher than the second can be generated with a varactor used in this manner. A number of methods have been suggested to generate outputs of orders higher than two: (1) Modify the Q-V characteristic and inject a current at a frequency  $f$  and then remove the output at a frequency  $nf$ , using only two tuned circuits; (2) use a circuit which short circuits the diode at all frequencies between  $f$  and  $nf$ ; (3) allow currents to flow at certain discrete frequencies between  $f$  and  $nf$ , or finally, (4) multiply by cascading doublers, or triplers.

Varactors have variations of capacitance which are proportional to  $V^{-\frac{1}{m}}$  where  $m$  is a number lying between

2 for an abrupt junction device and 3 for a diffused junction device. These two curves are plotted in Figure 3 and it can be seen that the two are very similar. In fact, in Figure 4 they are shown displaced such that they lie close to each other. The difference amounts to only a slight change in the shunt capacity and of the bias voltage applied to the device. Hence, all varactors behave essentially as square-law devices and cannot generate high harmonics directly.

The second method, which is to imbed the diode in series between two parallel resonant circuits at  $f$  and  $nf$ , can generate high harmonics. This is true because, in the model, currents are allowed to flow at all harmonic frequencies between  $f$  and  $nf$ . Any fundamental current injected into the diode yields second-harmonic current which mixes with the fundamental to yield third harmonic; the second harmonic also is doubled to yield fourth and

this in turn mixes with the first to give fifth, and so on. Thus, this device is at least theoretically capable of generating high order harmonics.

A number of problems arise in connection with the series circuit. First, it is difficult to insure zero reactance around the loop at all frequencies, since the diode has both stray inductance and barrier capacitance. If this difficulty can be overcome, one is then faced with the problem of having all possible harmonic currents flow through the diode, the majority of which are not required for the basic purpose of frequency multiplication. The unnecessary currents cause power loss in the spreading resistance and thus lead to decreased efficiency. Furthermore, the presence of these currents is likely to lead to parametric oscillation, with parasitic reactances acting as idler circuits.

The third scheme is, however, very practical and consists of paralleling the diode with series resonant circuits at each of the necessary idler frequencies.

For the fourth harmonic generator, an analysis is shown in Figure 5. Here, it will be noted the output is proportional to the fourth power of the idler current. This illustrates how important it is that the idler current be maximized, and hence that the impedance in the idler circuit be very carefully controlled. Although demonstrated only for a quadrupler, it is evident that a similar principle applies to devices of other orders. It is principally for this reason that the idler tanks are necessary, as it is very difficult to build a circuit without adjustments which have the correct impedance at the several idler frequencies necessary.

The results of an experimental verification of the fourth power relationship between idler current and power output are shown in Figure 6.

Harmonic generators of orders 2, 4, 8 and 16 were built and their efficiencies were studied. In all cases the output frequency was 1600 Mc. Efficiencies of 55, 45, 32, and 10%, respectively, were obtained.

**Acknowledgements**

The author is grateful to D. Linden and B. Herzog for their helpful comments on the preparation of this paper, to H. Morgan for his many creative ideas on the subject, and to H. Hasin for construction of the circuits.

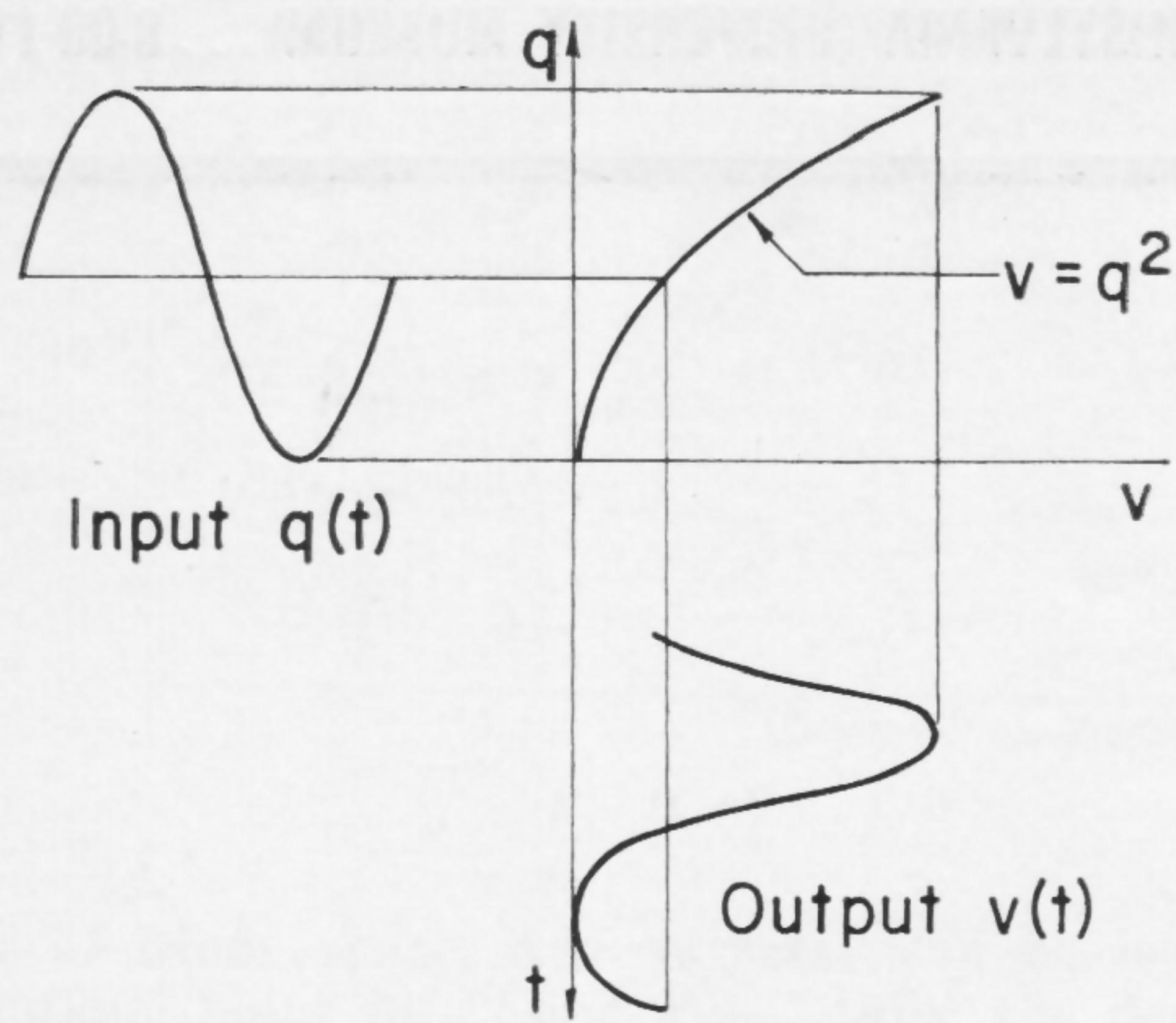


Figure 1—Transfer characteristics of varactor diode.

$$\begin{aligned}
 q(t) &= Q_0 + Q_1 \sin \omega_1 t + Q_2 \sin \omega_2 t \\
 v(t) &= q^2(t) \\
 &= Q_0^2 + \left(\frac{Q_1^2}{2} + 2Q_0 Q_1 \sin \omega_1 t\right) + \left(\frac{Q_2^2}{2} + 2Q_0 Q_2 \sin \omega_2 t\right) \\
 &\quad - \frac{Q_1^2}{2} \sin 2\omega_1 t - \frac{Q_2^2}{2} \sin 2\omega_2 t \\
 &\quad + Q_1 Q_2 \cos(\omega_1 - \omega_2) t - Q_1 Q_2 \cos(\omega_1 + \omega_2) t
 \end{aligned}$$

Figure 2—Harmonic generation and mixing in a varactor diode.

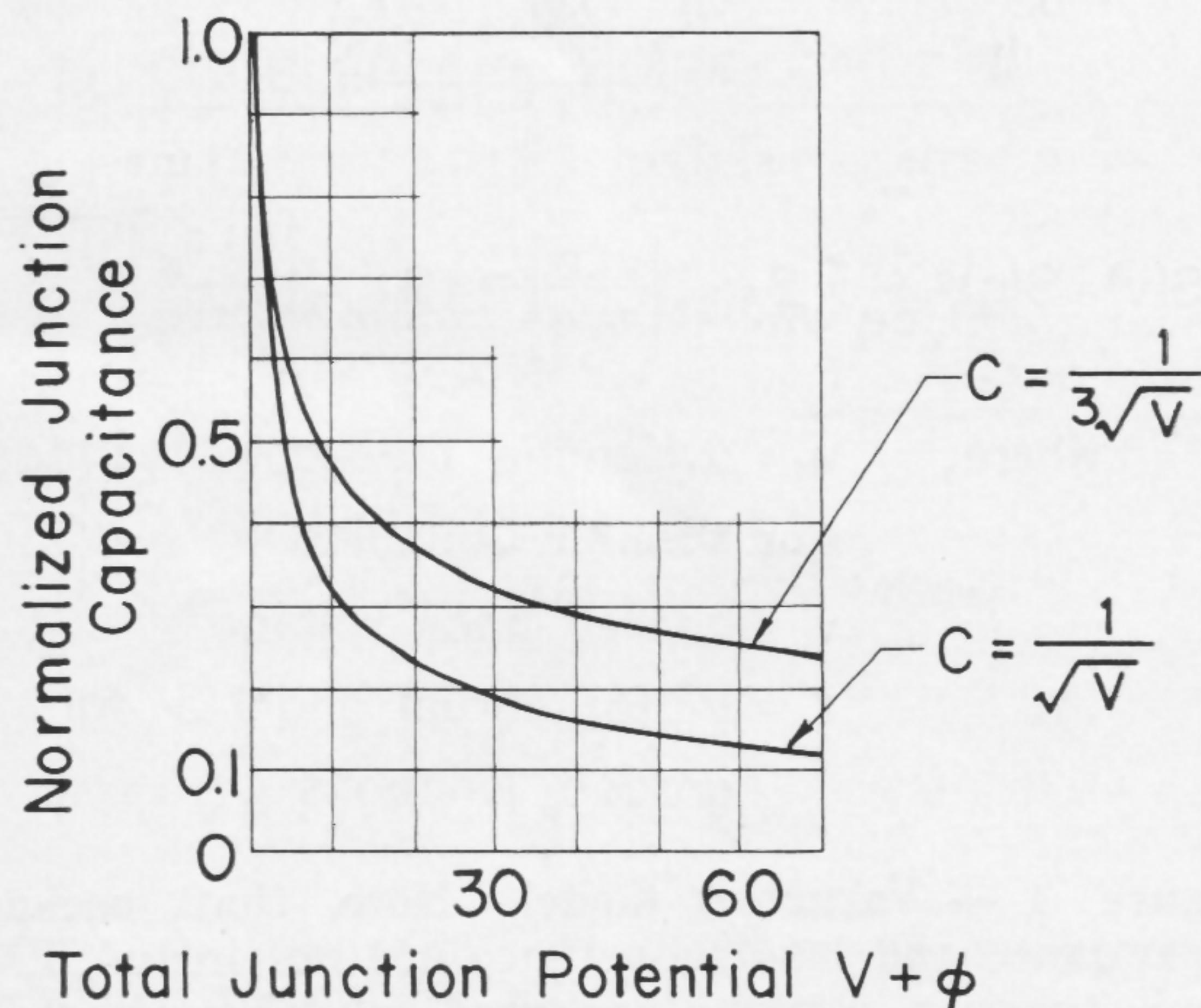


Figure 3—Junction capacitance of varactor diodes.

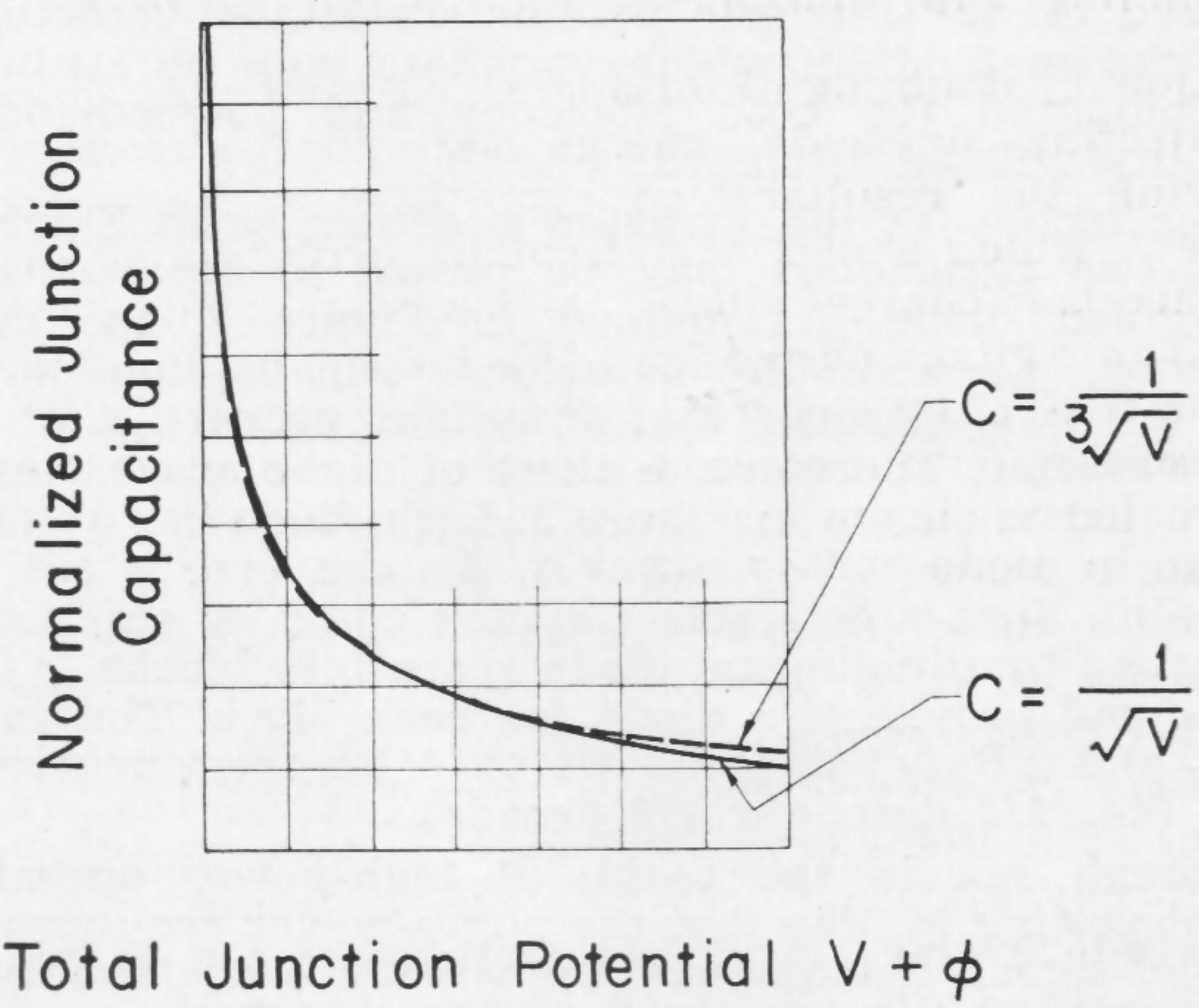
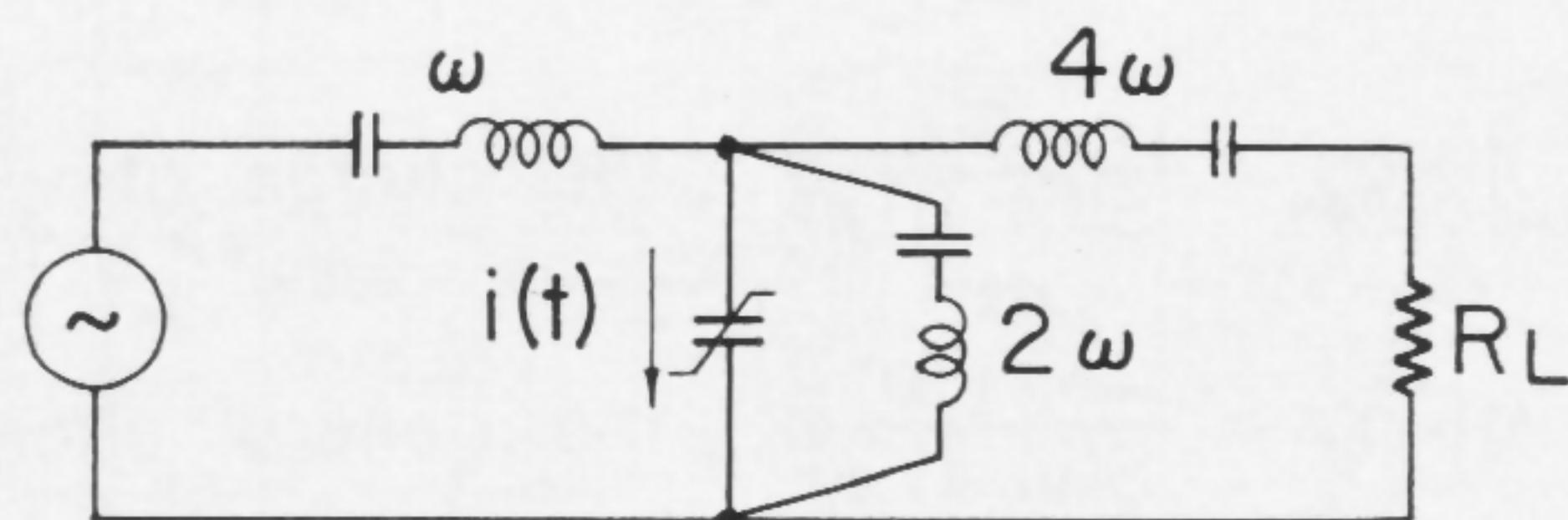


Figure 4—Superposition of curves given in figure 3.



Let  $i(t) = I_1 \sin \omega t + I_2 \cos 2\omega t - I_4 \cos 4\omega t$   
 Integrate  $i(t)$  to obtain  $q(t)$   
 Operate on  $q(t)$  to obtain  $v(t)$   
 Solution of resulting equations yields:

$$\text{Power Output} \approx I_2^4$$

Figure 5—Analysis of varactor quadrupler.

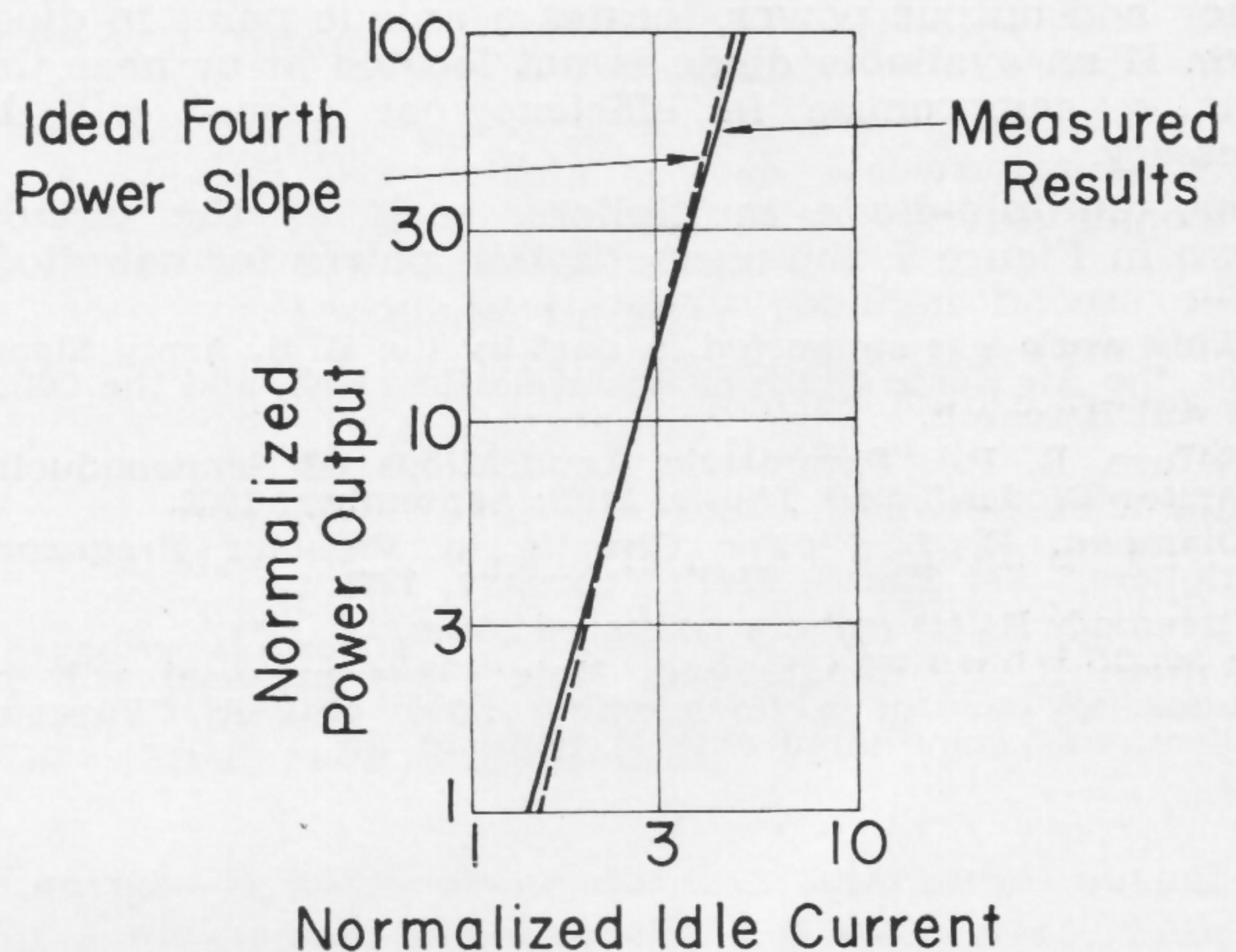


Figure 6—Power output as a function of idle current for varactor quadrupler.

## SESSION II: Microwave Parametric Circuits

## WM 2.2: High Power Operation of Varactor Devices\*

R. P. Rafuse

Research Laboratory of Electronics, MIT  
Cambridge, Mass.

THE INCREASED INTEREST in obtaining moderate output powers from varactor devices, in the order of tens of watts, has resulted in a need for a suitable *goodness* criterion. Any method for comparing the potential of various varactors should be circuit-independent and should be based on the intrinsic parameters of the varactor. A successful method by which varactors may be evaluated and compared for both efficiency and power-handling capability will be discussed.

If the model for the varactor is chosen as in Figures 1 and 2, two parameters may be picked as representative of a given diode. As defined in Figure 2, the cutoff frequency,  $f_c$ , and the varactor normalization power,  $P_{norm}$ , are two intrinsic and invariant properties of any given varactor. Therefore, a chart of diode space may be constructed as shown in Figure 3. Each diode has a unique position in diode space; however, the converse is not true at present. Such a desirable situation could be approached in practice by dividing up diode space into blocks,  $\Delta f_c$  by  $\Delta P_{norm}$ , and providing a diode for each block. The values of  $\Delta f_c$  and  $\Delta P_{norm}$  might be set by a log-increment technique (i.e., 1/3 decade  $\times$  1/3 decade).

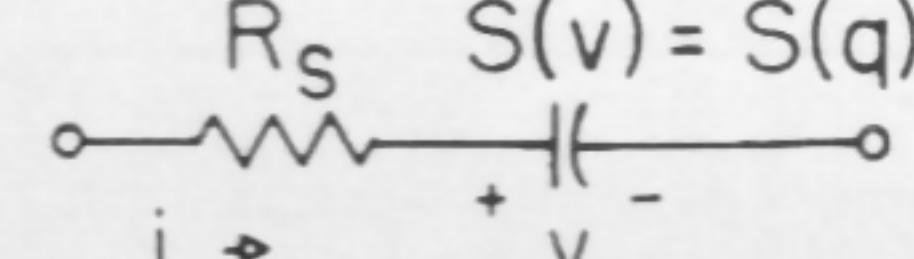
Although not in the realm of high-power operation, it is interesting to note that the pump-power requirements of small-signal devices can be written very simply in terms of  $f_c$  and  $P_{norm}$ <sup>1</sup>. The formula will be found in Figure 4, together with the power required to pump at the optimum pump frequencies (for signal frequencies  $\ll f_c$ ).

The maximum efficiency of frequency multipliers is entirely a function of the ratio of the output frequency to the cutoff frequency. Similarly, if the output power (or input power) is normalized by dividing by  $P_{norm}$ , it, too, becomes a function of the normalized output frequency. The maximum efficiency and normalized output power for x2, x3, x4, x5 and x6 harmonic multipliers are shown as functions of  $F = f_{output}/f_c$  in Figures 5 and 6<sup>1,2,3</sup>. A given output frequency, together with a required efficiency and output power, locates a unique point in diode space. If an available diode is not located at or near this point, a compromise in efficiency or power will be necessary.

For multiple-diode multipliers, such as the circuits shown in Figure 7, the normalization power for one diode

is simply multiplied by the number of operating diodes (provided they are identical), while the efficiency remains

[Continued on page 104]



$$S(v) = S(q) = \frac{dv}{dq} = S_{max} \left[ \frac{v + \phi}{V_B + \phi} \right]^{\gamma} = S_{max} \left[ \frac{q + q_{\phi}}{Q_B + q_{\phi}} \right]^{\frac{1}{1-\gamma}}$$

where,  $V_B$  = avalanche breakdown voltage  
 $\phi$  = contact potential  
 $v$  = applied back voltage  
 $\gamma$  = 1/2 for abrupt and 1/3 for  
 graded junctions

Figure 1 — Varactor model. Note that package capacitance and lead inductance are *not* included. A given junction may be packaged in different ways; therefore, the package elements properly belong to the external circuit.

(Below)

Figure 2—Varactor parameters for the model of Figure 1. Note that the varactor cutoff frequency and normalization power are *invariant* to the operation of the varactor in any particular circuit.

$$Q_B + q_{\phi} = \frac{V_B + \phi}{S_{max}(1-\gamma)}, \text{ the charge at } V_B$$

$$q_{\phi} = \frac{\phi}{S(0) \cdot (1-\gamma)}, \text{ the charge at } v=0$$

$$q + q_{\phi} = \frac{v + \phi}{S(v) \cdot (1-\gamma)}, \text{ the general charge}$$

$$f_c = \frac{1}{2\pi} \frac{S_{max}}{R_S}, \text{ the cutoff frequency}$$

$$P_{norm} = \frac{(V_B + \phi)^2}{R_S}, \text{ the normalization power}$$

\* This work was supported in part by the U. S. Army Signal Corps, the Air Force Office of Scientific Research, and the Office of Naval Research.

<sup>1</sup> Rafuse, R. P., "Parametric Applications of Semiconductor Capacitor Diodes," ScD Thesis, MIT; September, 1960.

<sup>2</sup> Diamond, B. L., "Idler Circuits in Varactor Frequency Multipliers," SM Thesis, MIT; February, 1961.

<sup>3</sup> Diamond, B. L., private communication.

<sup>4</sup> Rafuse, R. P., unpublished. Note: This material will be included as part of a forthcoming book entitled "Varactor Applications," coauthored with P. Penfield, Jr.

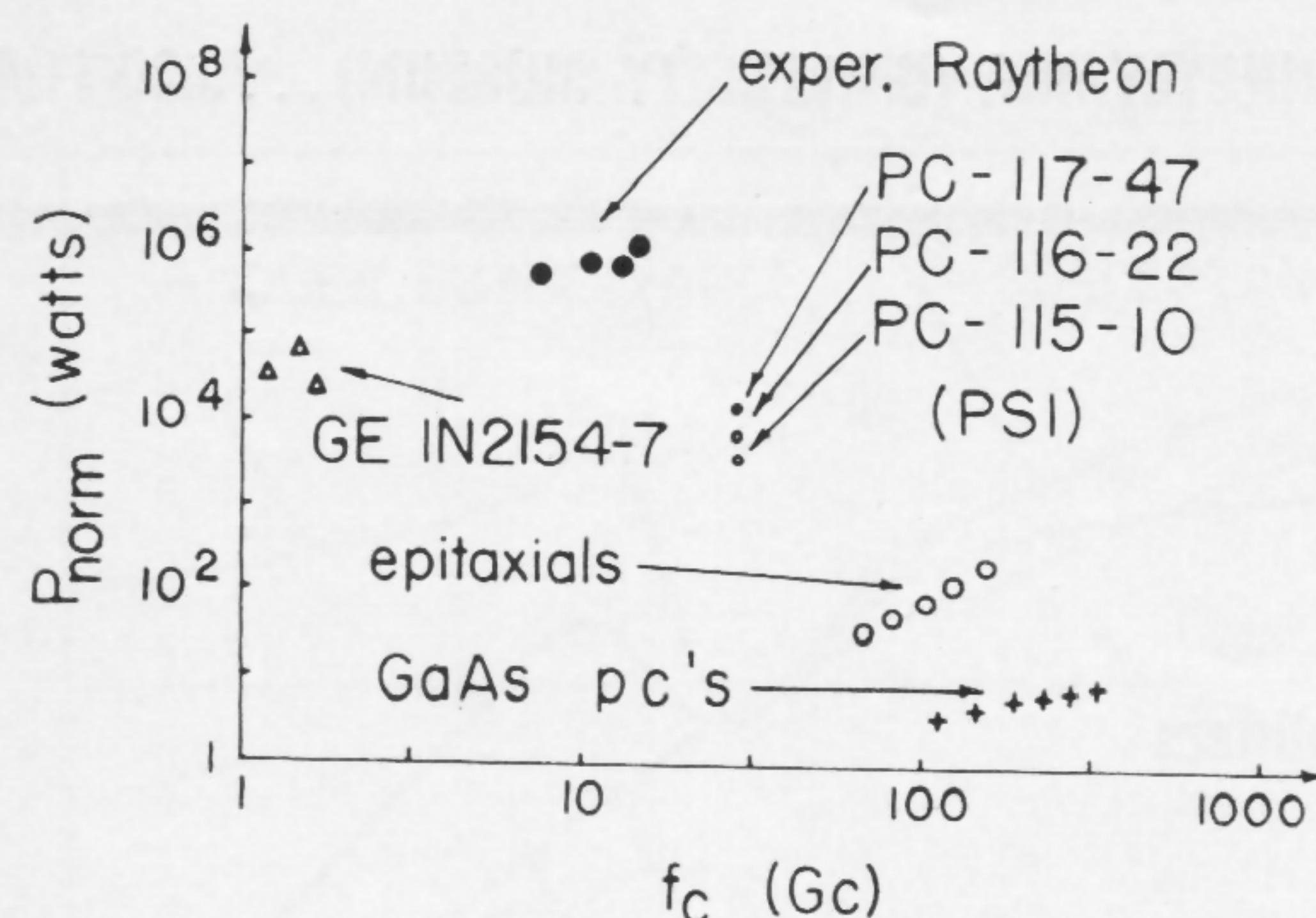


Figure 3—Diode space. Any varactor can be located as a unique point by  $f_c$  and  $P_{norm}$ . Once the desired diode parameters for a given circuit have been chosen, an examination of diode space will decide the availability of such a diode.

$$\begin{aligned}
 \text{DOUBLER (1,2)} & \quad \text{TRIPLER (1,2,3)} \\
 1 - 10F + 40F^2 & \quad 1 - 12.6F + 62F^2 \\
 \text{QUADRUPLER (1,2,4)} & \quad F = \frac{f_{\text{output}}}{f_c} \\
 1 - 15.8F + 80F^2 & \\
 \text{QUINTUPLER (1,2,4,5)} & \\
 1 - 18.7F + 207F^2 - 1290F^3 + 2900F^4 & \\
 \text{SEXTUPLER (1,2,4,6)} & \\
 1 - 21.3F + 341F^2 - 2060F^3 &
 \end{aligned}$$

Figure 5—Efficiency of various abrupt-junction harmonic multipliers as a function of normalized output frequency. The equations hold for values of  $f_{\text{out}}/f_c$  up to 1/10.

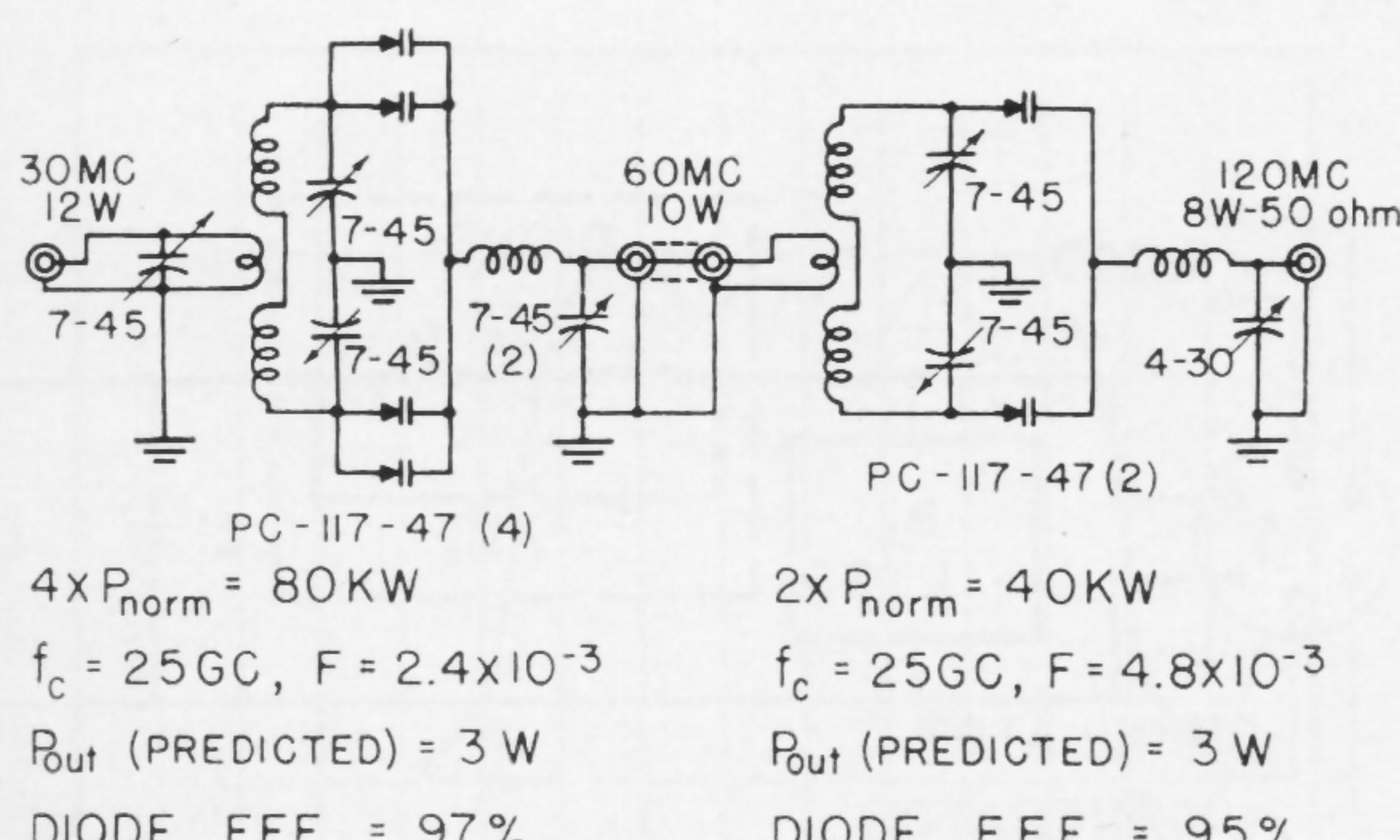


Figure 7—Medium-power cascade of two symmetric doublers. Some overdriving results in power levels in excess of theoretical (8 to 10 watts out as compared to 3 watts predicted).

$$P_p = \frac{1}{8(1-\gamma)^2} \left[ \frac{f_p}{f_c} \right]^2 P_{\text{norm}}$$

At the optimum pump frequency, with  $f_s$ , the signal frequency,  $\ll f_c$ ,

$$P_{p0} = \frac{1}{32} P_{\text{norm}} \text{ for } \gamma = 1/2$$

$$P_{p0} = \frac{1}{79} P_{\text{norm}} \text{ for } \gamma = 1/3$$

Figure 4—Pump-power requirements for abrupt- and graded-junction varactors. Values given are for maximum pumping for parametric amplifiers and upconverters.

$$\begin{aligned}
 \text{DOUBLER (1,2)} & \quad \text{TRIPLER (1,2,3)} \\
 P_0 = 1.6 \times 10^{-2} F [1 - 3.75F] & \quad P_0 = 6.85 \times 10^{-3} F [1 - 6.45F + 21F^2] \\
 \text{QUADRUPLER (1,2,4)} & \\
 P_0 = 4.75 \times 10^{-3} F [1 - 8.90F + 1.4F^2 + 220F^3] & \\
 \text{QUINTUPLER (1,2,4,5)} & \\
 P_0 = 3.26 \times 10^{-3} F [1 - 0.05F - 224F^2 + 1618F^3] & \\
 \text{SEXTUPLER (1,2,4,6)} & \\
 P_0 = 2.93 \times 10^{-3} F [1 - 0.05F - 224F^2 + 1618F^3] & \\
 F = \frac{f_{\text{output}}}{f_c} & \quad P_0 = \frac{P_{\text{output}}}{P_{\text{norm}}}
 \end{aligned}$$

Figure 6—Power-handling ability of various abrupt-junction harmonic multipliers as a function of normalized output frequency. The equations hold for values of  $f_{\text{out}}/f_c$  up to 1/10.

$$\begin{aligned}
 DR = 208 - 10 \log_{10} B - 15 \log_{10} \frac{f_c^2}{f_s f_u} - 10 \log_{10} (1 + t_{\text{ant}}) \\
 + 10 \log_{10} P_{\text{norm}} \text{ db}
 \end{aligned}$$

where,  $B$  = bandwidth in cps  
 $f_s$  = signal frequency  
 $f_u$  = upper-sideband frequency  
 $t_{\text{ant}}$  = antenna noise ratio

$$\text{and, } P_{\text{out}} = \frac{1}{216} \frac{f_p}{f_c} P_{\text{norm}}, f_p = f_u - f_s$$

Experimental Amplifier:  $f_s = 3.5 \text{ MC}$ ,  $f_c = 1.2 \text{ GC}$ ,  $f_u = 29.5 \text{ MC}$ ,  $P_{\text{norm}} = 40 \text{ KW}$ ,  $B = 1 \text{ KC}$ ,  $t_{\text{ant}} = 1$ .  $P_{\text{out}} = 4.5 \text{ W PRED, } 5 \text{ W MEAS}$ ;  $DR = 159 \text{ db PRED, } > 150 \text{ db MEAS}$ .

Figure 8—Dynamic range and maximum power output for a high-power upper-sideband upconverter. These results hold for operating frequencies much less than the cutoff frequency. An experimental example is also illustrated.

## SESSION II: Microwave Parametric Circuits

## WM 2.3: Design Techniques for Broadband, Nondegenerate Parametric Amplifiers

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SINCE THE DEVELOPMENT of the first relatively narrow-band parametric amplifiers, a number of investigators<sup>1,2</sup> have suggested how multituning could improve bandwidth; these techniques have been demonstrated to be particularly successful in degenerate parametric amplifier design<sup>3,4</sup>.

This paper will describe a technique for increasing the bandwidth of nondegenerate parametric amplifiers. It differs from other design techniques in that the emphasis is placed on designing around the parameters of the varactor diode to obtain a flat or multiresonant net signal and idler susceptance response; not, as is the usual method, in resonating the diode in the signal and idler cavities and then employing multituning techniques. Using this approach, single-diode nondegenerate amplifiers from S through X band, that have bandwidths of 10% or more at 10 to 13-db gain, have been constructed.

For optimum noise-figure performance (*opt nf*)<sup>5</sup>, the diode should have as large a figure of merit ( $\gamma Q$ ) as possible, and its idler-to-signal-frequency ratio should be

$$\text{that given by } \frac{\omega_2}{\omega_1 \text{ opt } nf} = \frac{\gamma^2 Q^2}{1 + \sqrt{1 + \gamma^2 Q^2}}; \quad (1)$$

where  $\gamma = \frac{C_1}{2C_0}$  = diode nonlinearity ratio,

and  $Q = \text{diode } Q \text{ at signal frequency} = \frac{1}{\omega_1 C_0 r_s}$ ;

in which  $r_s$  is the diode series resistance and  $C_0$  the operating point junction capacitance. This idler-to-signal-frequency relationship for optimum noise figure is nearly compatible with that for wide bandwidth, as can be seen by comparing equation 1 with

$$\frac{\omega_2}{\omega_1 \text{ opt bandwidth}} \approx \left[ \gamma^2 Q^2 \right]^{1/3}. \quad (2)$$

<sup>1</sup> Seidel, H. and Herman, G. F., "Circuit Aspects of Parametric Amplifiers," *IRE WESCON Convention Record*, Part 2, p. 83-90; 1959.

<sup>2</sup> Matthaei, G. L., "A Study of the Optimum Design of Wideband Parametric Amplifiers and Upconverters," *PGMTT Conference*; 1960.

<sup>3</sup> Little, A. G., "A Wide-Band Single-Diode Parametric Amplifier Using Filter Techniques," *Proc. IRE*, p. 821-822; April, 1961.

<sup>4</sup> Gilden, M., and Matthaei, G. L., "A Nearly Optimum Wide-Band Degenerate Parametric Amplifier," *Proc. IRE*, p. 833-834; April, 1961.

<sup>5</sup> Kotzebue, K. L., "Optimum Noise Performance of Parametric Amplifiers," *Proc. IRE*, p. 1324-1325; July, 1960.

In addition, for wide bandwidths it is desirable to have  $\gamma$  as large as possible for a given  $\gamma Q$  product.

A number of possible circuits were analyzed. It was found that the broadest bandwidths came from those circuits whose idler frequency approximately equaled the diode self-resonant frequency, and also approximately satisfied equation 2. Of the circuits considered, the one with the best performance is shown in Figure 1. When using a diode with a case capacitance that is not negligible,  $L'$  and  $C'$  can often be chosen to provide a double-tuned signal response and a single-tuned idler response. When case capacitance is small compared to junction capacitance,  $L'$  and  $C'$  can be chosen to provide a single-tuned signal response and a double-tuned idler response. To show how a net triple-tuned response can be achieved in the latter case, the susceptance contributions of the signal and transformed idlers are illustrated in Figure 2.

Figure 3 shows a typical nondegenerate amplifier. In a cross section of that amplifier (Figure 4)  $Z_{01}$ , a length of low-impedance transmission line, corresponds to  $C'$  of Figure 1 and  $Z_{02}$ , a high-impedance line, corresponds to  $L'$ . When looking from the amplifier input terminals toward the generator, it is necessary to see a flat impedance over the operating range. Thus, a broadband, low *vswr* circulator and a low *vswr* filter network (B in Figure 2) should be used. On the other hand, reactive discontinuities appropriately placed on the transmission line can provide a flatter susceptance response around the signal resonance and thus improve the bandwidth. This approach is essentially the same as that described by Matthaei for multituning<sup>2</sup>.

Using the design techniques described, several parametric amplifiers have been constructed and evaluated. Some of the characteristics of these amplifiers are presented in Figures 5, 6, and 7.

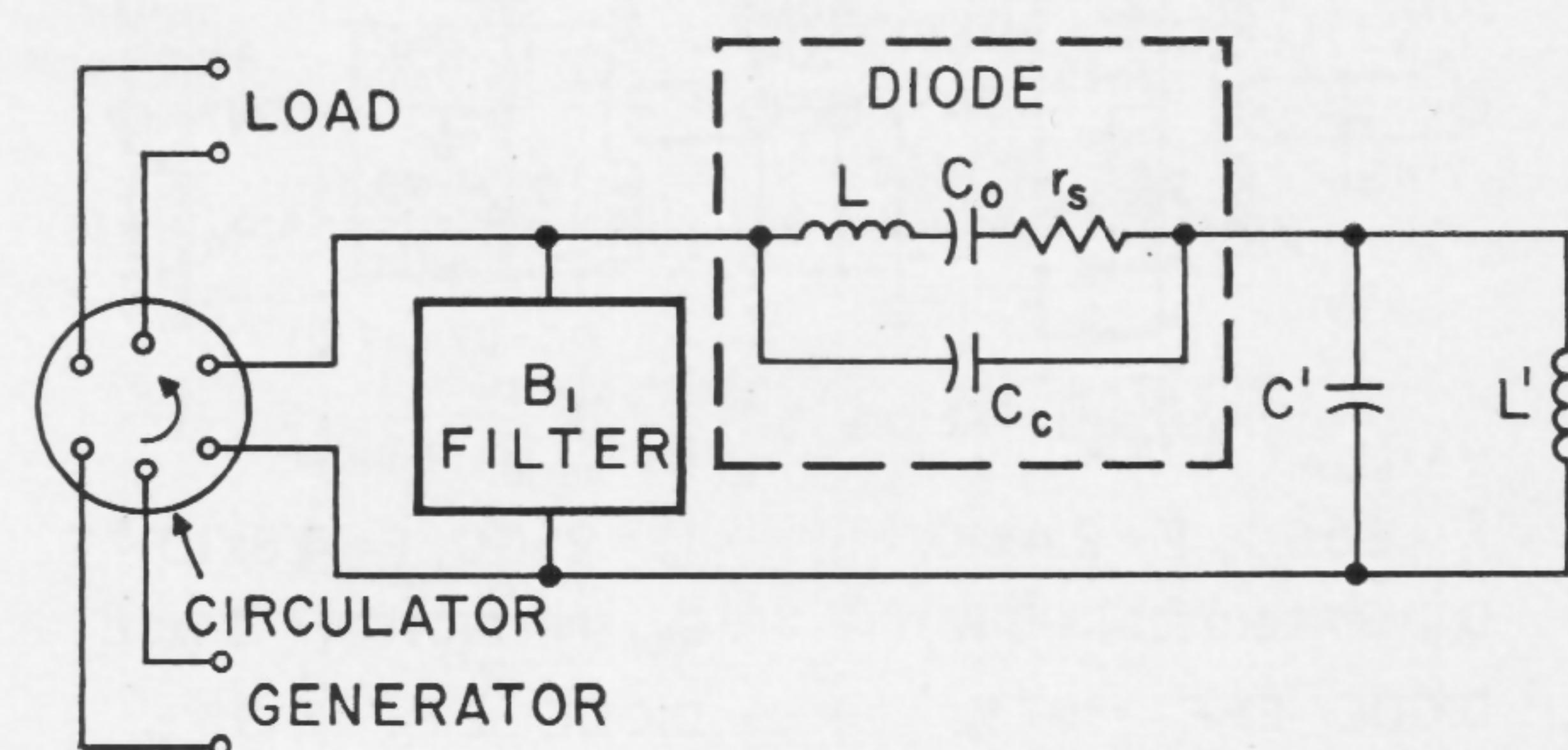


Figure 1—Parametric amplifier equivalent circuit.

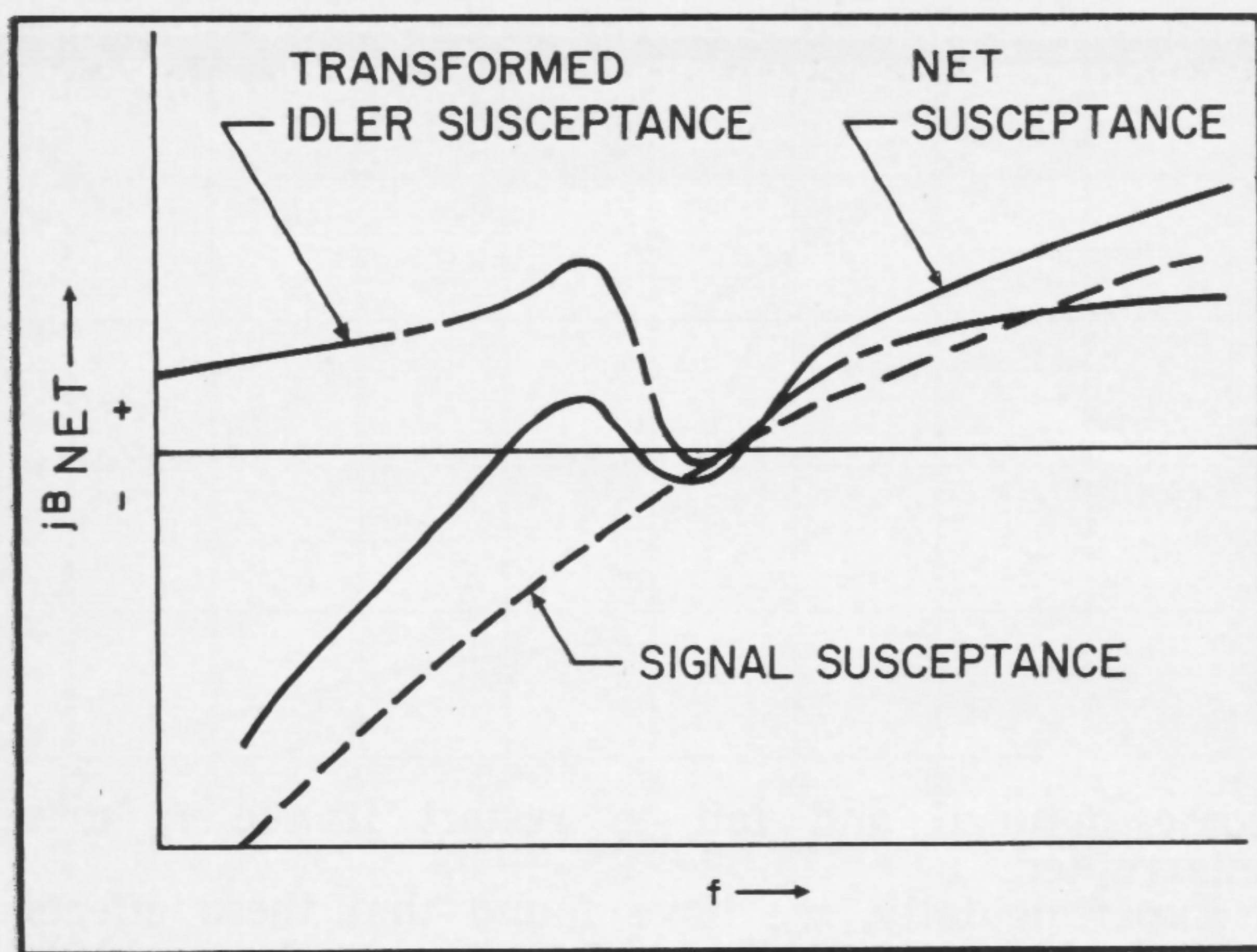


Figure 2—Typical net susceptance about the signal frequency.



Figure 3—Parametric amplifier.

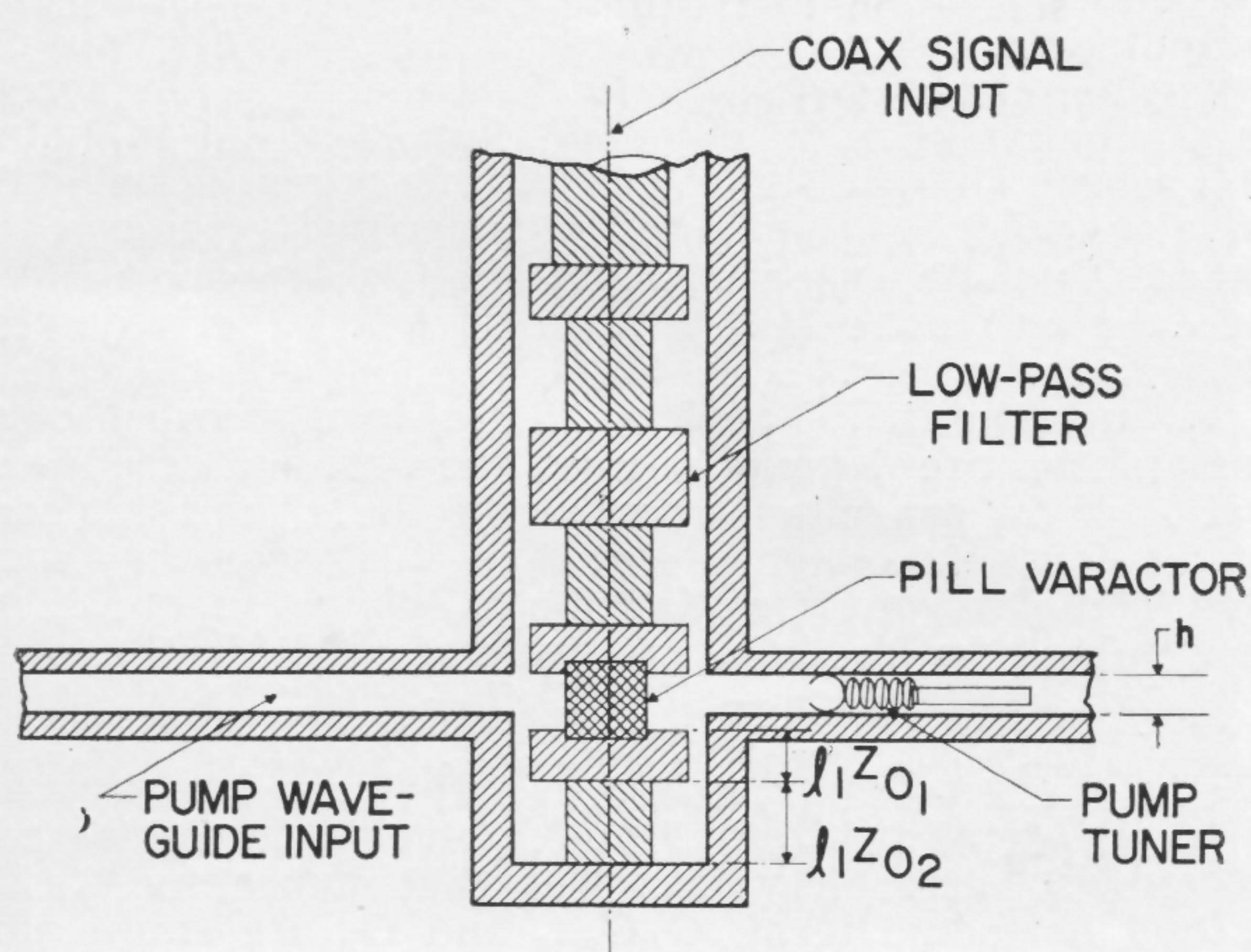


Figure 4—Cross section of parametric amplifier shown in Figure 3.

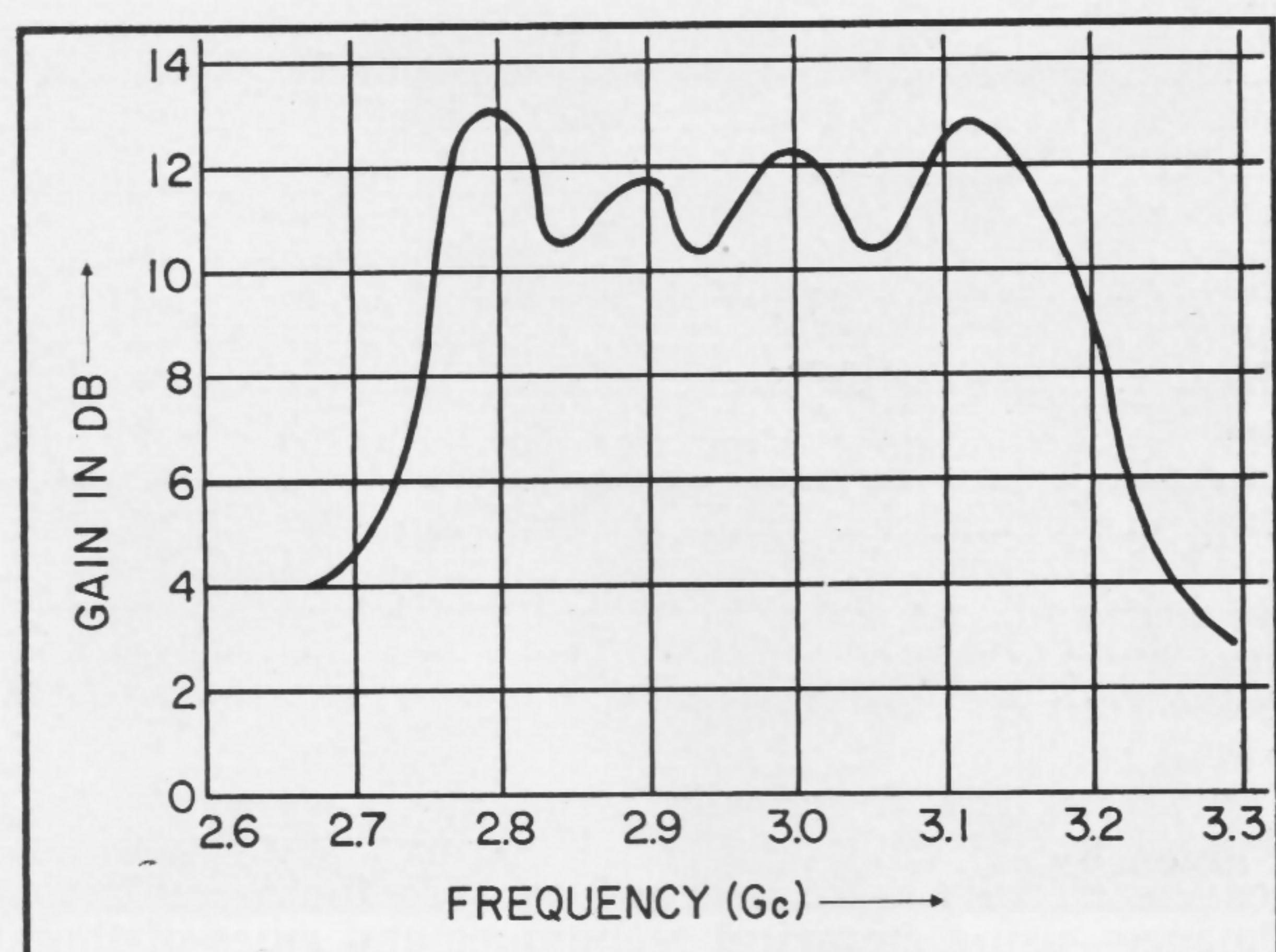


Figure 5—Plot of amplifier with a 13-db gain; 425-Mc b-w.  $NF = 2.1$  db (amp alone),  $G^{1/2} B = 1900$  Mc,  $\%G^{1/2} B = 64\%$ .

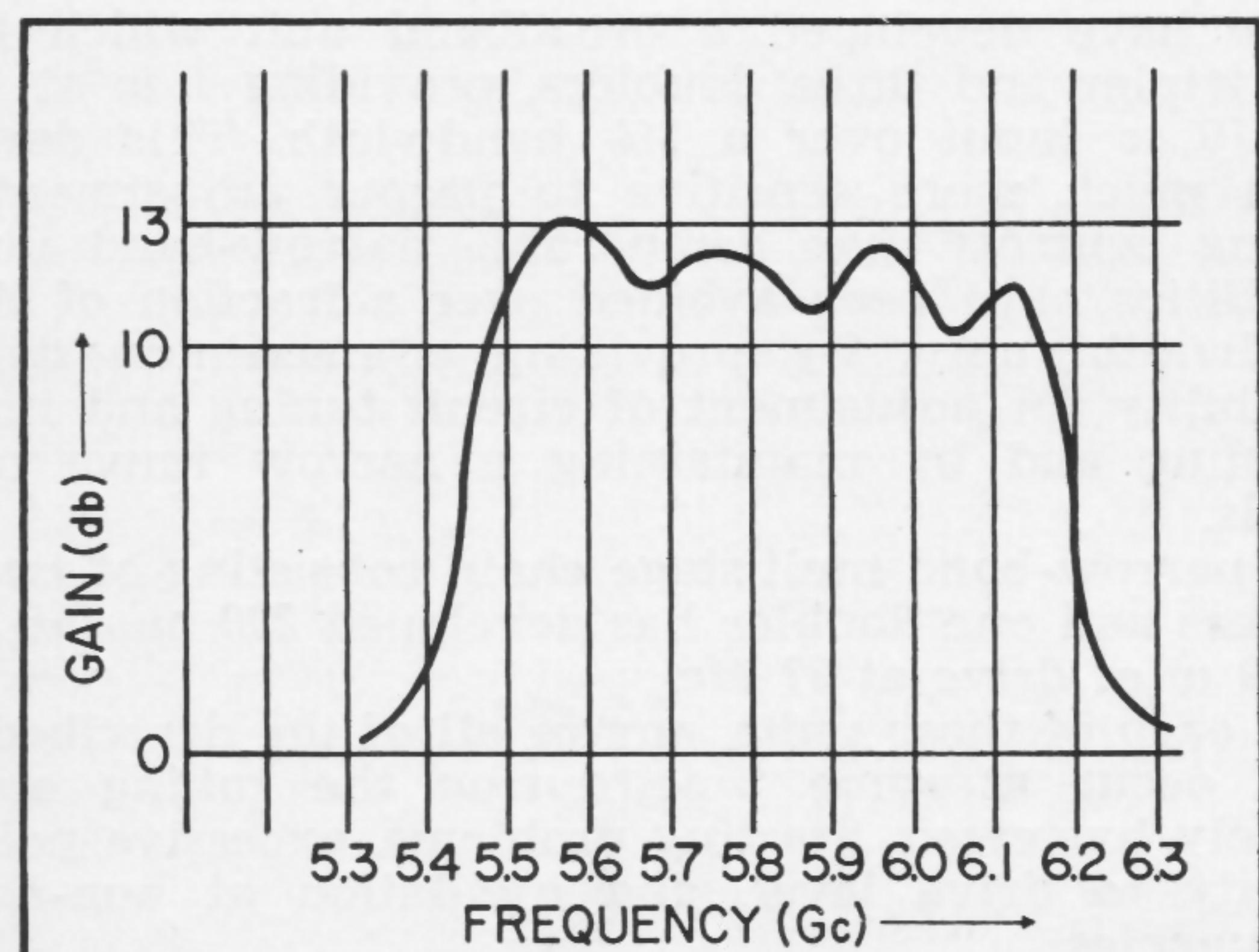


Figure 6—Plot of another type of amplifier with a 13-db gain; 700-Mc b-w.  $NF = 2.4$  db (amp alone),  $G^{1/2} B = 3130$  Mc,  $\%G^{1/2} B = 54\%$ .

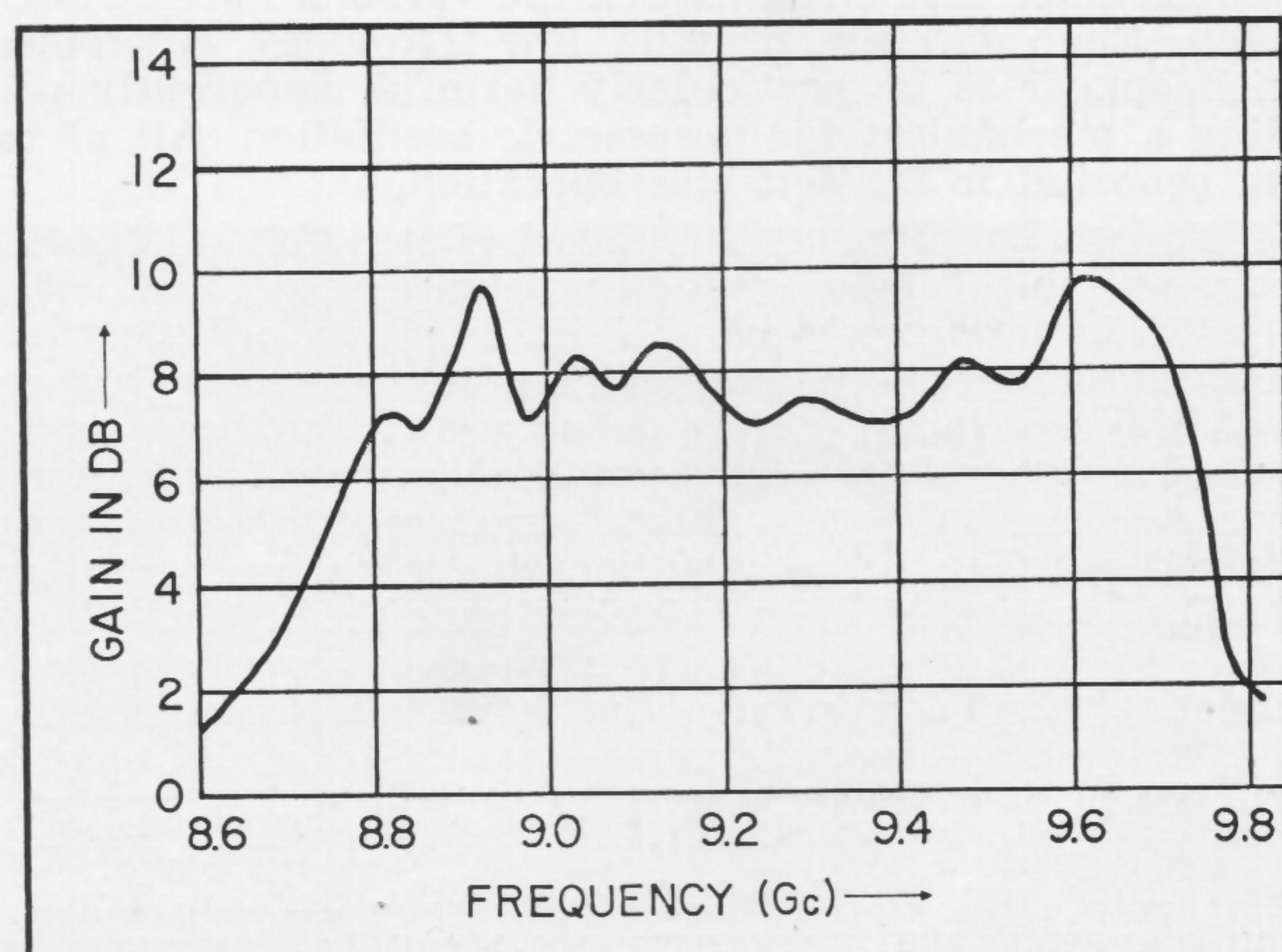


Figure 7—Characteristics of a third type amplifier: 10-db gain; 900-Mc b-w.  $NF = 3.2$  db (amp alone),  $G^{1/2} B = 2930$  Mc,  $\%G^{1/2} B = 31.5\%$ .

## SESSION II: Microwave Parametric Circuits

## WM 2.4: Special Problems in Microwave Harmonic Generator Chains

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THIS PAPER WILL DESCRIBE experimental work with single and multiple-stage varactor harmonic generators that can be used to provide useful power at *uhf* and microwave frequencies beyond the capabilities of transistor operation. These devices use the nonlinear charge-verses-voltage characteristic of the varactor diode. When operated at an average reverse bias, the diode generates harmonics when strongly driven by an *ac* wave. With high-*Q* varactors, the nonlinearity is largely reactive rather than resistive, allowing high efficiency in frequency conversion to integral harmonic frequencies.

Several special problems have been encountered and this paper will offer, in the main, a description of observed behavior. Because of the essential nonlinearity, and because we are dealing with strong signals at two or more frequencies, the devices cannot be readily analyzed in terms of instabilities with respect to other frequencies, including *dc* bias. Various types of instabilities have been observed, and some have been reported in the literature<sup>1,2,3</sup>. These include parametric oscillations, hysteresis and multiple-level problems, starting difficulties, bias oscillations, and high level noise. As a general problem the situation is very complex. Practically speaking, however, we have been successful in obtaining stable, reliable, operation—once the circuits are tuned and coupled for optimum performance—using empirical techniques and rules-of-thumb.

It is hoped that this paper will encourage theorists to study these problems in greater depth than has been done to date.

It has been our experience that self-bias is satisfactory. This is done by leaving the varactors open circuited at *dc*. Alternatively, we have shunted the varactor with a large resistor on the order of 10,000 ohms or more, or biased the varactor through such a resistor. We have been notably unsuccessful in obtaining stable operation using low-resistance bias circuit when the varactors are strongly driven. Such circuits provide low-frequency resonances which appear to be particularly harmful, apparently providing a mechanism for parametric oscillation. All of the data reported is for self-bias operation.

Hysteresis is often observed when varying either the frequency or the driving power, as shown in the illustrations. Under some fixed conditions, one, two, or even three operating modes are possible, depending upon past history. Discontinuous mode jumps occur when the level is increased or decreased, or when the driving frequency is increased or decreased. Such jumps occur at different levels depending upon whether the variation is in one direction or the other, producing an effect resembling a hysteresis loop when varying through a complete cycle. This effect has been found to be due to *dynamic detuning*, an effect which depends upon the variation of average capacitance of a varactor with *rf* voltage<sup>2,4</sup>. Under strong *rf* voltage drive, a varactor circuit will have different resonant frequency than when weakly driven. Thus, a circuit once started may resonate strongly, but may be-

come detuned and fail to restart if the *rf* drive is interrupted.

Experimentally, we have found that these effects can be minimized by proper circuit tuning. In doublers and triplers, it has been found that a proper *loading* exists at the input and at the harmonic output, and we also have a proper *tuning* for each resonance providing smooth swept-frequency responses over wide ranges of input drive. These conditions have been determined experimentally.

At least two modes of parametric oscillations have been observed; in one case, two simultaneous oscillating frequencies whose sum is equal to the driving frequency. Such effects cause a loss in output power at the desired frequency and are often accompanied by noisiness in the output. We believe that these effects most often occur when the circuit includes a low-frequency resonance. This is particularly likely when a long line is used between the source and the first stage. Another type is believed to involve second harmonic variations in the varactor capacitance. This can cause an instability in the drive level or produce two oscillating frequencies on either side of the driving frequency.

In an unpublished analysis it has been shown that such instabilities are dependent upon the first and second-order variation in capacitance and upon the circuit impedance at the driving frequency. Based on this theory, we suspect that stability requires that the following inequalities be maintained for the two respective cases:

$$\omega_s \omega_p - s^2 C_1^2 < G_s G_{p-s}$$

$$\omega_p E_2 < G_p$$

where the subscript *s* refers to a spurious low frequency, *p* to the drive frequency, and *p-s* to their difference. *C*<sub>1</sub> is the first harmonic variation in capacitance and *C*<sub>2</sub> is the second harmonic term; *G*<sub>*s*</sub>, *G*<sub>*p-s*</sub> and *G*<sub>*p*</sub> are shunt admittances at these frequencies. The avoidance of such oscillations depends upon our ability to load the circuit at the input and output to a sufficient degree to provide stability against such effects. Experimentally, this has generally been possible.

As many as seven doubler stages have been coupled in tandem providing 200 *mw* at 8.2 *kMc* for an input of 12 *w* at 64 *Mc*. If the drive level is decreased by about 3 *db*, instabilities, which appear to be parametric oscillations, occur with an accompanying spectral breakup. The oscillation appears as a kind of *relaxation oscillation* with the generation of a saw-tooth variation in the output wave at frequencies on the order of 100 *kc*.

We have developed a broadband unit which includes one tripler and three doublers, providing 1 *w* at 1000 *Mc* for 10 *w* input over a 7% bandwidth. This device has been much more sensitive to proper adjustment of all tuning controls than comparable narrow-band units. Instabilities have been avoided over a fraction of the total bandwidth, only, by providing a maximum degree of flexibility for adjustment of circuit tuning and interstage coupling and by maintaining a narrow range of drive levels.

A narrow-band multistage chain consisting of two quadruplers and one doubler has developed 200 *mw* at 1184 *Mc* for 3 *w* of drive at 37 *Mc*.

In each of these units, any or all of the described effects may occur at some time during the tuning operation, namely hysteresis, starting problems, excessive noise, sensitivity to drive level, and oscillation at non-harmonic frequencies.

It has been found it necessary to tune each stage in turn before proceeding to the next. It is helpful and often surprising to use a swept-frequency source and monitor the output with a video-detector and a broadband oscilloscope.

<sup>1</sup> McDode, J. C., *Proc. IRE*, p. 957-958; May, 1961.<sup>2</sup> McDode, J. C., *Proc. IRE*, p. 91-92; Jan., 1962.<sup>3</sup> Seigel, K., *Proc. IRE*, p. 1159-1160; June 1960.<sup>4</sup> Hines, M. E., *NEREM Record*, Vol. 3, p. 142-143; Nov., 1961.

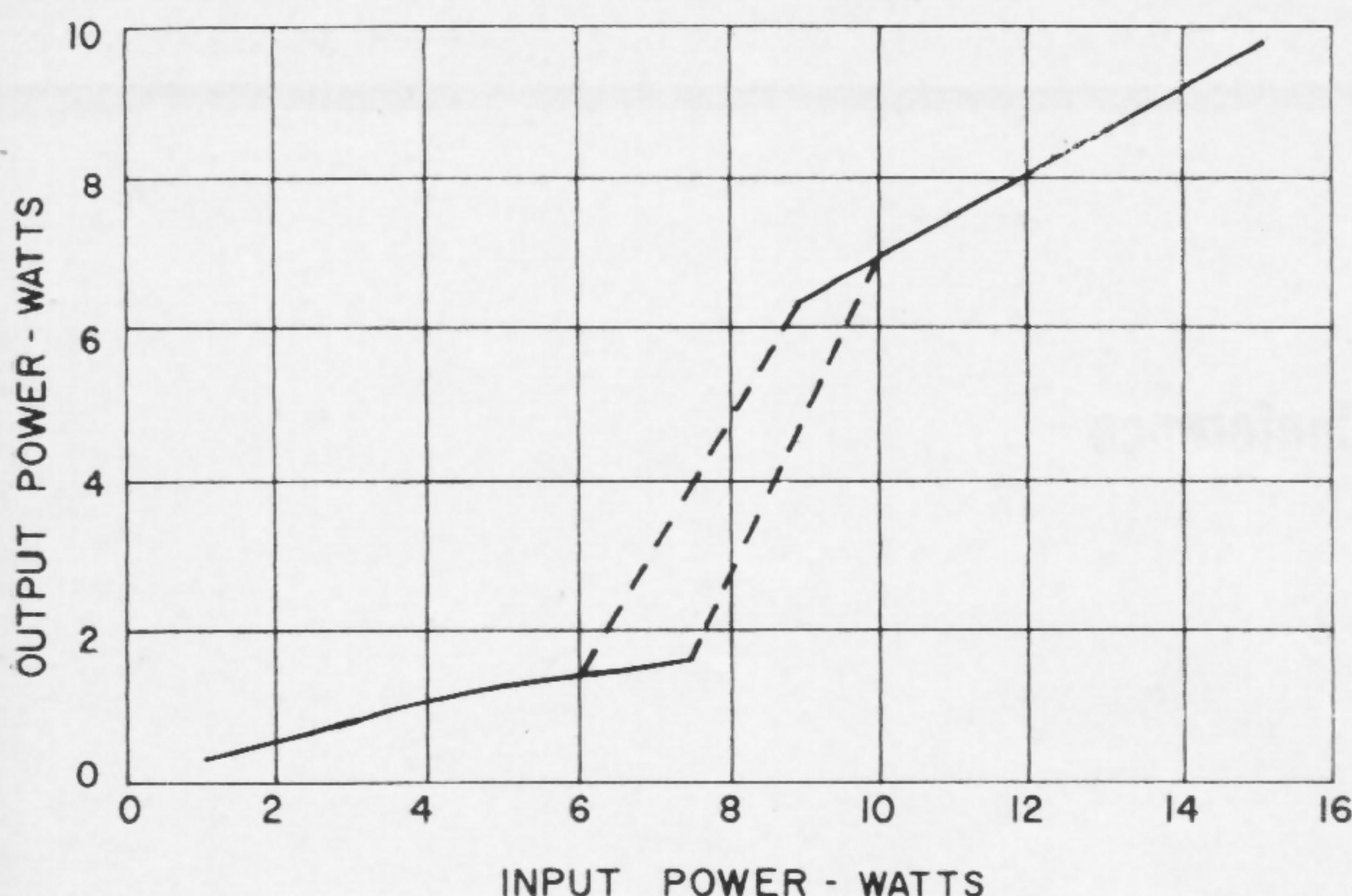


Figure 1—Hysteresis as a function of input driving power. The dotted lines are discontinuous jumps. The input drive jumped also because of simultaneous change in the input standing-wave ratio.

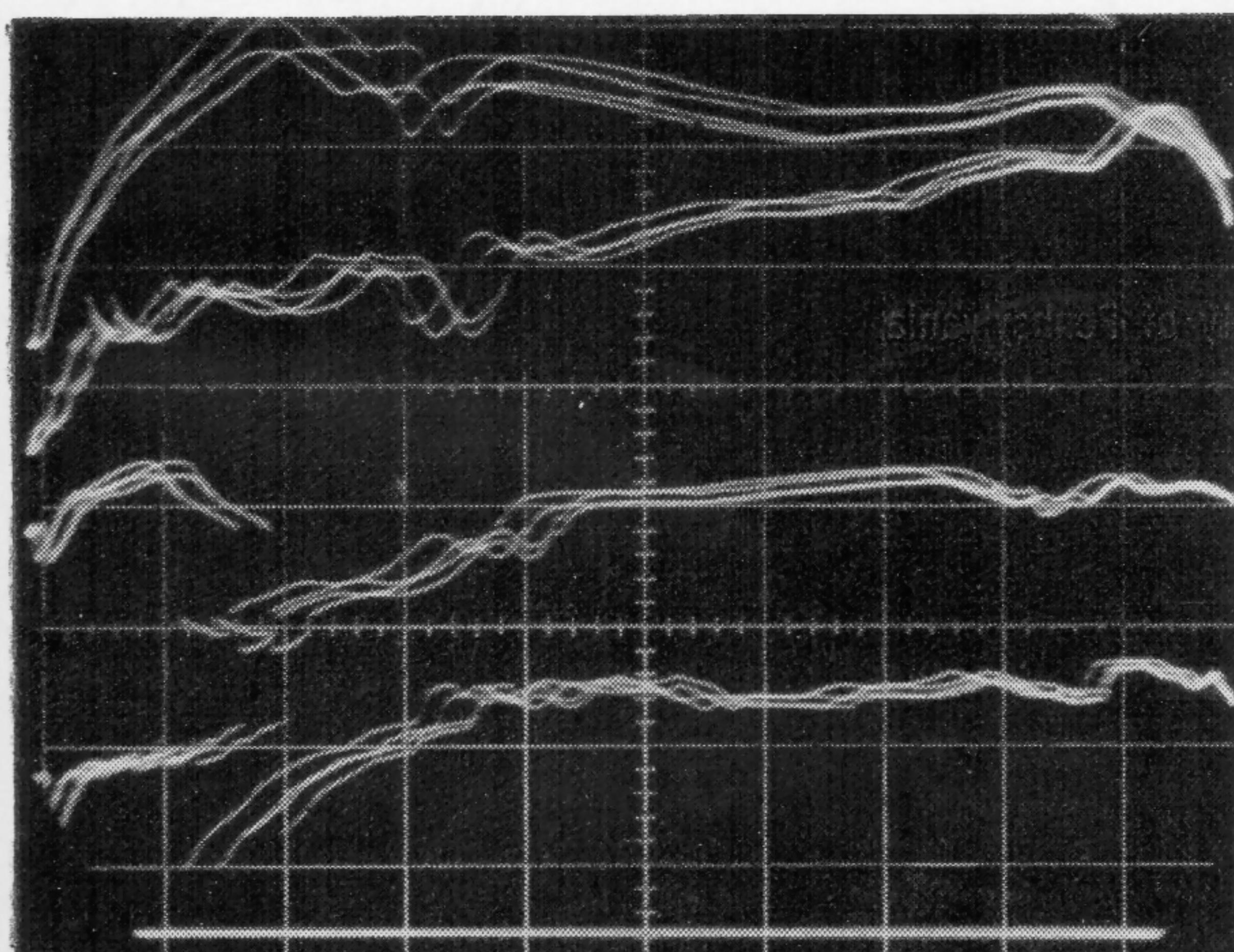


Figure 2—Swept-frequency response at various stages in a  $3 \times 2 \times 2 \times 2$  broadband chain which accepts 10 w at 40 Mc and provides 1.5 w at 960 Mc. (Four traces are shown for each level because of the motor-driven sweeper used.) The upper trace is the tripler output at 120 Mc, the next three are at 240, 480, and 960 Mc, respectively. The flat line at the bottom is zero output. The input frequency varies from 36.6 Mc at the left to 45.5 Mc at the right, approximately 25% bandwidth.

(Right)

Figure 5—Spectrum-analyzer response of a  $\times 24$  multiplier when underdriven (top), normally driven (center), and overdriven (bottom). The second response in the center trace arises in the spectrum analyzer and is not generated by the multiplier.

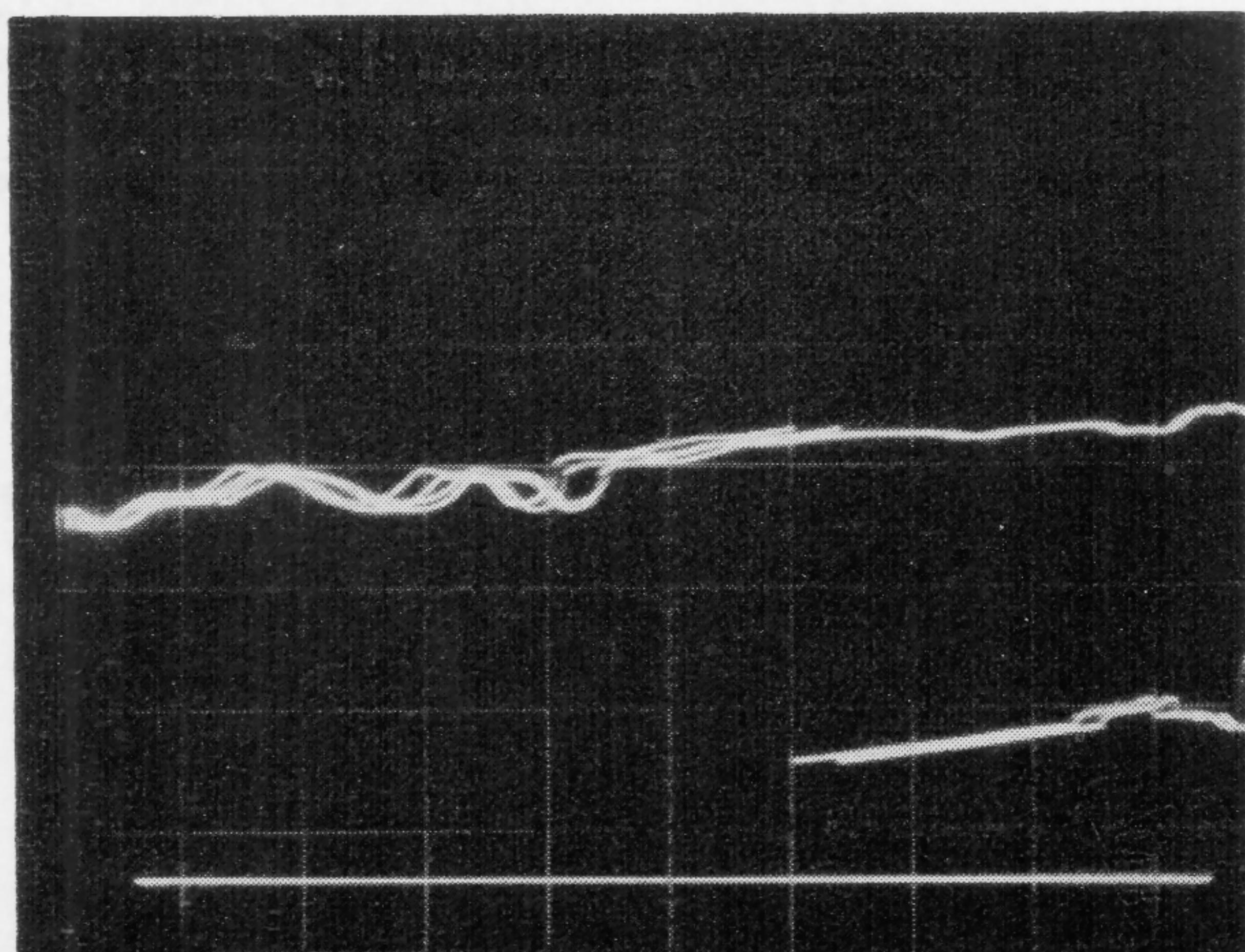


Figure 3—Simple frequency-sweep hysteresis in the broadband multiplier stage two under reduced input drive. In the right hand half of the sweep, two levels are found, one for each sweep direction.

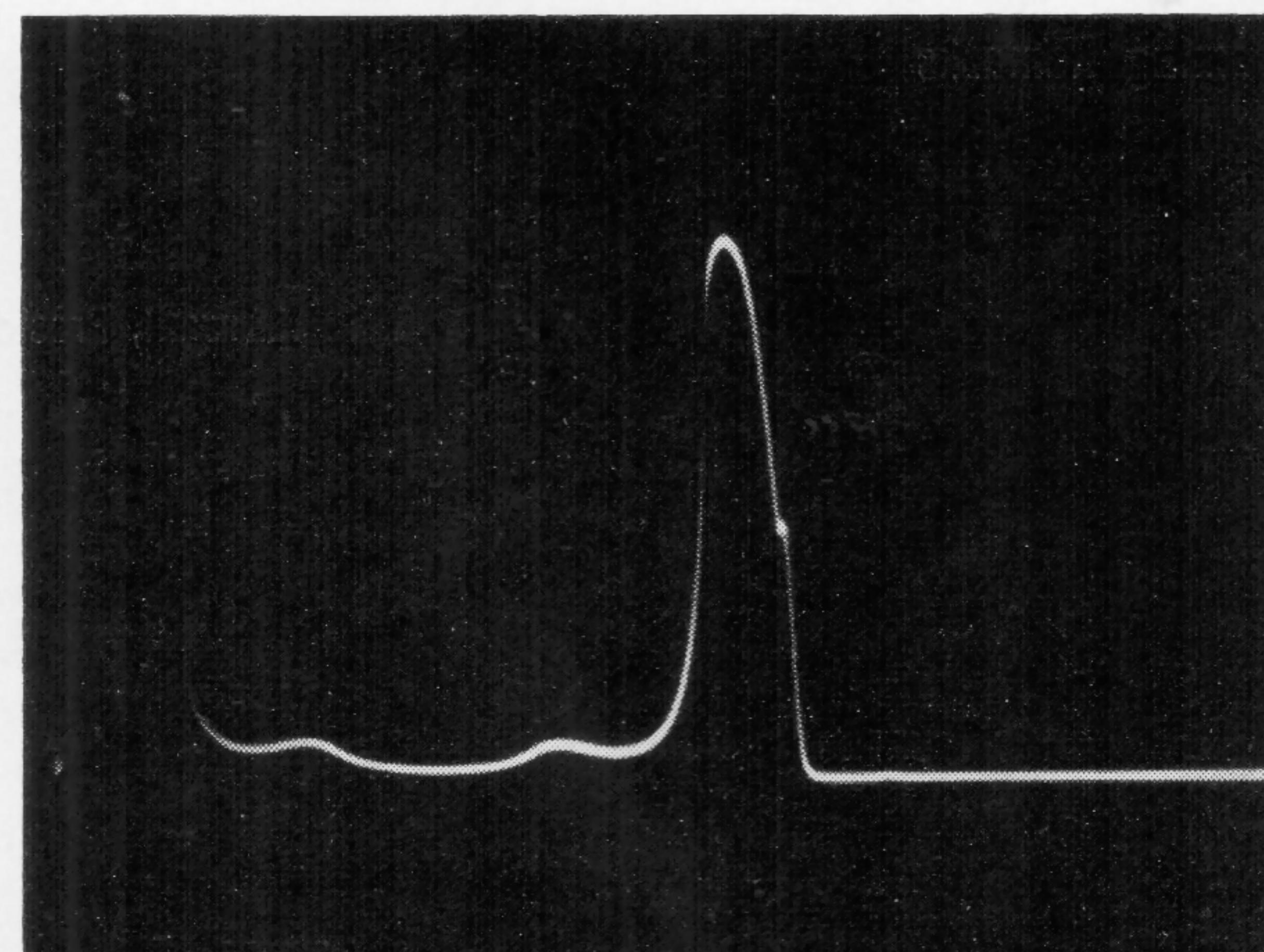
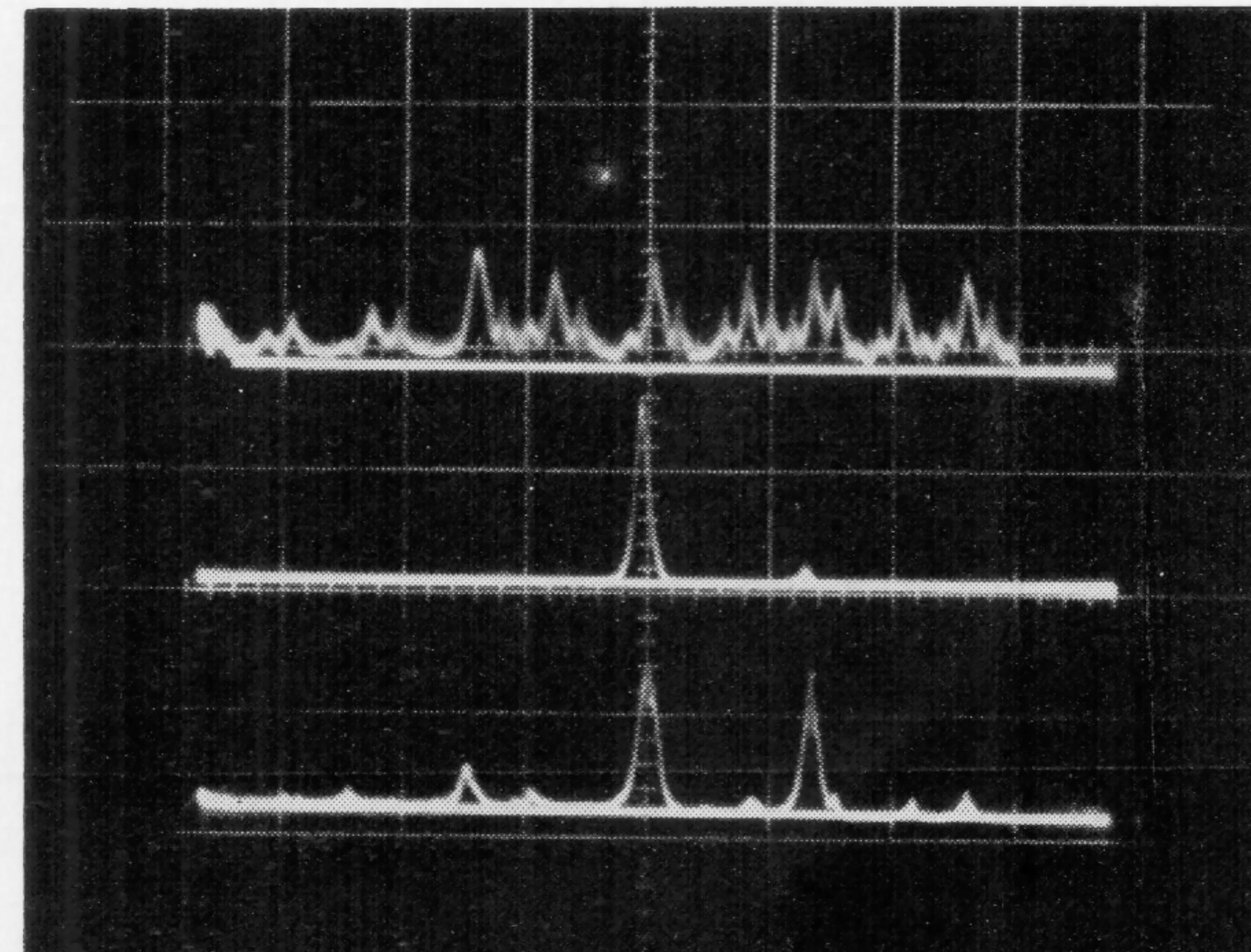


Figure 4—Swept-frequency response of a narrow-band (1%) unit,  $4 \times 4 \times 2$ , from 3 w at 37 Mc to .2 w at 1184 Mc. This shows the clean response obtained with proper tuning.



### Formal Opening of Conference

#### Introductory Comments

Chairman of Conference—**J. J. Suran**, Electronics Laboratory, General Electric Company

#### Welcoming Remarks

**G. P. Harnwell**, President, University of Pennsylvania

#### 1961 Conference Awards

Chairman, 1961 Conference—**T. R. Finch**, Bell Telephone Laboratories, Inc.

#### Invited Address

**P. Aigrain**, Director of Defense Research for France and Professor of Physics, University of Paris

#### The Principles and the Promise of Active Homogeneous Semiconductor Devices

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The Conference gratefully acknowledges assistance received from the Office of Naval Research



## SESSION III: New Devices and Device Characterization

Chairman: S. K. Ghandhi

Philco Research Division, Blue Bell, Pa.

## WA 3.1: Generalized Gain and Speed Limitations of Linear Amplifiers\*

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Research Laboratory of Electronics, MIT  
Cambridge, Mass.

ON THE SINGLE CONSERVATION law<sup>1</sup>, often called *Tellegen's Theorem*, noted below, one can find a basis for network composition and prophesies of performance.

$$\sum v_b(t_1) \cdot i_b(t_2) = 0 \quad (1)$$

This law is a direct consequence of *Kirchhoff's Laws*, but it can also be derived by assuming only (1) the conservation of energy law and (2) the insensitivity of the conservation law to the variation of independent variables. For the field theory analog of equation 1 we note that the integral overall space of  $\bar{P}(t_1) \cdot \bar{Q}(t_2)$  is zero if  $\operatorname{div} \bar{P} = 0$  and  $\operatorname{curl} \bar{Q} = 0$ . The summation in equation 1 is over all branches of a self-contained circuit and for  $t_1 = t_2$  this basic theorem expresses conservation of instantaneous power. Generally, however,  $t_1$  and  $t_2$  are independent variables, and thus we can derive the transformed, special

case  $\sum V_b(s^*) \cdot I_b(s) = 0 \quad (2)$

Equation 2 expresses conservation of complex power for complex frequencies. The interpretation of the consequences of this equation will be the subject of this paper. It should be pointed out that the conservation-of-power approach does not lead to a single, simple figure of merit. Rather, it leads to a criterion about whether a desired network is compatible with the available circuit components. It enables us to predict the maximum possible gain that is commensurate with the desired transient response.

Since *complex* power is conserved, the total complex power absorbed by a network must equal the sum of complex powers absorbed by the individual circuit components. Thus, if the circuit components have restrictions on the power that they can absorb, then the overall network *may* also have restrictions. For linear circuits, the restrictions on the angle of the *complex power* for *complex frequencies* determines important speed limitations.

## Criteria for RLC Conditions

The total *complex* power absorbed by a network constructed from one-port components is the sum of the powers absorbed by the individual one-ports. For example, the complex power absorbed by an *RLC* network at a frequency  $s$  is  $P = P_R + P_C \exp(s/|s|) + P_L \exp(s^*/|s|)$  where  $P_R$ ,  $P_L$ , and  $P_C$  are positive real for  $s = \sigma + j\omega$ . For  $\sigma < 0$  there are positive real values of  $P_R$ ,  $P_C$ , and  $P_L$  that will produce an arbitrary  $P$ . However, for  $\sigma \geq 0$  we find

\* This work was supported in part by the U. S. Army Signal Corps, the Air Force Office of Scientific Research, and the Office of Naval Research.

<sup>1</sup> Tellegen, B. D. H., "A Network Theorem With Applications," *Phillips Research Report*, 7; 1952.

<sup>2</sup> See, for example, Stratton, J. A., "Electromagnetic Theory," *McGraw-Hill Book Company*, p. 111; 1941.

<sup>3</sup> For other examples see the author's paper, "Active RC Networks," *IRE PGCT*; Sept., 1957.

definite restrictions on  $P$  given by  $/s \geq /P \geq /s^*$ . Thus for *RLC* circuits the *s*-plane region of unrestricted power angle is the left half-plane. These criteria can be used to derive virtually all *RLC* realizability conditions.

For networks containing active components the power-angle restrictions are usually more difficult to determine and the *s*-plane region of unrestricted power includes at least part of the right half-plane. For example, a circuit containing tunnel diodes, inductors, capacitors, gyrators, and resistors has power-angle limitations as shown in Figure 1.

For a two-port, the power-angle restriction can be determined by an elementary but tedious derivation; the results are given in Figure 2. (The expressions in this figure have inherent ambiguities that must be resolved as follows:  $\beta_a$  lies within the acute angle bounded by

$\angle h_{11}$  and  $\angle h_{22}$ \* and  $0 \leq \beta_d \leq \pi/2$ ). For practical circuits the active two-port is combined with *RLC* circuits and typical examples<sup>2</sup> of power-angle restrictions for active device + *RLC* circuits are given in Figures 3 and 4. Although the complete specification of power limitations is likely to be quite complicated, the parameters  $\sigma_o$  and  $\omega_o$  indicated in Figures 1, 3, and 4 offer convenient figures of merit for device characterization. These parameters determine the penetration of the region of unrestricted power into the right half-plane.

The practical importance of determining the region of unrestricted power is best illustrated by simple examples. Figure 5 shows the power limitations for a two-port that is, in essence, a unilateral, single-time-constant amplifier. If this amplifier is to be constructed by interconnecting various circuit components, then clearly the amplifier cannot be expected to absorb power that cannot, in turn, be absorbed by the components. Thus the shaded region in Figure 5 must lie within the shaded region of the appropriate figure (Figures 1, 3, or 4) and we must at least satisfy the limitations

$$(k-1) \omega \leq \sigma_o; (k^2-1) \omega^2 \leq \omega_o^2 \quad (3)$$

with  $\sigma_o$  and  $\omega_o$  determined from the component characteristics. For high gains, equation 3 reduces to the familiar gain-bandwidth-product limitation.

As a second example, Figure 6 shows the region of unrestricted power for an all-pass, unilateral amplifier with delay  $\tau$ . Applying the same arguments as in the first example, we find that

$$(In k) / \tau \leq \sigma_o \quad (4)$$

The interpretation of equation 4 is easily understood in terms of the cascading of amplifier stages; to double the *db* of gain, we must double the delay. Cascading can increase the gain-bandwidth product, but only at the cost of increasing the phase shift.

A more detailed study shows that useful power gain is only possible at complex frequencies for which the power angle is unrestricted. For frequencies within the unrestricted region the power gain can be varied at will, provided that the power gain drops below unity outside of this region.

$$\beta_a + \beta_d \geq \text{POWER} \geq \beta_a - \beta_d$$

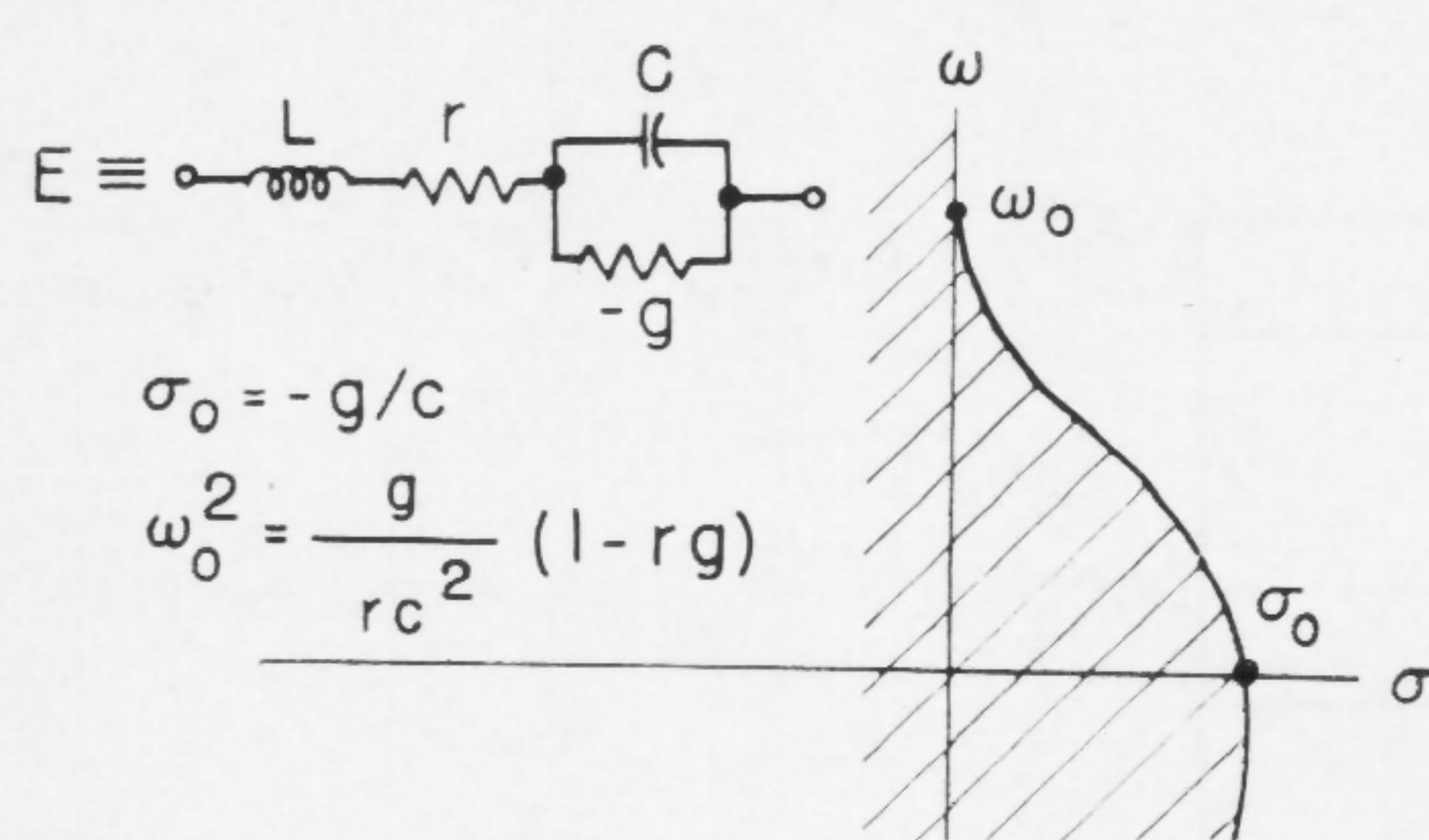


Figure 1—Region of unrestricted power for  $E+G+L+R+C$  circuits.

$$2\beta_d = \angle h_{11}^* + \angle h_{22} = \angle y_{11} y_{22} - y_{12} y_{21}$$

$$\cos 2\beta_d = \frac{2 \operatorname{Re} [h_{11} h_{22}] - |h_{12}^* + h_{21}|^2}{2 |h_{11} h_{22}|}$$

$$= \frac{2 \operatorname{Re} [y_{11}^* y_{22}] - |y_{12}|^2 - |y_{21}|^2}{2 |y_{11} y_{22} - y_{12} y_{21}|}$$

Figure 2—Allowed power angles for a two-port.

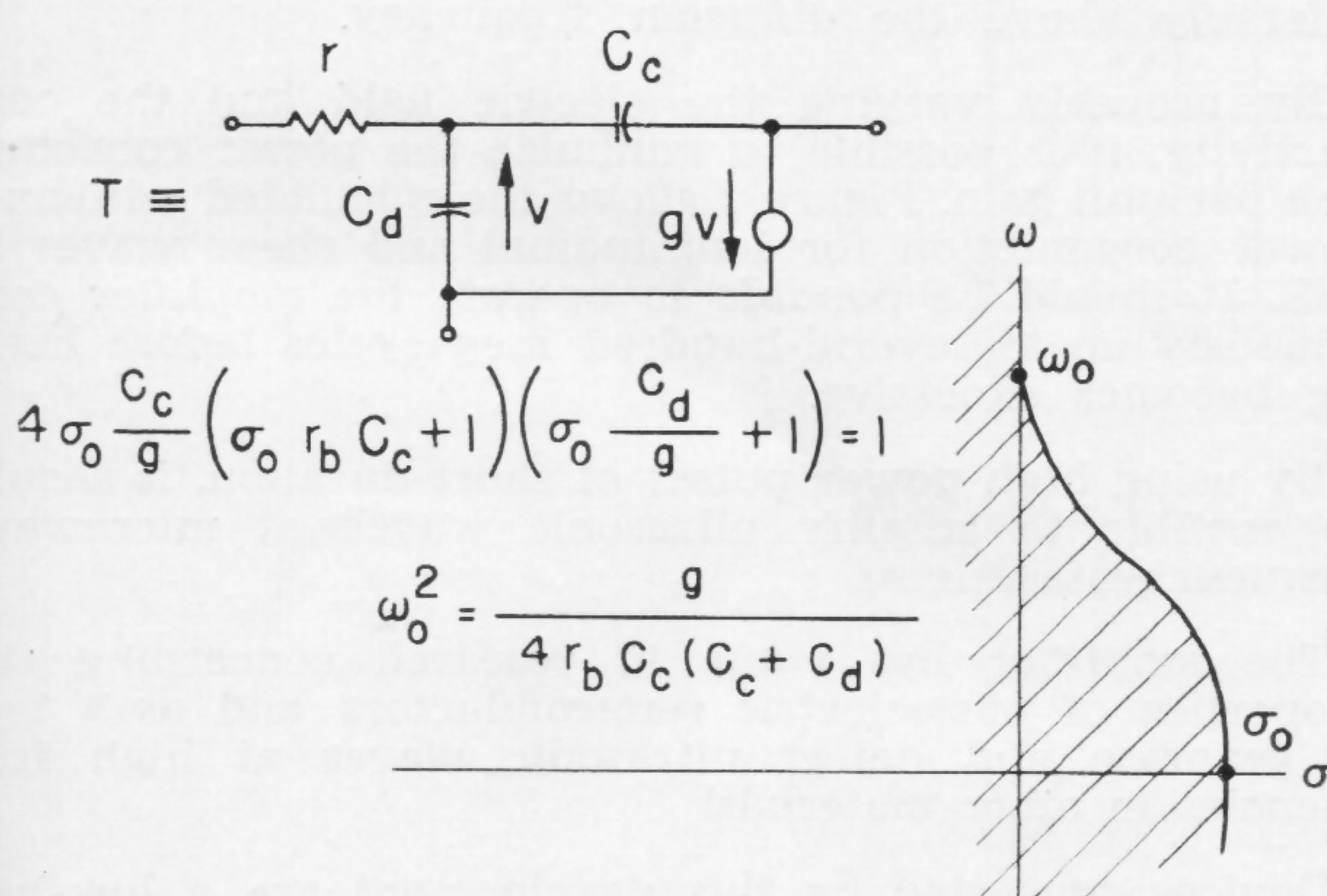


Figure 3—Region of unrestricted power for  $T+L+R+C$  circuits.

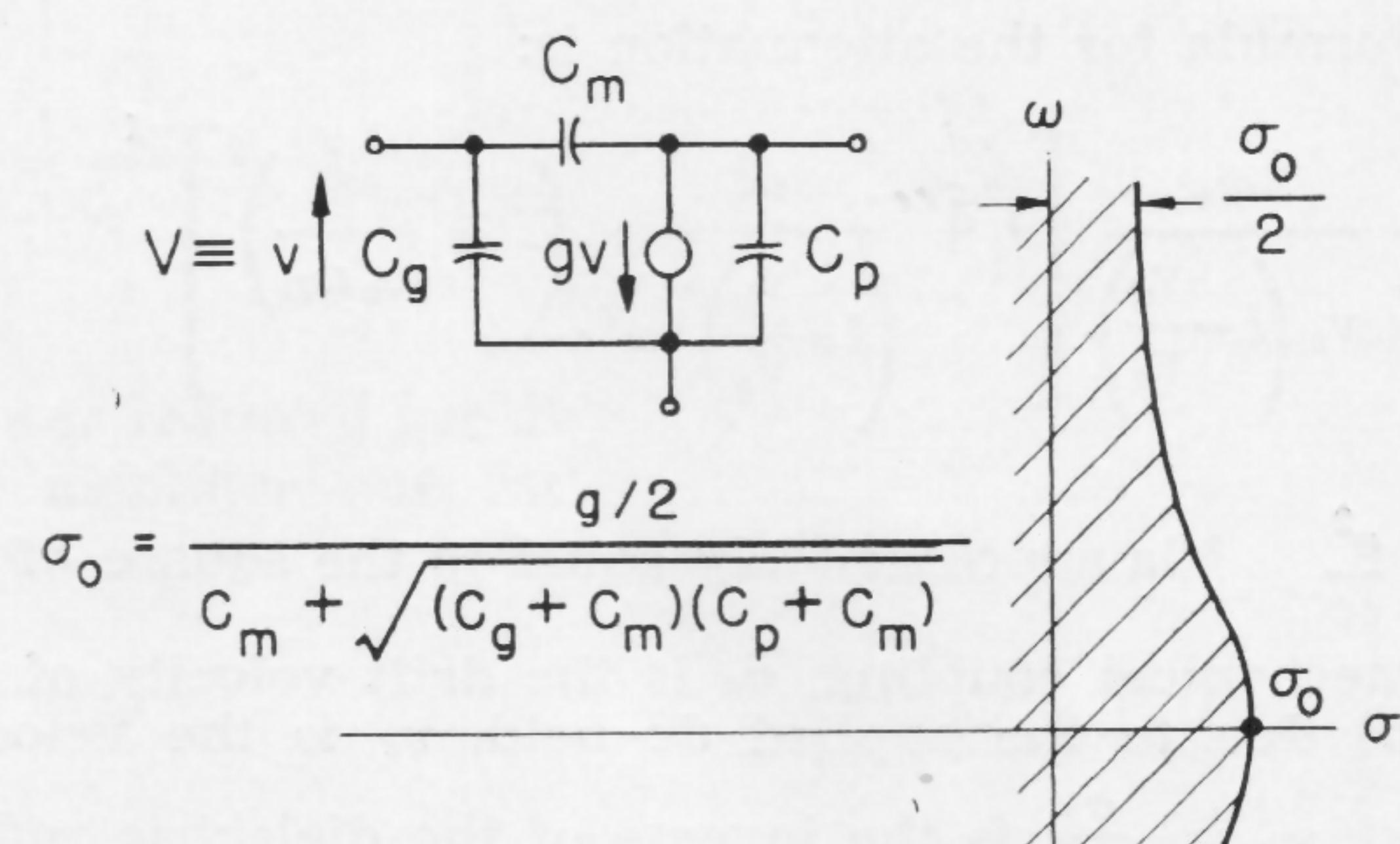


Figure 4—Region of unrestricted power for  $V+L+R+C$  circuits.

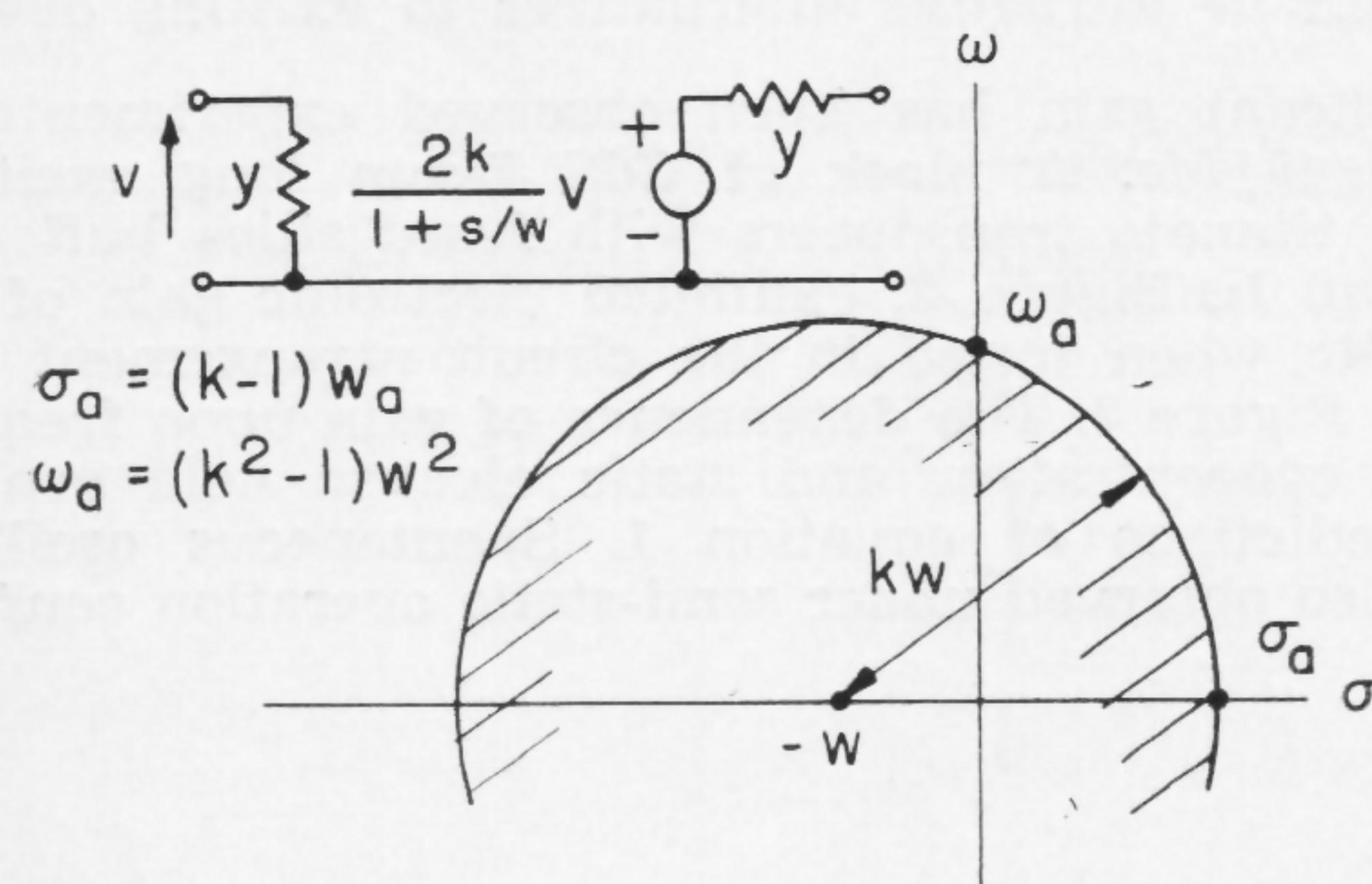


Figure 5—Region of unrestricted power angle for unilateral, single-time-constant amplifier.

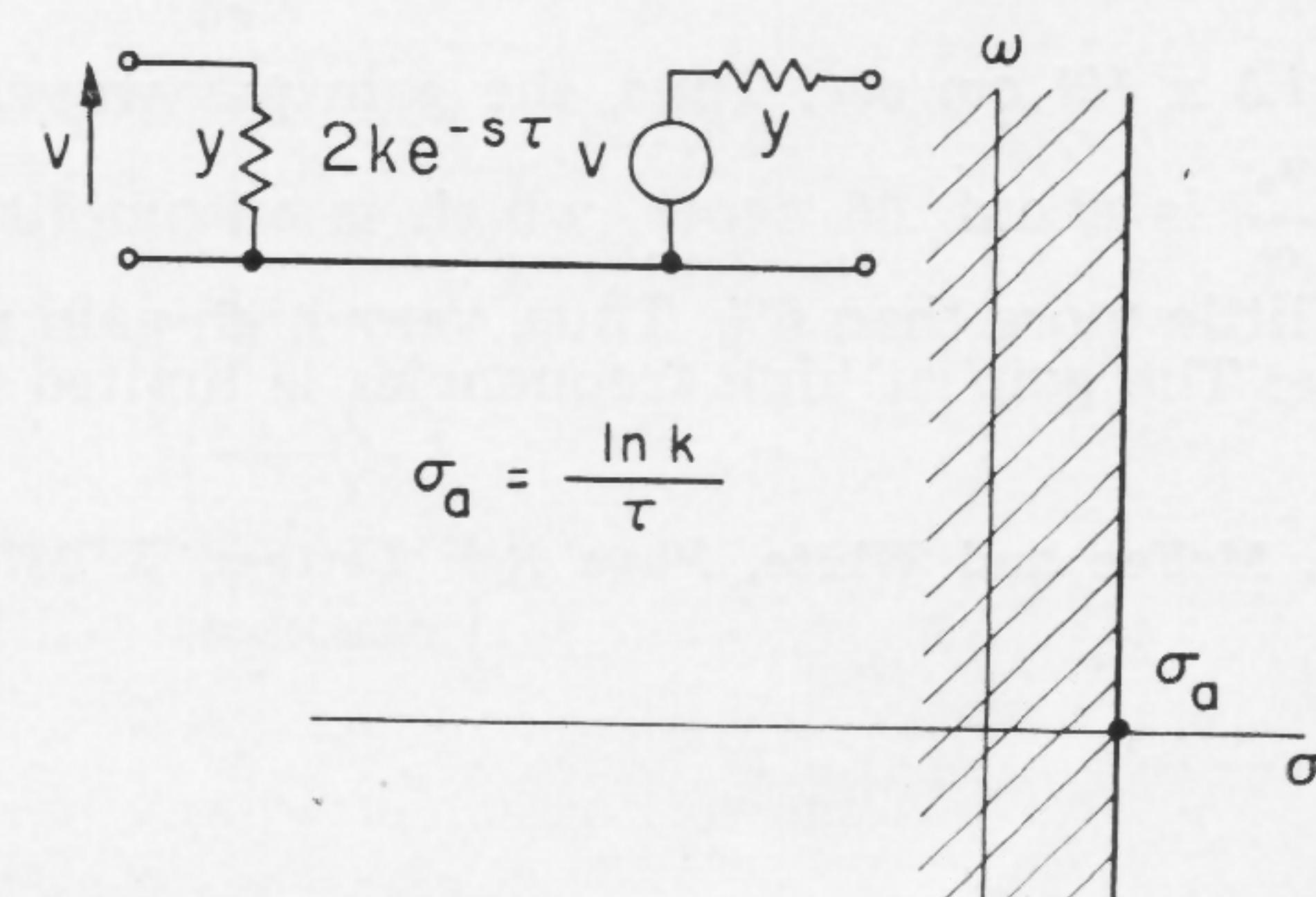


Figure 6—Region of unrestricted power for amplifier with delay.

## SESSION III: New Devices and Device Characterization

## WA 3.2: Amplification of Ultrasonic Waves

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Bell Telephone Laboratories, Inc.  
Whippany, N. J.

AN ULTRASONIC WAVE traveling in certain directions in a piezoelectric semiconductor, such as cadmium sulfide, can be amplified or attenuated by application of a *dc* electric field<sup>1</sup>. The direct current flowing through the medium creates a traveling *ac* electric field which interacts with the ultrasonic wave by piezoelectric coupling. Amplification can occur when the drift velocity of the electrons exceeds the velocity of sound in the medium.

The formula for the attenuation is:

$$\alpha = \frac{e^2}{2\epsilon c} \frac{\omega_c}{v_s \left(1 - \frac{v_d}{v_s}\right)} \left[ 1 + \frac{\omega_c^2}{\left(1 - \frac{v_d}{v_s}\right)^2 \omega^2} \left(1 + \frac{\omega^2}{\omega_c \omega_D}\right)^2 \right]^{-1} \quad (1)$$

where  $\frac{e^2}{\epsilon c}$  is approximately equal to the square of the electromechanical coupling,  $v_d$  is the drift velocity of the electrons due to the applied *dc* field,  $v_s$  is the velocity of sound,  $\omega_c = \frac{\sigma}{\epsilon}$  is the inverse of the dielectric reflection time,  $\sigma$  is the conductivity,  $\epsilon$  the dielectric permittivity, and  $\omega_D = \frac{v_s^2}{D}$  is the diffusion frequency, where  $D$  is the diffusion constant of the electrons. When the drift velocity exceeds the velocity of sound, the attenuation is negative, i.e., there is gain. If  $\omega_c \omega_D \ll \omega^2$ , the maximum

gain which occurs at  $\omega = \frac{\omega_c}{\left|1 - \frac{v_d}{v_s}\right|}$  is

$$\alpha = \frac{e^2}{4\epsilon c} \frac{\omega}{v_s} \quad (2)$$

For shear waves in cadmium sulfide  $\frac{e^2}{\epsilon c}$  is about .04,  $v_s = 1.8 \times 10^5$  cm/sec. Thus, the gain per wavelength,  $-2\pi \alpha \frac{v_s}{\omega}$  is about .06 neper, which is an amplitude gain of a little more than 6%. Thus, very high gain per cm is possible. The gain at high frequencies is limited by the

<sup>1</sup> Hutson, McFee and White, *Phys Rev Letters*, p. 237; Sept. 15, 1961.

diffusion term,  $\omega_D$ . The diffusion frequency for shear waves in CdS, using the *Einstein* relation for  $D$ , is about 770 Mc. However, at the expense of high *dc* power consumption, (high conductivity, high electric fields in equation 1) it is possible to have substantial gain at frequencies considerably above the diffusion frequency.

By properly varying the electric field and the conductivity, it is possible to minimize the power consumption per unit gain. Figure 1 shows the calculated minimum power consumption for longitudinal and shear waves in CdS. It should be possible to operate the amplifier continuously up to several-hundred megacycles before heating becomes excessive.

By using high power pulses of short duration, it should be possible to amplify ultrasonic waves at microwave frequencies.

The amplifier has value in research concerning the properties of piezoelectric semiconductors and as a tool to generate and detect ultrasonic waves at high frequencies in other materials.

Devices suggested by this development are a low-loss high-frequency delay line and an amplifier of electromagnetic energy at *uhf* or higher frequencies. Since the bandwidth of the amplifier is very large, similar to a traveling wave tube, the bandwidth of the devices in which it is used will ultimately be limited by the transducer bandwidth.

Ultrasonic absorption in materials and loss due to the transducers increases rapidly with frequency. Inclusion of an amplifier in a *uhf* or microwave ultrasonic delay line will greatly reduce the insertion loss. It is possible to make the overall gain of the ultrasonic amplifier larger than other losses and have an amplifier of electromagnetic energy. The overall noise figure of such a microwave amplifier system will be dependent upon transducer loss and considerable improvement over present transducer performance must be achieved before such amplifiers will be attractive alternatives to existing devices.

Significant gain has been observed experimentally at 15 and 45 Mc. A block of CdS 7-mm long excited by barium titanate transducers with fused silica buffer rods, as shown in Figure 2, exhibited electronic gain of 40 db at 45 Mc when tested in the circuit arrangement shown in b of Figure 2. The dependence of gain upon frequency, carrier concentration and static electric field confirmed the predictions of equation 1. Spontaneous oscillations were also observed under semi-static operation conditions.

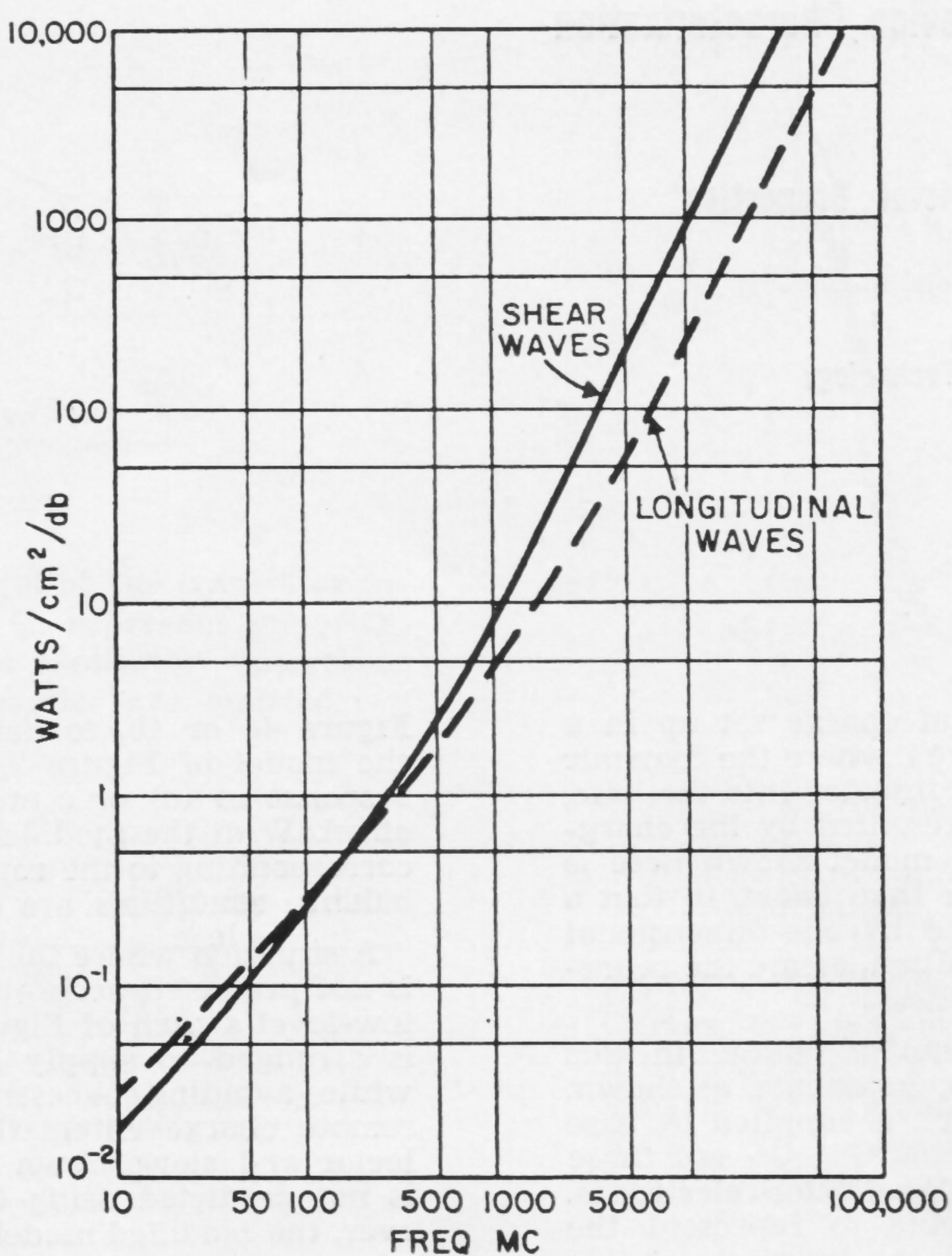


Figure 1—Calculated minimum power required per db amplification for CdS ultrasonic amplifier one  $\text{cm}^2$  in cross section.

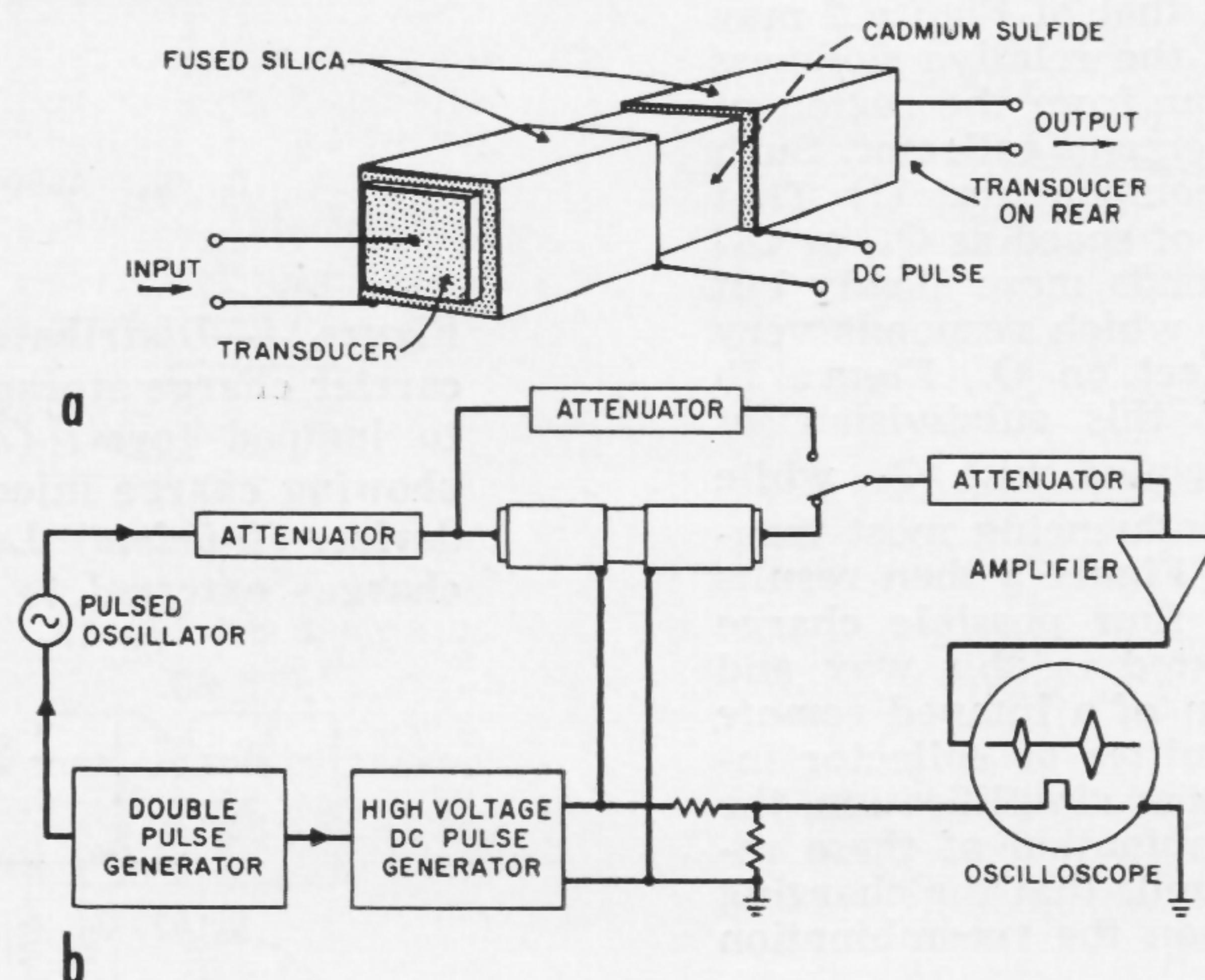


Figure 2—(a) A low frequency CdS ultrasonic amplifier employing thickness mode transducers and buffer rods for time and voltage isolation. (b) Circuit used to test the ultrasonic amplifier.

## SESSION III: New Devices and Device Characterization

## WA 3.3.: Charge Definition of Transistor Properties\*

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THE ESSENTIALLY-DISTRIBUTED nature of charge set up in a transistor is emphasized in *a* of Figure 1, where the dynamic behavior of minority carrier charges injected into the base, emitter and collector regions is represented by the charging of RCG transmission lines. The model shown here is to some extent diagrammatic, rather than exact, in that a 3-dimensional medium is represented by one-dimensional lines; depletion layer charges are omitted, as are the representations of other extrinsic properties.

The total quantity  $Q$  of the minority charge in this illustration may be divided into six components, as shown, the majority counterpart  $-Q$  of which is supplied by base current flow. In particular, components  $Q_{b1}$ ,  $Q_{b2}$  are those contained between the emitter and collector electrodes. For practical purposes it is desirable to represent the transistor by a simple lumped model, the simplest possible one being that of Figure 2 in which all charge injected by emitter, collector or base, respectively, is supposed to have the same time dependence. This model corresponds to the definition of charge control parameters for the device, relating charges delivered through the base to the resulting electrode currents. If the base charge concerned in such definitions, and in Figure 2, is the total charge  $Q$  defined in Figure 1*a*, the characterization can apply accurately only for slowly varying transients; otherwise, for more rapid changes, only a portion of the total steady-state charge  $Q$  can be involved in the characterization. In many cases, testing procedures for deriving the parameters of this simple lumped model reveal its shortcomings (viz., the *wiggle* effect of Sparks<sup>1</sup>), while careless adoption of the model can result in poor prediction of device performance or erroneous estimation of its physical properties under certain circumstances.

A more representative model than that of Figure 2 may be arrived at if account is taken of the relative slowness of response of the charge situated far from the region of the base immediately between emitter and collector. Such charge may be divided into three components: (1) That which responds with the same order of speed as  $Q_{b1}$  or  $Q_{b2}$  as appropriate; (2) that which responds more slowly but affects  $Q_b$  appreciably; and (3) that which responds very slowly and has negligibly small effect on  $Q_b$ . Figure 1*b* shows a lumped representation of this subdivision of charge. Component  $\bar{Q}_1$  may be associated with  $Q_b$ , while  $\bar{Q}_3$  is neglected as not significantly influencing most transient behavior. The device model of Figure 3 then results if the assumption is made that all four possible charge components outside  $Q_b$  may be treated in this way and combined into a single representation of a lumped *remote* charge  $Q_{r1}$  or  $Q_{r2}$  associated with emitter or collector injection, respectively. Finally, for further simplification, the conductances representing the recombination of these remote charges are omitted on the grounds that the charging currents  $Q_{r1}$ ,  $Q_{r2}$  are much larger than the recombination currents in most transients.

The validity and usefulness of this modified lumped model has been verified. If a transistor is tested, as in

Figure 4*a* or 4*b*, to derive charge control parameters or the model of Figure 2, inability to achieve square-wave response in (a) or a null in (b) is often observed; *wiggle* effect. With the modified test circuits of Figures 4*c* or 4*d*, corresponding to the representation of remote charge, good balance conditions are easily achieved in such cases.

A situation where the transient response of the transistor is not predicted accurately by the simple model is for the low-level switch of Figure 5. Here, the switching network is arranged to supply and remove base charge quickly, while avoiding excessive output-voltage transients; but remote charge enters the base between emitter and collector and slows down the switch-off process. This effect is not predicted using the simple model; Figure 5. However, the modified model predicts the output voltage wave-

[Continued on page 105]

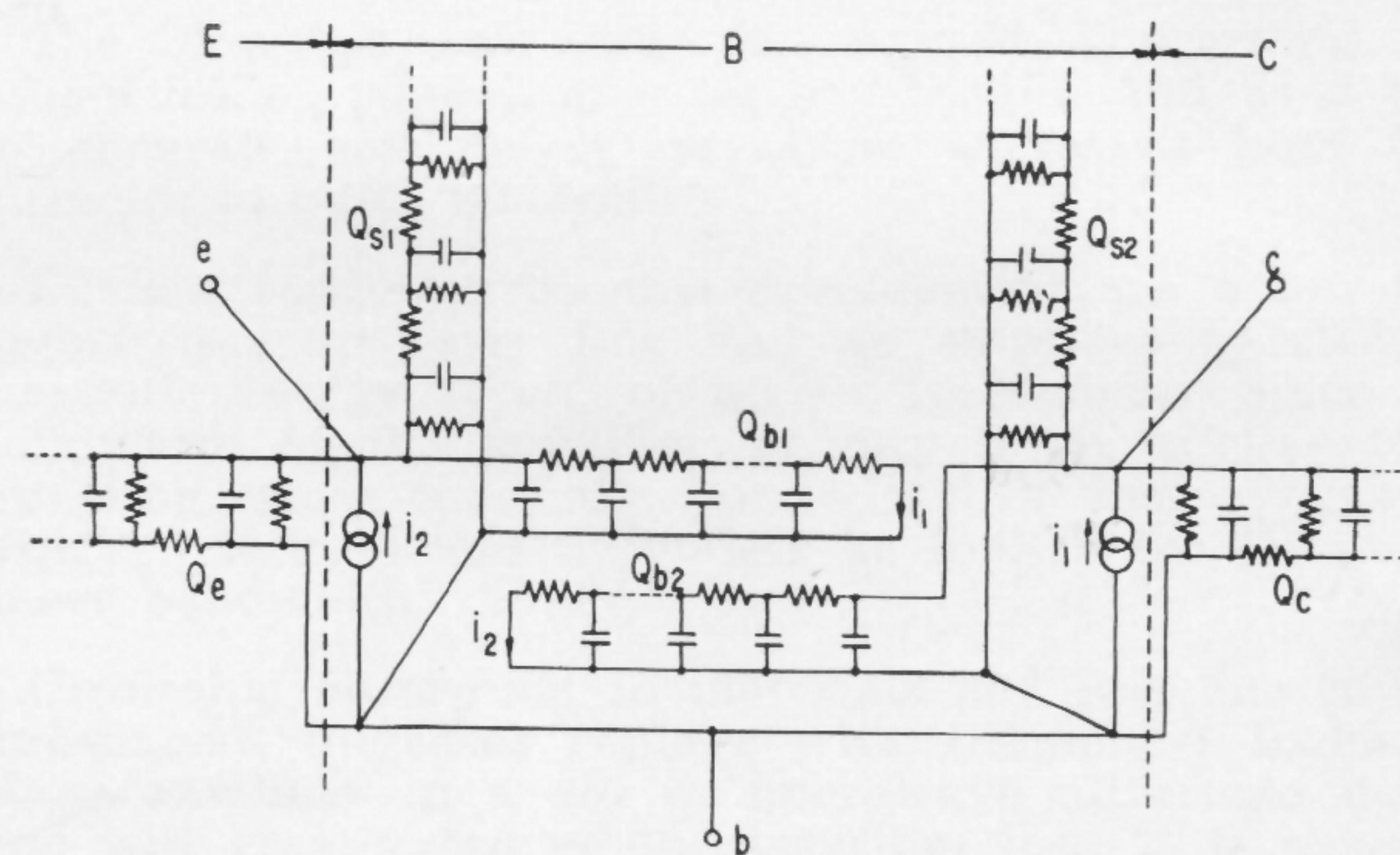
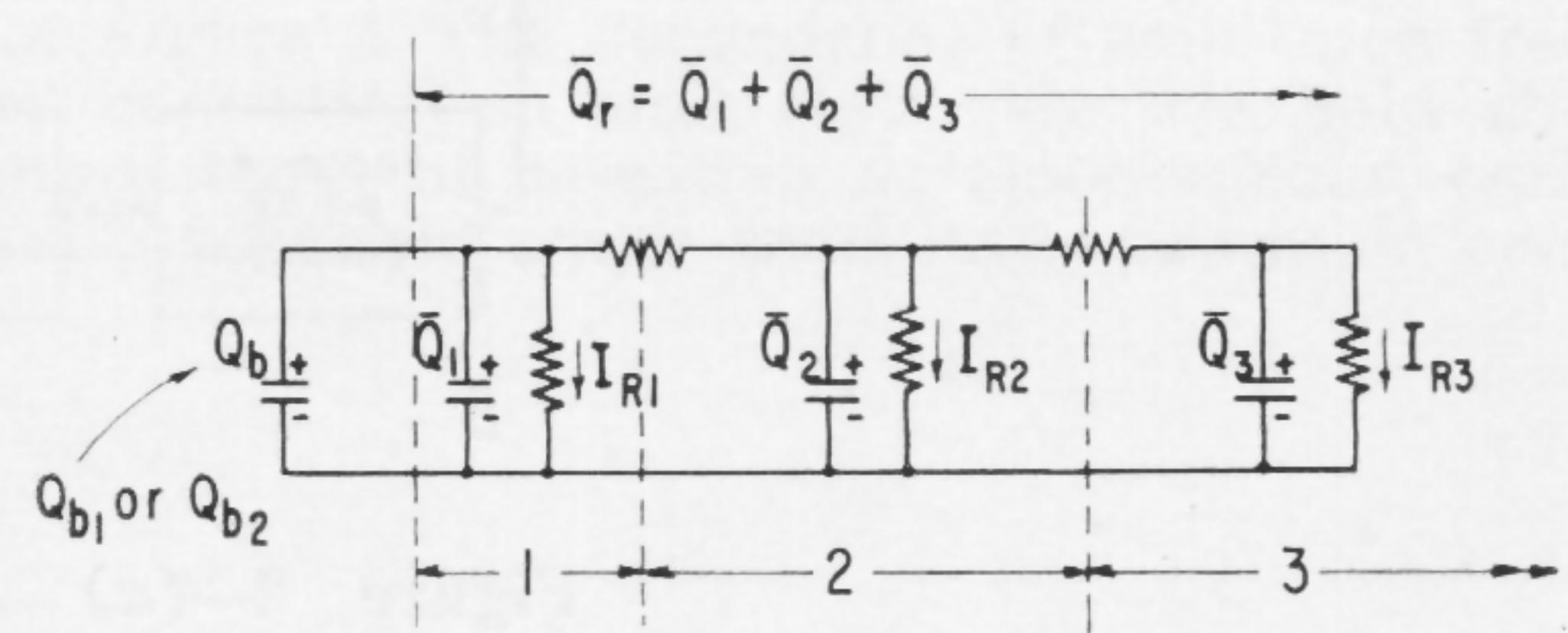
 $Q_{S1}, Q_{S2}$  : ASSOCIATED WITH SURFACE RECOMBINATION

Figure 1—Distributed model representing minority carrier charge storage in the transistor; its reduction to lumped form: (a-*above*) The distributed model, showing charge injected into the three regions of the device. (b-*below*) Lumped representation of *remote* charges external to  $Q_b$ ;  $I_r$  = recombination current.

 $\bar{Q}_r$  = REPRESENTS  $Q_{S1}, Q_{S2}, Q_e$  or  $Q_c$ 

<sup>1</sup>Sparks, J. J., "A Study of the Charge Control Parameters of Transistors," Proc. IRE, p. 1696-1705; October, 1960.

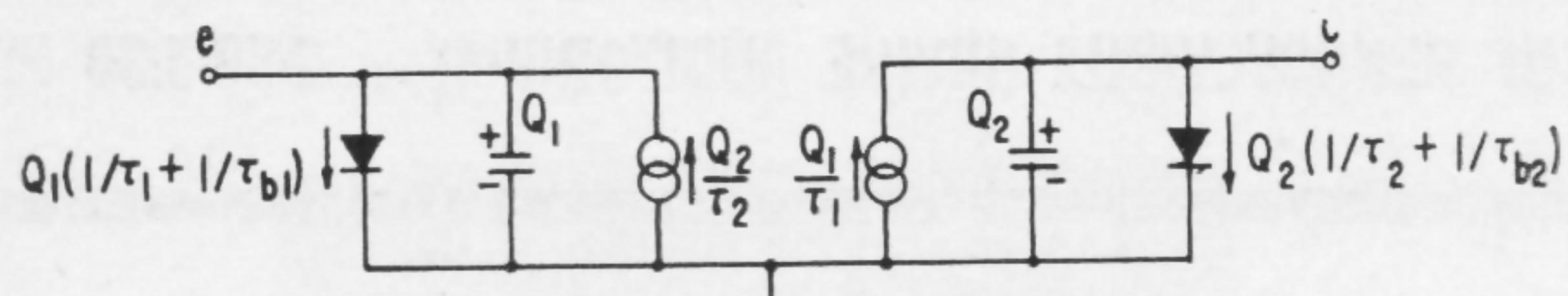


Figure 2—Simplest lumped model of the transistor in two alternative forms.  $Q_1$  and  $Q_2$  represent minority charge due to emitter and collector injection, respectively. Extrinsic properties are omitted.

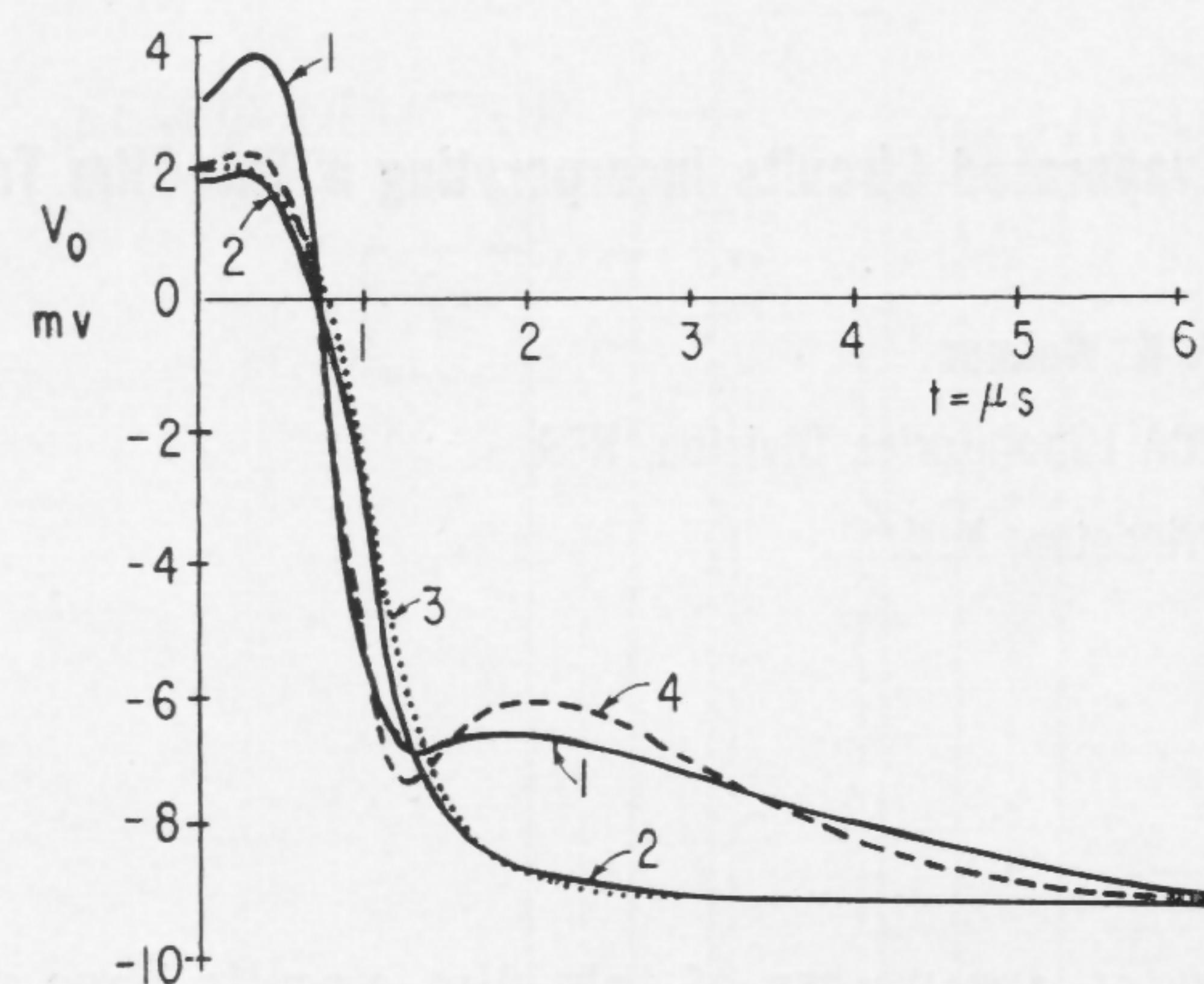
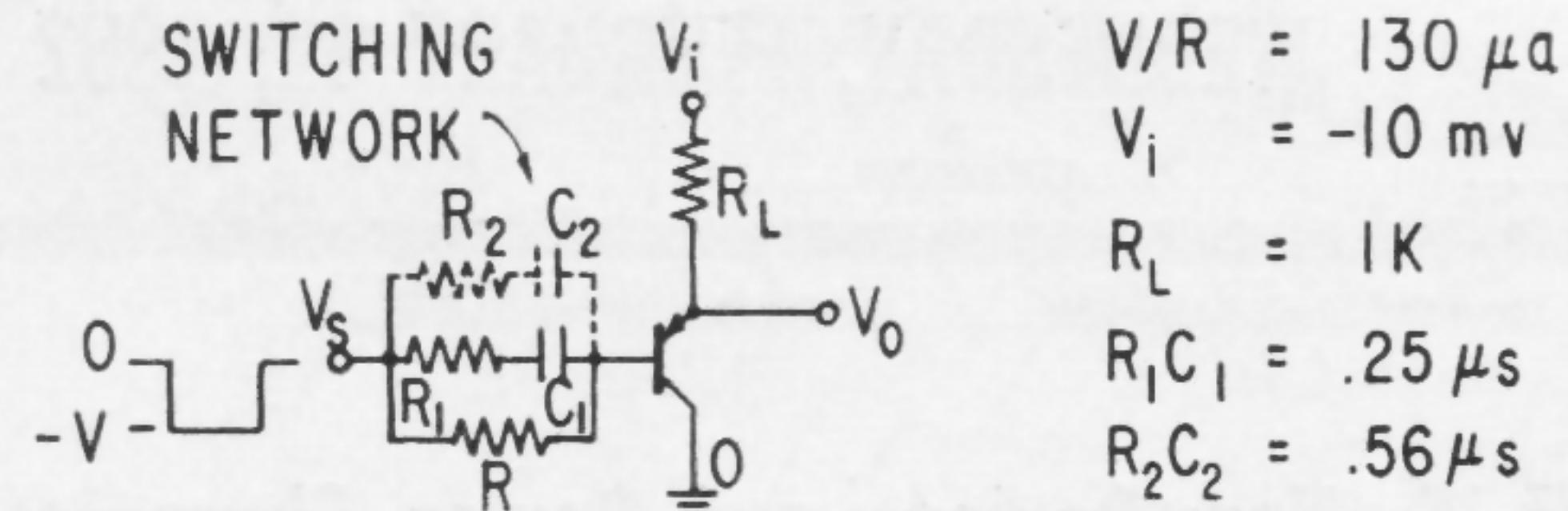


Figure 5—Response of low-level transistor switch. Curves (1) measured,  $R_2C_2 = 0$ ; (2) measured,  $R_2C_2 = 0.56 \mu\text{sec}$ ; (3) computed from model of Figure 2,  $R_2C_2 = 0$ ; (4) computed from model of Figure 3,  $R_2C_2 = 0$ . In modified model  $\tau_1 = 0.02 \mu\text{sec}$ ,  $\tau_{r2} = 0.59 \mu\text{sec}$ ,  $\tau_2 = 0.07 \mu\text{sec}$ ,  $\tau_{r2} = 0.50 \mu\text{sec}$ .

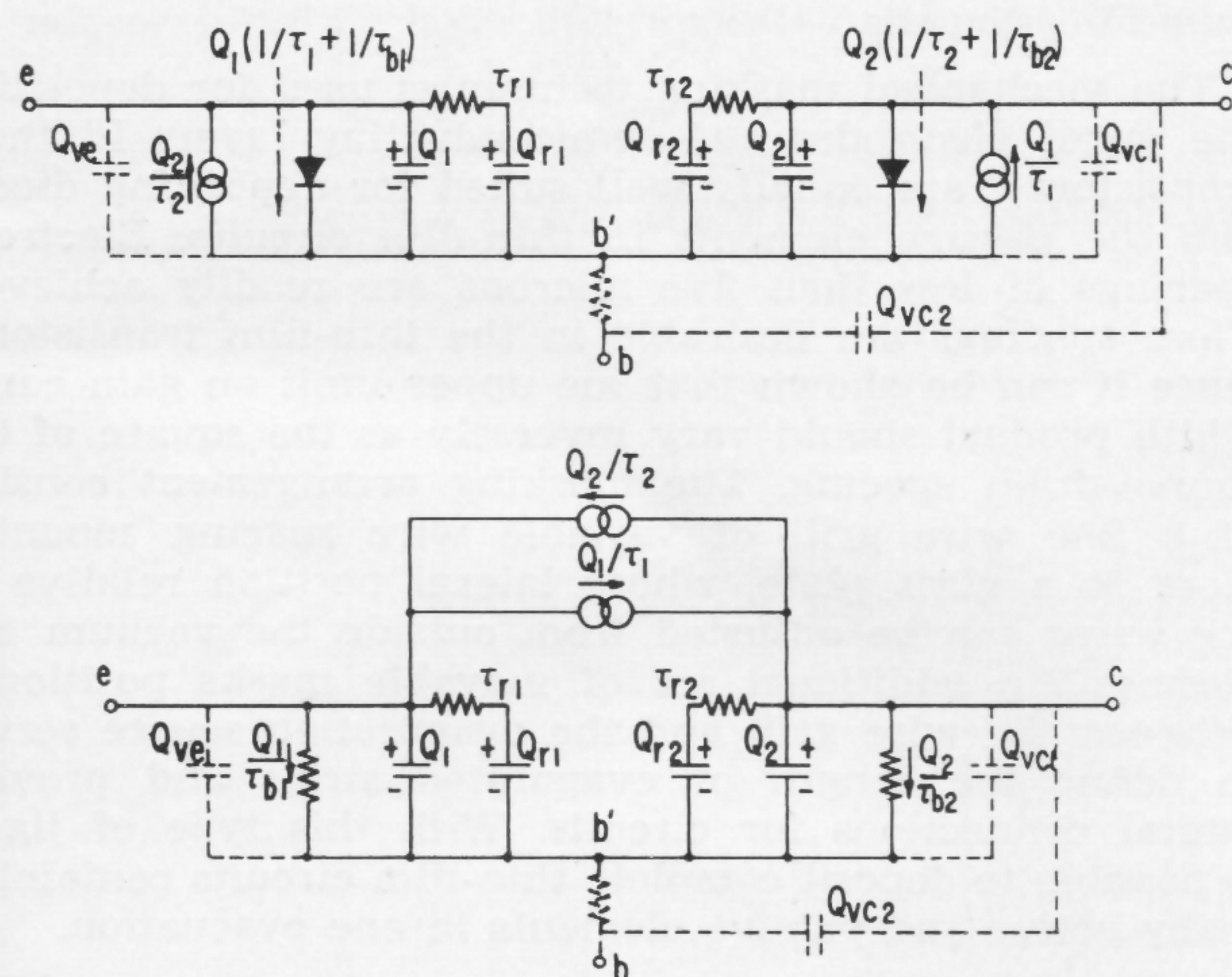


Figure 3—Modified lumped model of the transistor, incorporating representation of *remote* charge  $Q_r$  (i.e., of  $Q_2$  in Figure 1b), but neglecting its recombination.

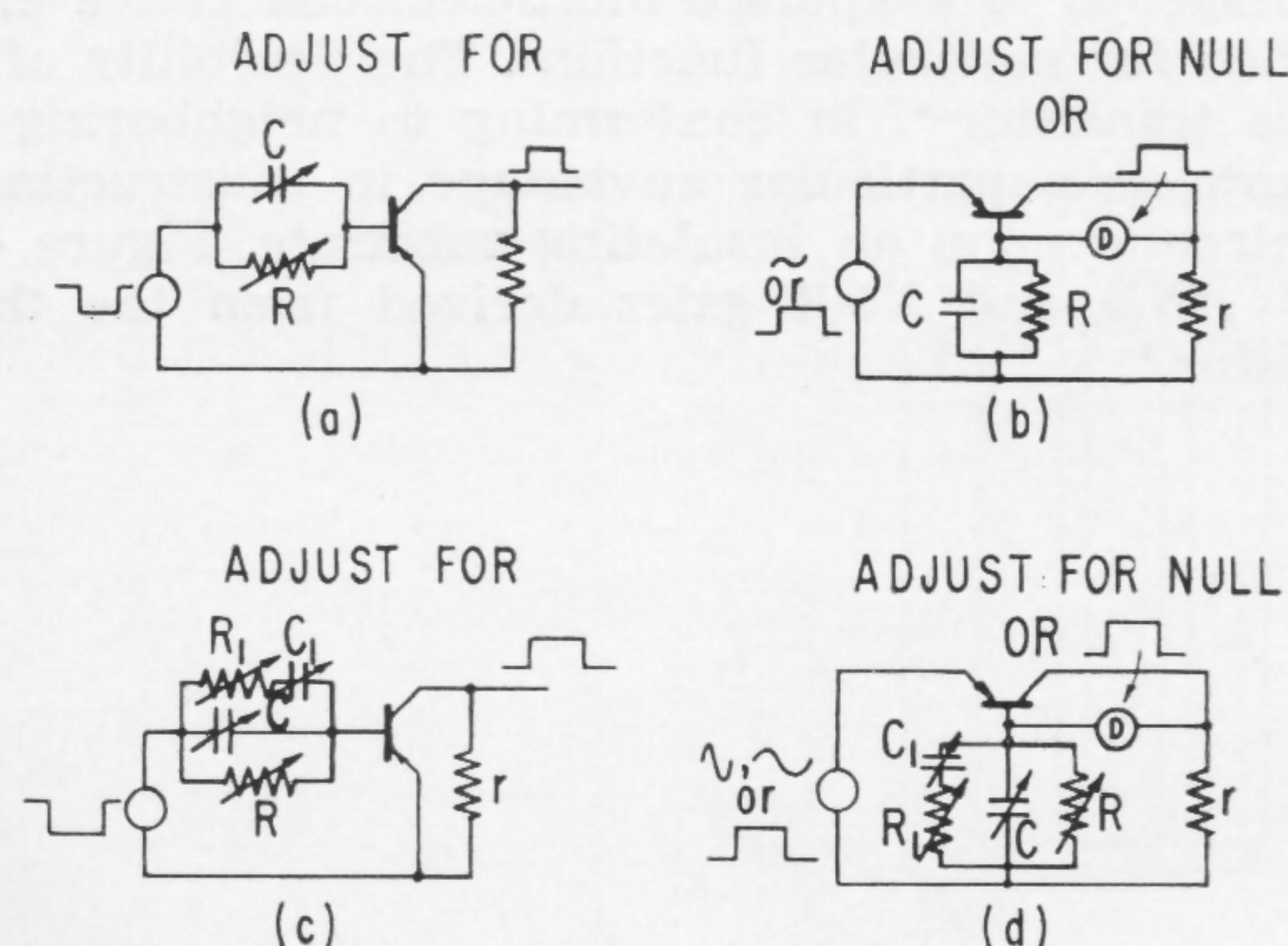
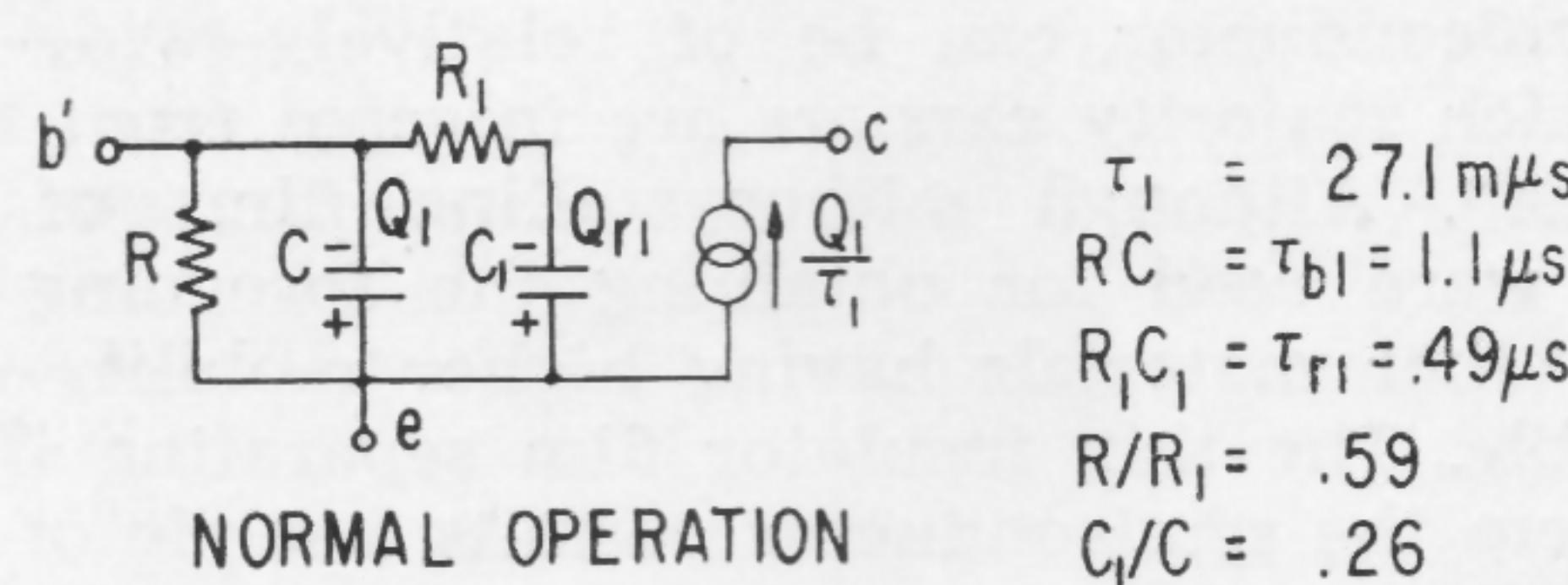


Figure 4—Schematic circuit arrangements for transistor testing to derive *charge-control* parameters: (a) and (b) correspond to model of Figure 2; (c) and (d) correspond to model of Figure 3.

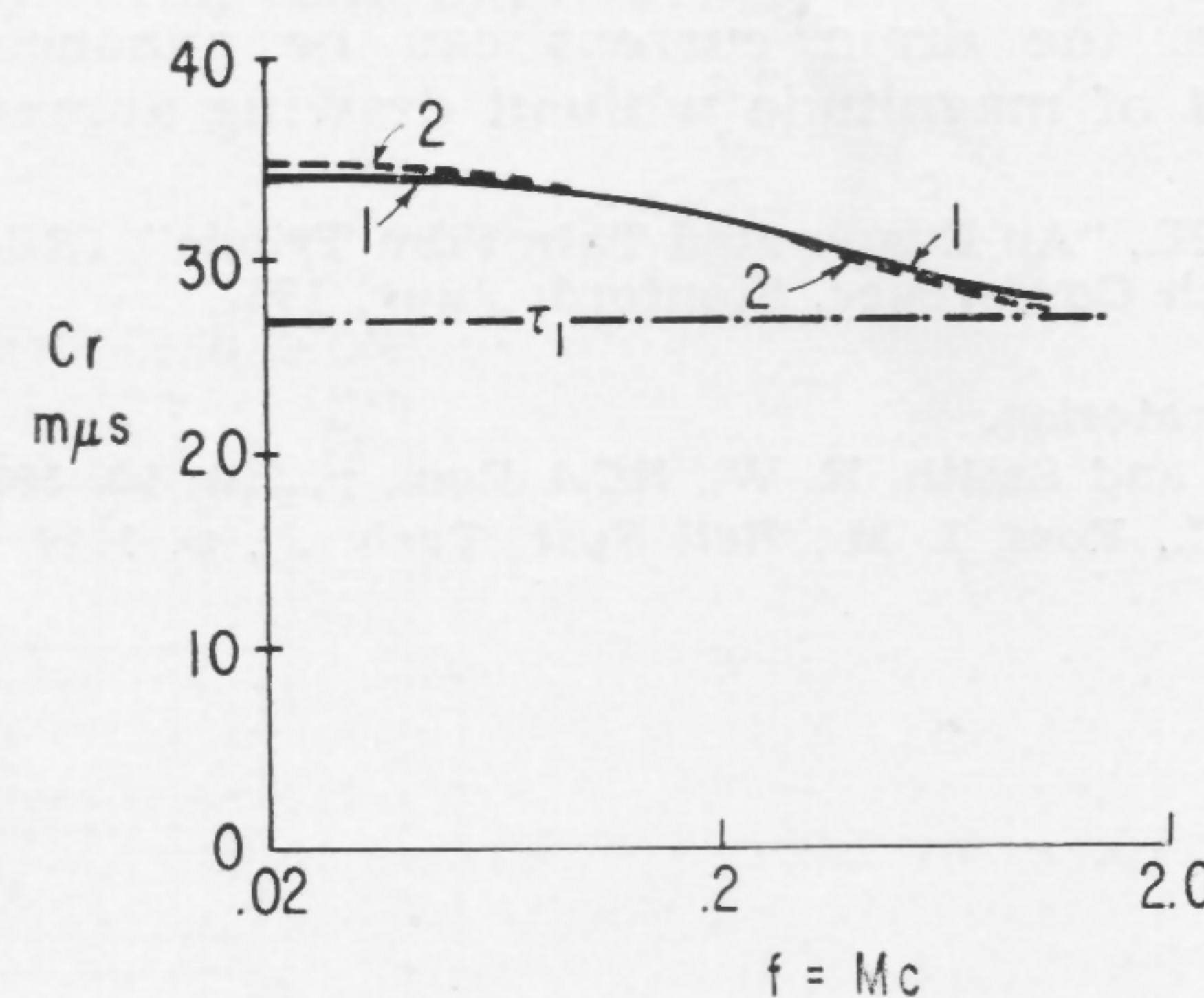


Figure 6—Normal *transit time*  $C_r$  as measured by bridge of Figure 5b. For simple model  $C_r = \tau_1$ . Curve (1) shows measured  $C_r$  for an alloyed uniform base sample; (2) shows  $C_r$  for the given model.

## SESSION III: New Devices and Device Characterization

## WA 3.4: Evaporated Circuits Incorporating a Thin-Film Transistor

P. K. Weimer

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THE POTENTIAL ADVANTAGES of thin-film circuits have until now been severely limited because of the lack of an amplifying element which could be deposited by thin-film techniques. A new class of thin-film transistors \*, fabricated by evaporation of all components upon an insulating substrate, is now being developed\*\*. One type, utilizing an insulated control gate<sup>1</sup>, has yielded the following extremely promising results: Voltage amplification factors of greater than 100, transconductances greater than 10,000  $\mu$ hos, input impedances of more than  $10^5$  ohms shunted by approximately 50 pf, and gain-bandwidth products exceeding 10 Mc. Switching speeds faster than .1  $\mu$ sec have been measured.

Figure 1 shows a typical set of operating characteristics for this thin-film transistor. Although the curves resemble those of a tube pentode or a unipolar field-effect transistor, a striking difference is noted in the choice of control gate bias.

Figure 2 shows a cross-sectional view of one form of insulated-gate of the new thin-film transistor \*. The electrodes, insulator and semiconductor are deposited by evaporation in successive layers on to a glass substrate. The semiconductor can be of relatively wide-band gap into which majority carriers are injected from the source electrode<sup>2</sup>. Although microcystalline films of cadmium sulfide were used for obtaining the foregoing measurements, other materials having higher mobility should be applicable. The thin insulator film separating the control gate from the semiconductor permits a mode of operation quite different from that of the conventional field effect transistor<sup>3</sup>. By biasing the gate positively, with respect to the source, the drain current can be enhanced by several orders of magnitude without drawing appreciable

gate current. Although negative bias operation is also possible, the enhancement mode offers a significant practical advantage: Direct coupling between stages becomes feasible, greatly simplifying the connections in evaporated thin film circuits.

The mechanical masking techniques used for depositing the metal electrodes and semiconducting layers in these transistors \* are equally well suited for depositing diodes and the passive elements in thin-film circuits. Electrode spacings of less than five microns are readily achieved. Close spacings are desirable in the thin-film transistor \*, since it can be shown that the upper limit on gain-bandwidth product should vary inversely as the square of the source-drain spacing. The masking arrangement consists of a fine wire grill of variable wire spacing mounted close to a glass plate, whose lateral position relative to the wires can be adjusted from outside the vacuum enclosure. An additional set of movable masks positioned between the wire grill and the evaporation source serves to define the length of evaporated strips and provide lateral connections for circuits. With this type of jig it is possible to deposit complete thin-film circuits containing many active and passive elements in one evacuation.

Figure 3 illustrates a three-stage thin-film amplifier which was deposited using the techniques described. The sharpness of the lines are such that much finer dimensions and greater circuit complexity within a given area should be readily possible.

An important field of application of the thin-film transistor \* is expected to be in the fabrication of miniaturized computer circuits. Although the basic elements of a computer could be constructed using these transistors \* in combination with other thin-film components, it may be advantageous to evaporate multielectrode active elements designed for particular functions. The flexibility of design of this transistor \*, in conforming to neighboring circuit elements, is a particular advantage in constructing thin-film circuits upon an insulating substrate. Figure 4 illustrates AND and NOR gates derived from the thin-film transistor \*.

<sup>1</sup> Weimer, P. K., "An Evaporated Thin Film Triode", IRE-AIEE Device Research Conference, Stanford, June, 1961.

\* TFT.

\*\* RCA Laboratories.

<sup>2</sup> Ruppel, W., and Smith, R. W., RCA Rev., p. 702; 20, 1959.

<sup>3</sup> Dacey, G. C., Ross, I. M., Bell Syst. Tech. J., p. 1149; June, 1955.

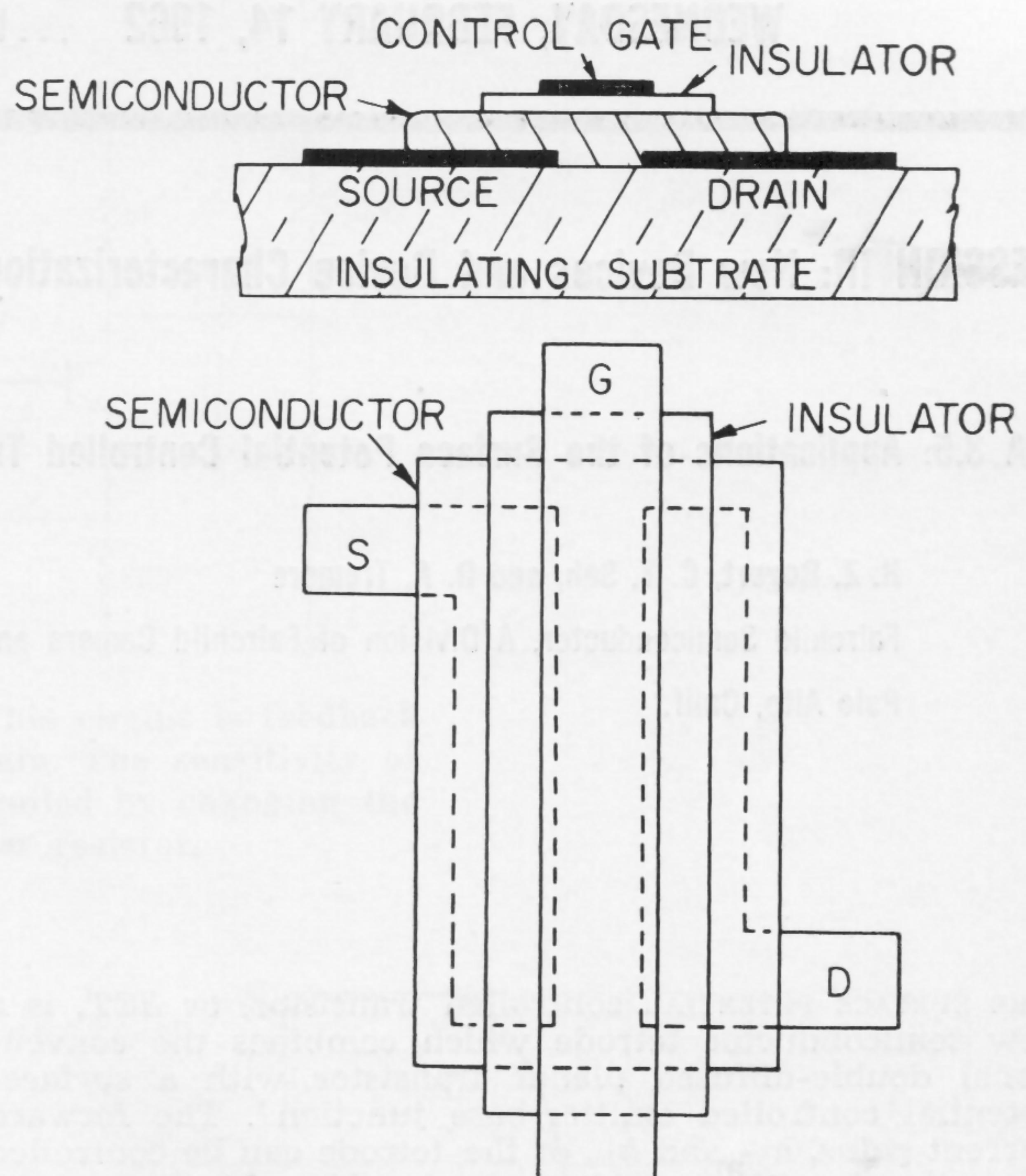
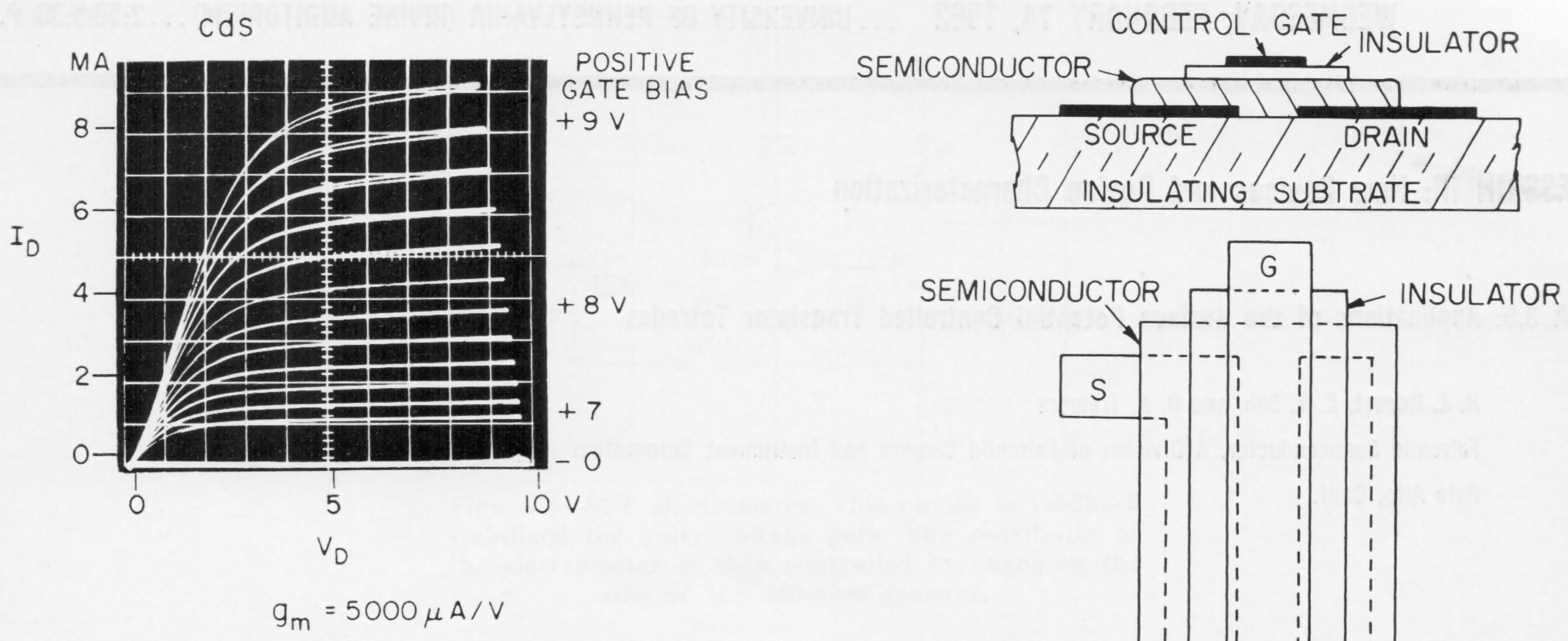


Figure 2 (right, above)—Cross-sectional and plan view of an insulated-gate thin-film transistor\*.

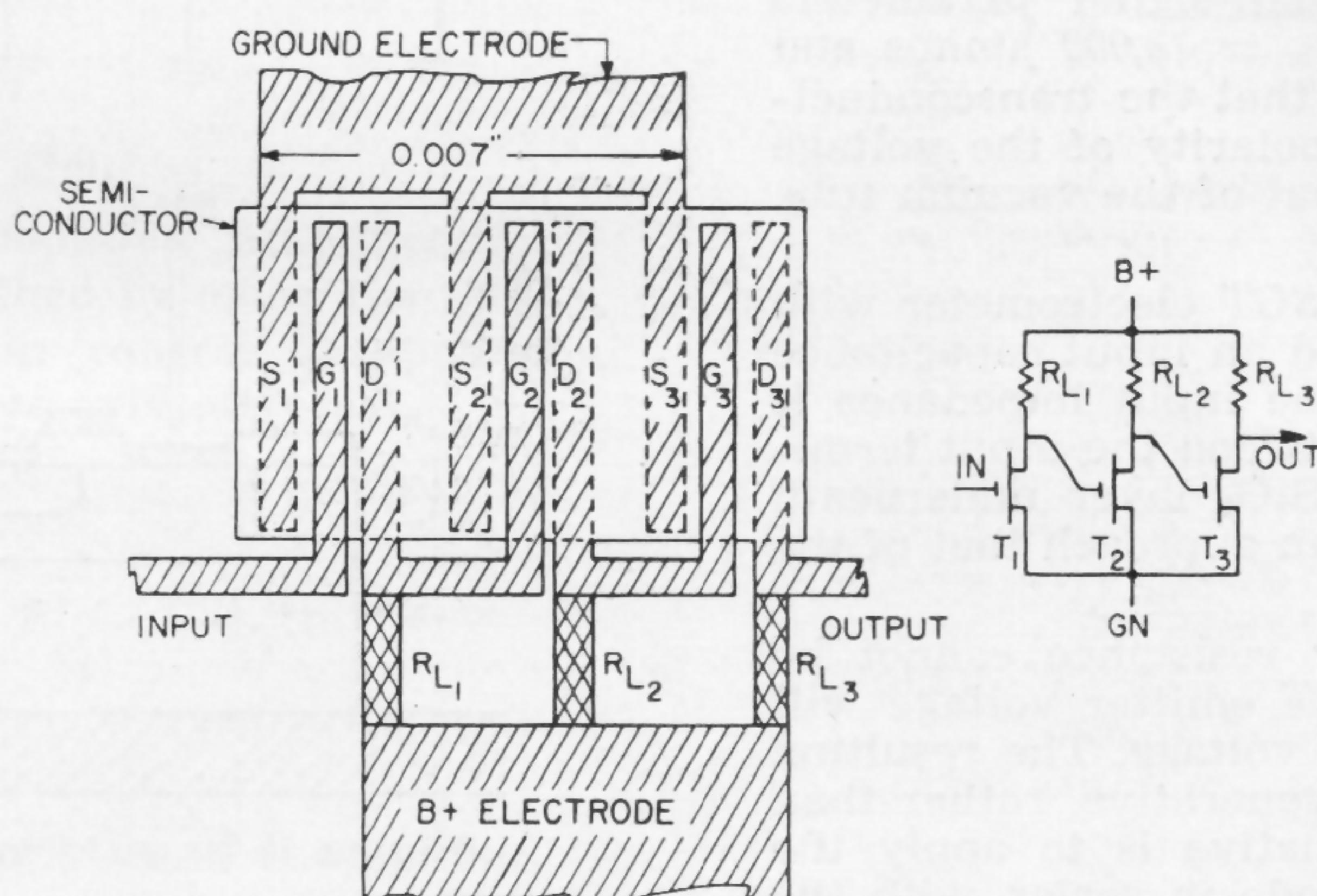


Figure 3—A three-stage thin-film amplifier incorporating thin-film transistors\*.

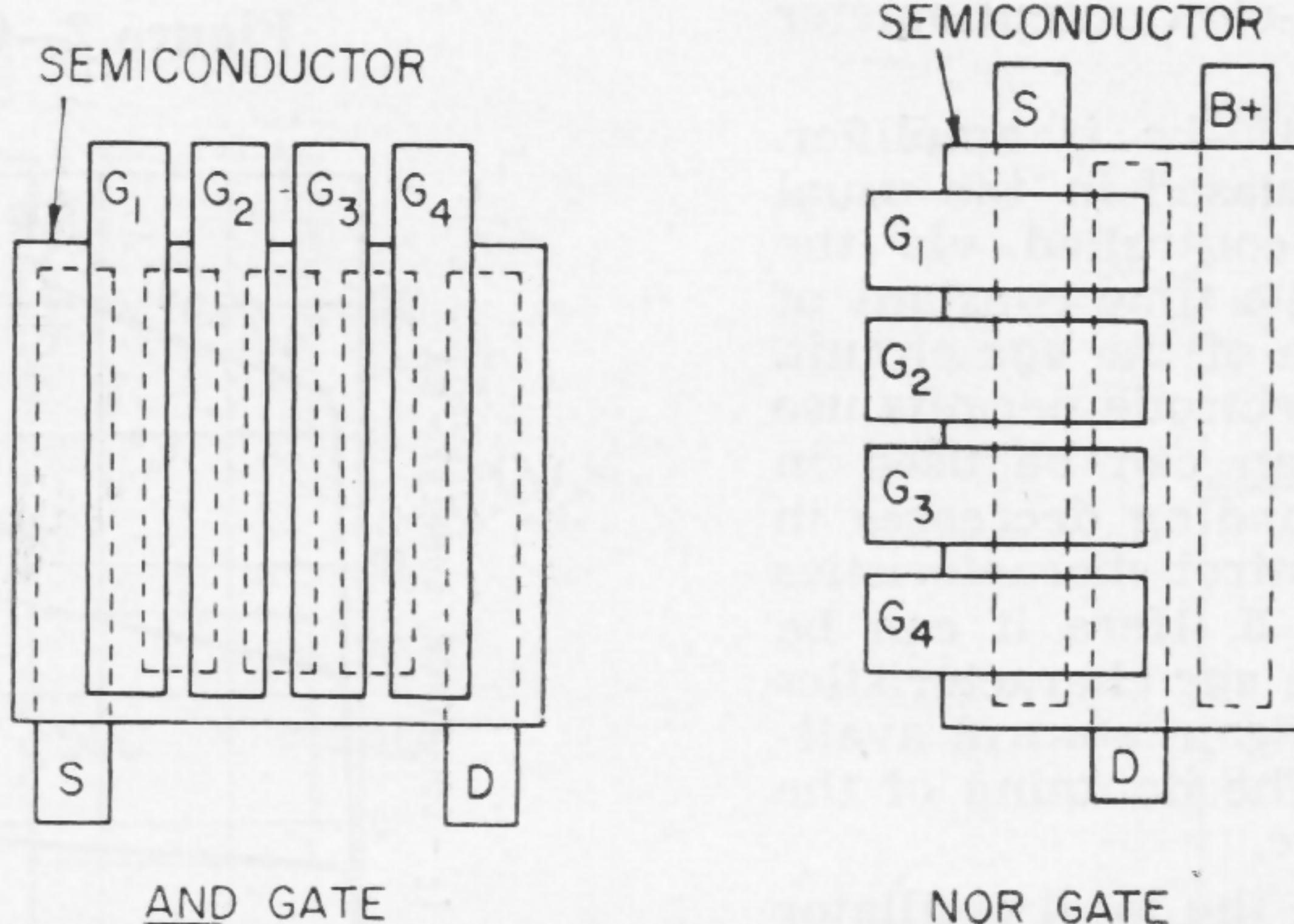


Figure 4—Thin-film AND and NOR gates based upon the thin-film transistor\*.

## SESSION III: New Devices and Device Characterization

## WA 3.5: Applications of the Surface Potential Controlled Transistor Tetrodes

H. Z. Bogert, C. T. Sah, and D. A. Tremere

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THE SURFACE POTENTIAL controlled transistor, or *SCT*, is a new semiconductor tetrode which combines the conventional double-diffused planar transistor with a surface-potential controlled emitter-base junction<sup>1</sup>. The forward current gains,  $h_{FE}$  and  $h_{fe}$ , of the tetrode can be controlled from the fourth or grid electrode shown in the cross-sectional view of Figure 1. Here we see the metal grid electrode over the  $\text{SiO}_2$  which covers the emitter base junction. The impedance of this electrode is typically  $10^{15}$  ohms and is shunted with a capacitance of 20 pf for the developmental devices to be discussed. Circuit applications include an electrometer and the *agc* of *if* stages.

Figure 2 shows an *SCT* collector family with grid voltage as a parameter. The pertinent small-signal parameters at  $V_C = 5$  v and  $I_c = 10$  ma are  $g_m = 12,000 \mu\text{hos}$  and  $r_p = 3600$  ohms. It should be noted that the transconductance of the *SCT* is such that the polarity of the voltage gain of a grid-input stage, unlike that of the vacuum tube pentode, is noninverting.

Figure 3 shows the circuit of an *SCT* electrometer with a sensitivity of 100 mv full scale and an input capacitance of 20 pf. The resistive portion of the input impedance is determined by the leakage paths between the input terminals and the leakage through the  $\text{SiO}_2$  layer underneath the gate electrode. This resistance can approach that of the gate electrode itself,  $10^{15}$  ohms.

Current feedback via an emitter resistance cannot be used in an *SCT* electrometer for the emitter voltage will then be out of phase with the gate voltage. The resulting circuit will therefore tend to be regenerative, rather than degenerative. Thus, the only alternative is to apply the feedback voltage to the gate electrode in series with the signal voltage. In the circuit of Figure 3, this voltage is taken from the top of the 200-ohm resistor. The voltage gain to the top of this resistor is then  $A/(1-A)$  where  $A$  is the open loop gain. The open loop gain is about 50, so the voltage gain from the input to the 200-ohm resistor is very nearly unity. Scale changes may be accomplished by changing the size of the 200-ohm resistor. The output meter may be zeroed by adjusting the 100,000-ohm potentiometer in the base circuit of the *SCT*.

Figure 4 shows a gain-controlled 450-*kc* *if* amplifier. The transistor portion of the *SCT* is biased in the usual fashion and the bias point is then controlled via the gate electrode. A low-pass filter having a time constant of .1-sec is used to control the attack time of the *agc* circuit. Here the high impedance of the gate electrode permits use of a much smaller filter capacitor than can be used in transistor *agc* amplifiers, with corresponding decreases in size and cost of the circuit. The gain-control characteristics of the amplifier are shown in Figure 5. Here it can be seen that there is a built-in delay to the *agc* characteristics of the amplifier, with the full 30-db of gain control available in the 1.5-v range from 1-2.5 v. The detuning of the amplifier is small, typically about 10 *kc*.

Figure 6 shows a tetrode mixer. Here the local oscillator signal is applied to the grid and the input signal is applied

to the base through a 1000-ohm resistor. Conversion gains of 20 db may be realized with this circuit when an .3 v rms local oscillator signal is used on the gate.

A simple oscillator circuit, which takes advantage of the fact that in the *npn* type tetrode the collector and the grid voltages are in phase<sup>1</sup>, is shown in Figure 7. In this circuit, bias stability is obtained by emitter degeneration. Oscillation, obtained at 10 *kc* with this circuit, is also possible at higher frequencies if the base to collector capacitance is neutralized.

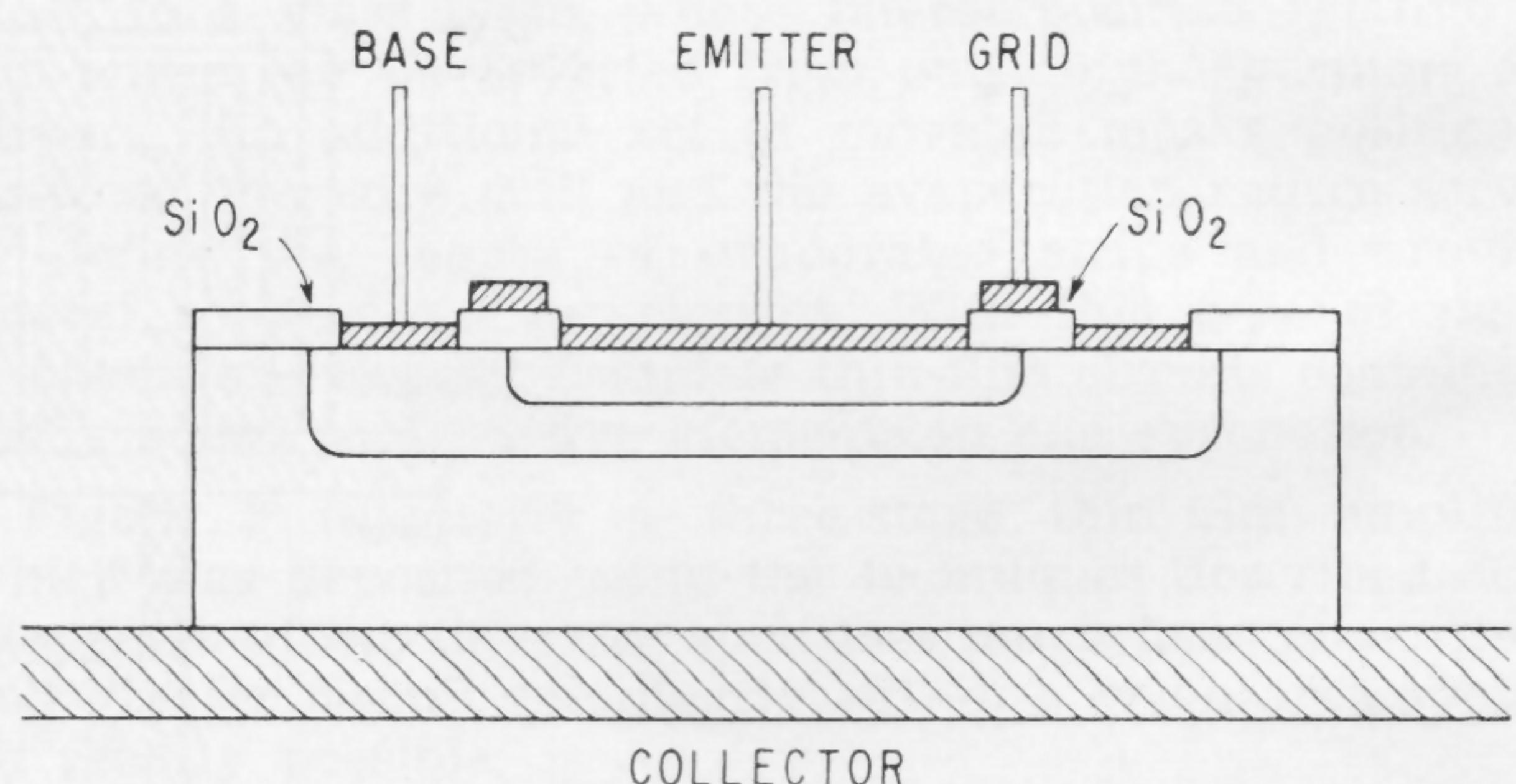
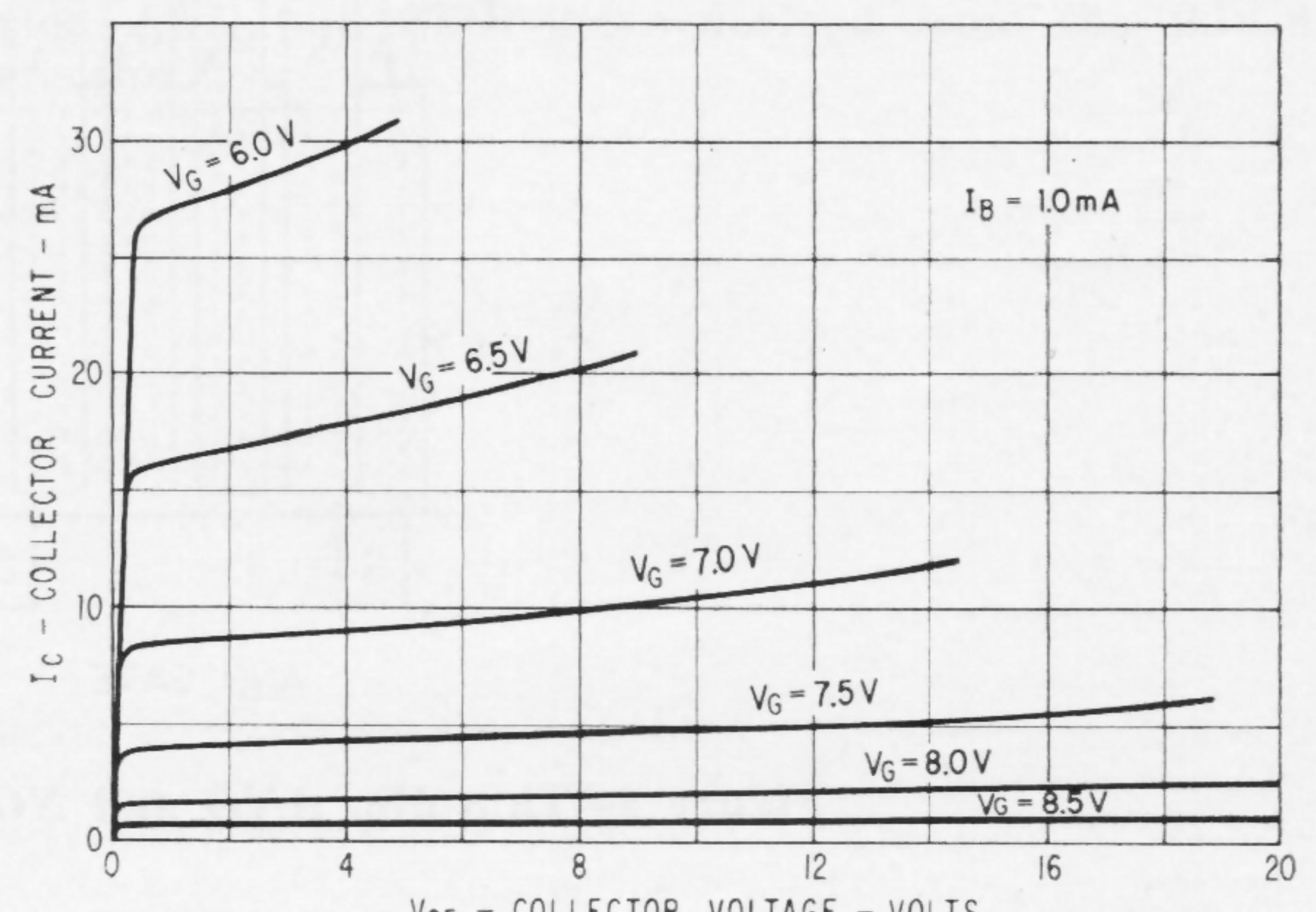


Figure 1—Cross-sectional view of tetrode. The grid electrode is shown on top of the  $\text{SiO}_2$  which covers the emitter base junction.

(Below)

Figure 2—Collector family for the *SCT*.



<sup>1</sup> Sah, C. T., "A New Semiconductor Tetrode, the Surface-Potential Controlled Transistor," (WESCON, August, 1961), Proc. IRE, p. 1623-1634; Nov., 1961.

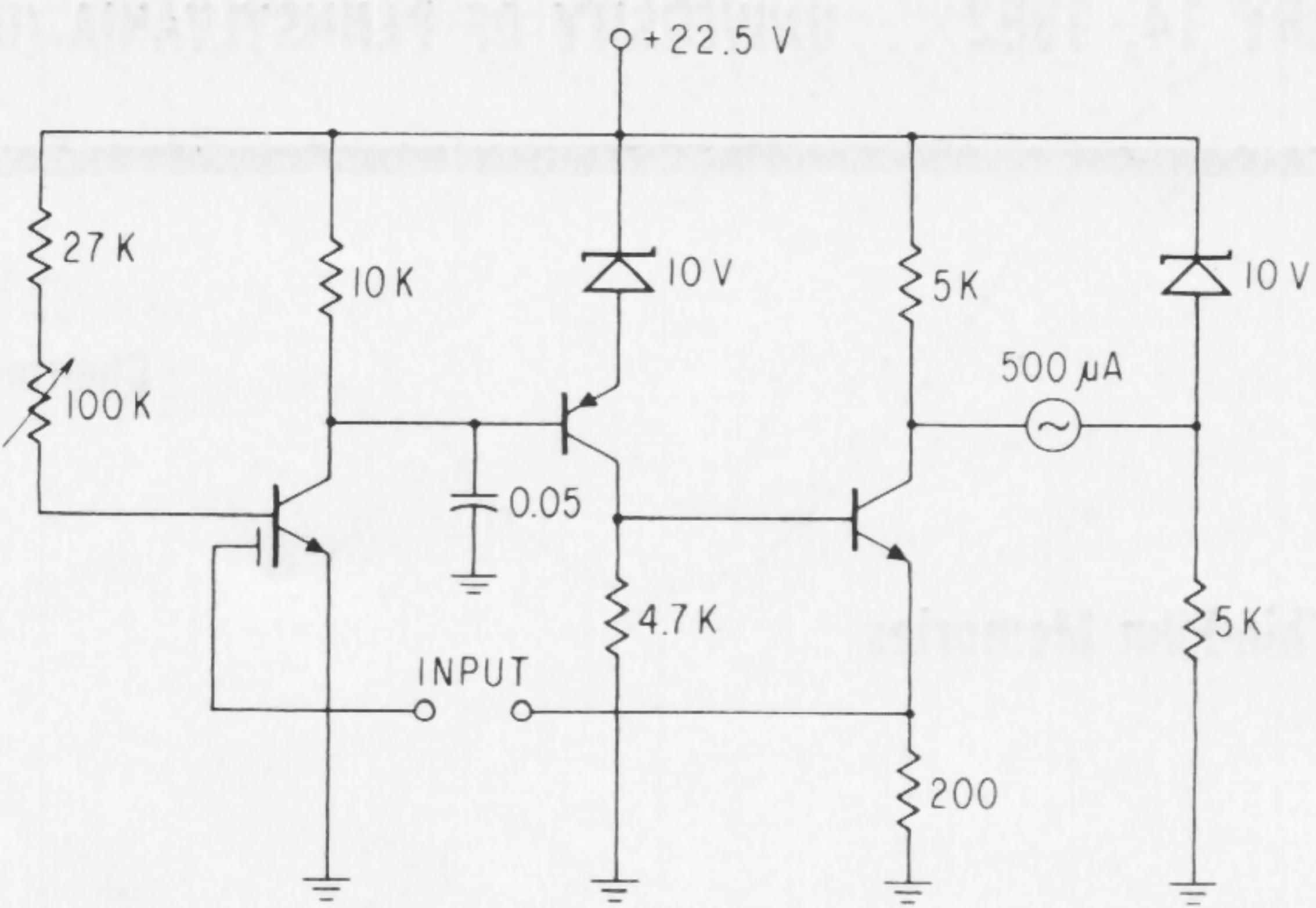


Figure 3—SCT electrometer. This circuit is feedback stabilized for unity voltage gain. The sensitivity of the electrometer is then controlled by changing the size of the 200-ohm resistor.

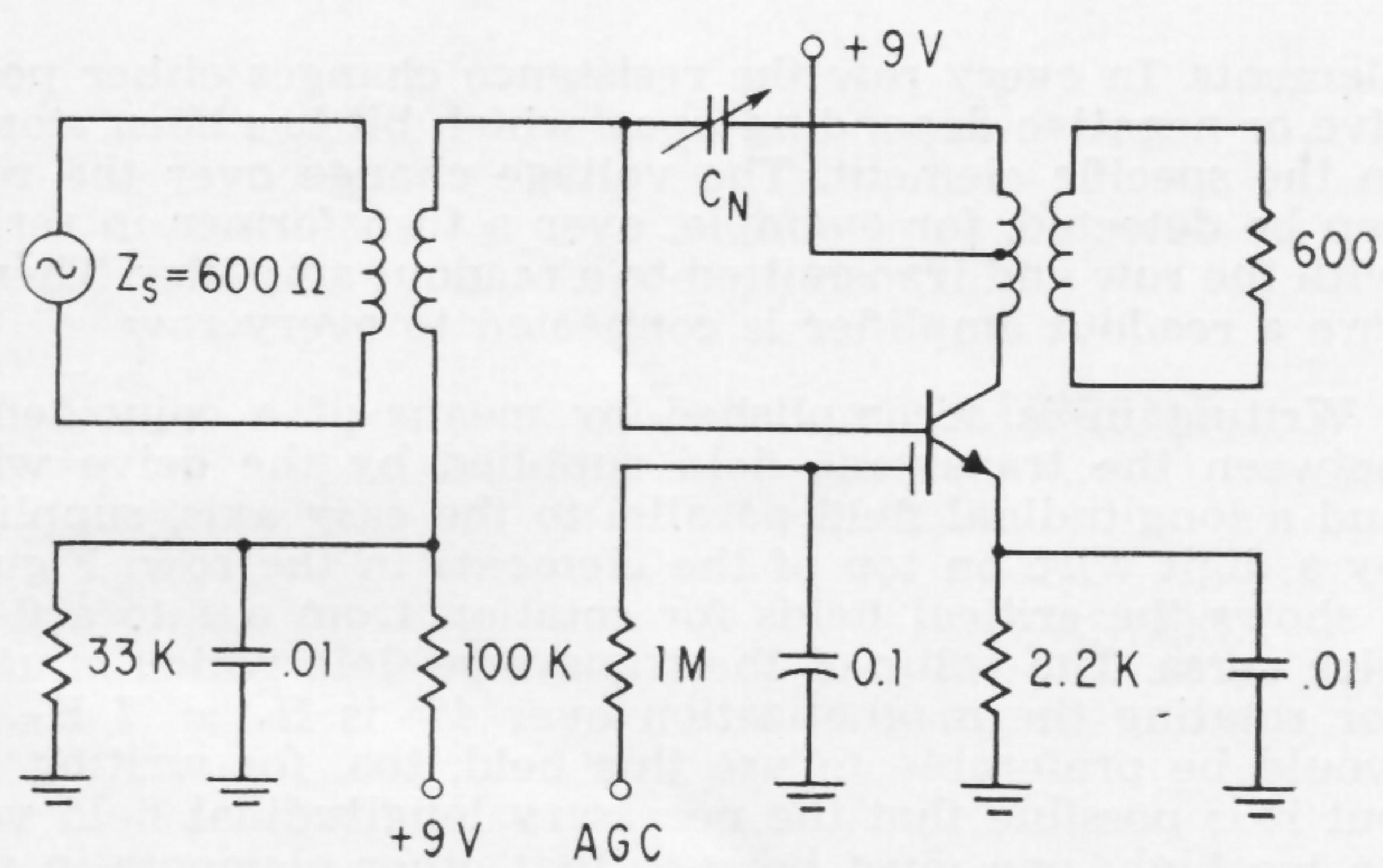


Figure 4—Gain-controlled if amplifier. Amplification of the if frequency is accomplished by using the SCT as a transistor amplifier. Gain control is applied through the high-impedance grid electrode.

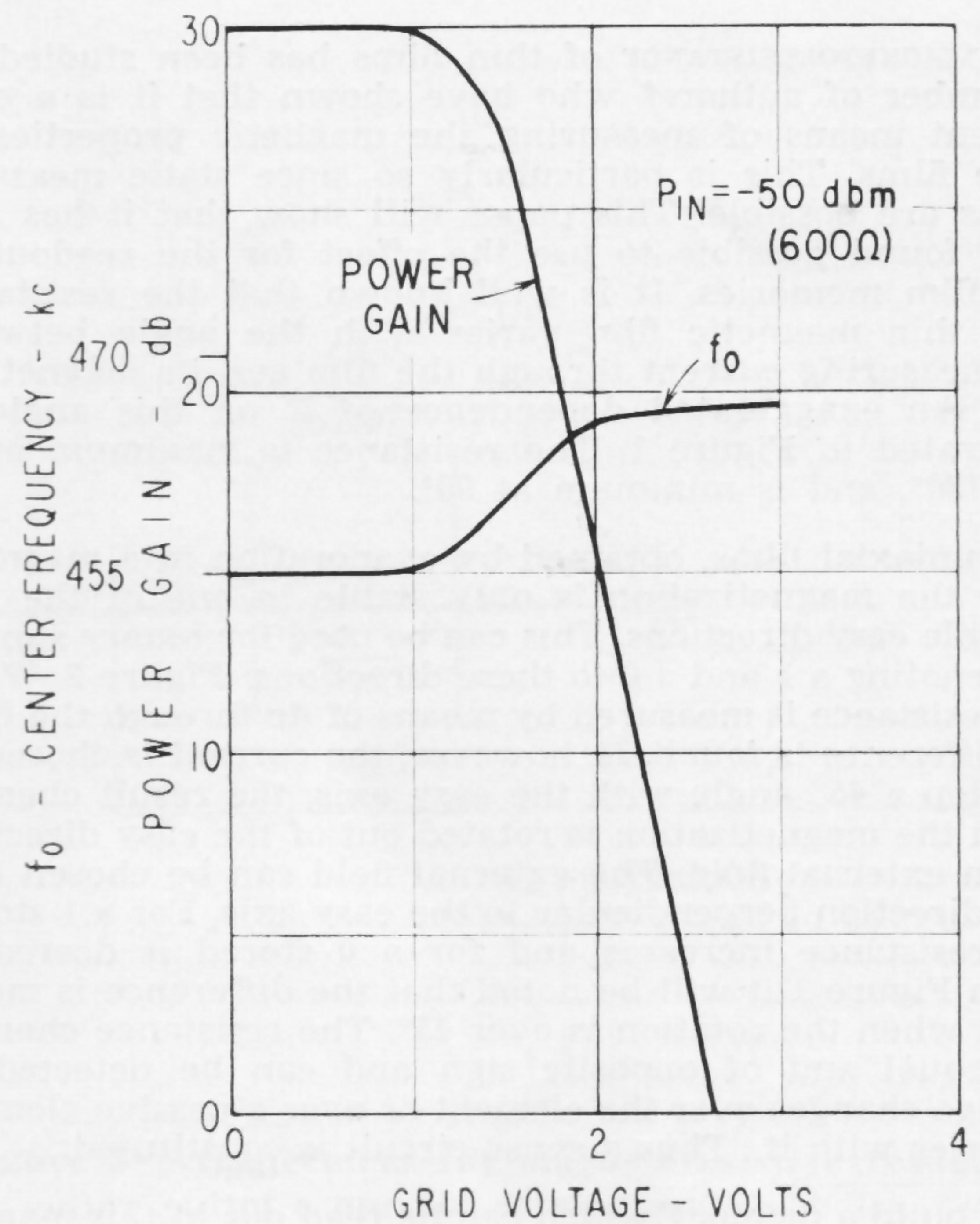


Figure 5—Gain control characteristics of if amplifier.

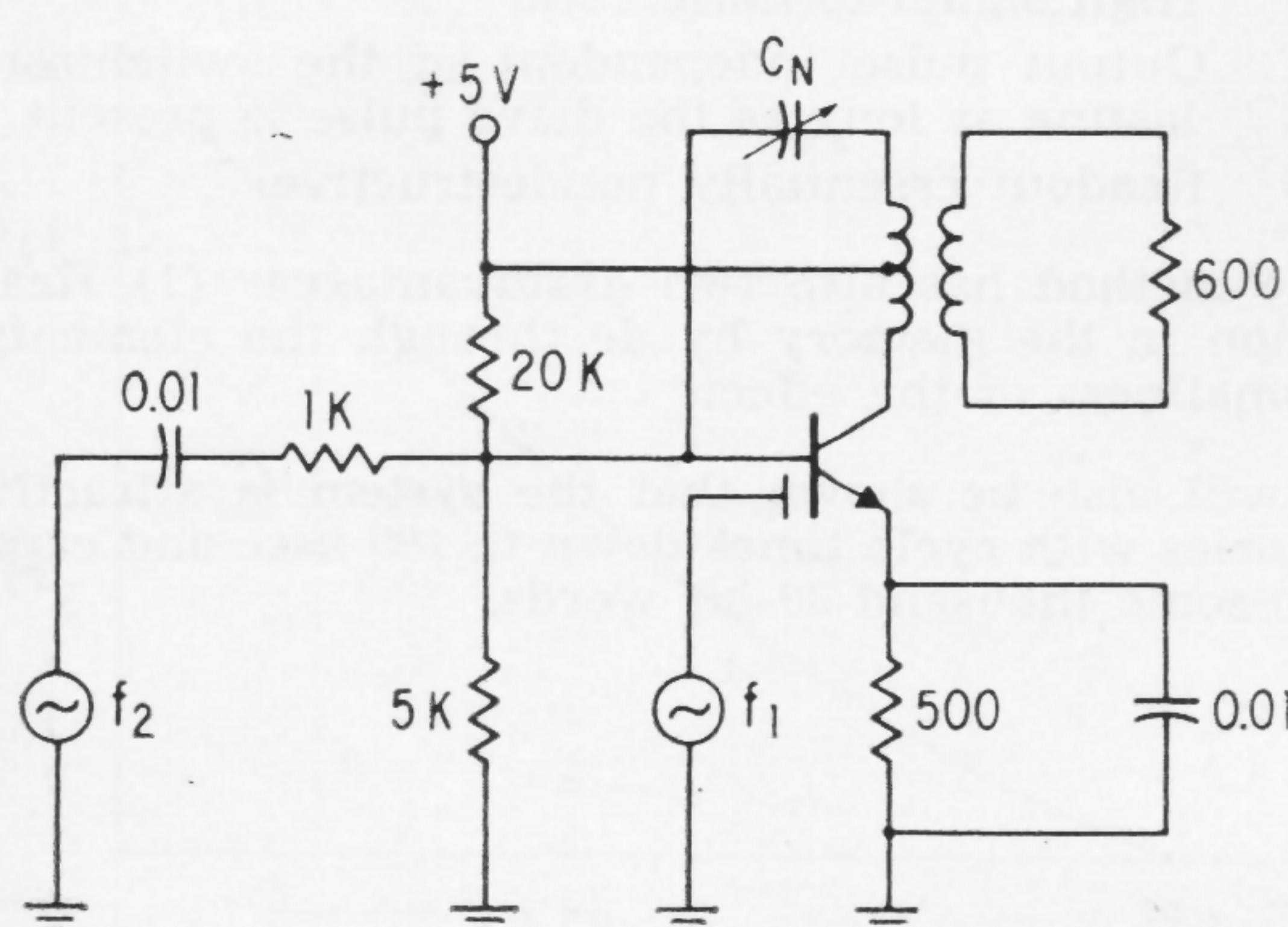


Figure 6—SCT mixer. Frequencies  $f_1$  and  $f_2$  are mixed in the SCT to obtain an output at the difference frequency of 455 kc.

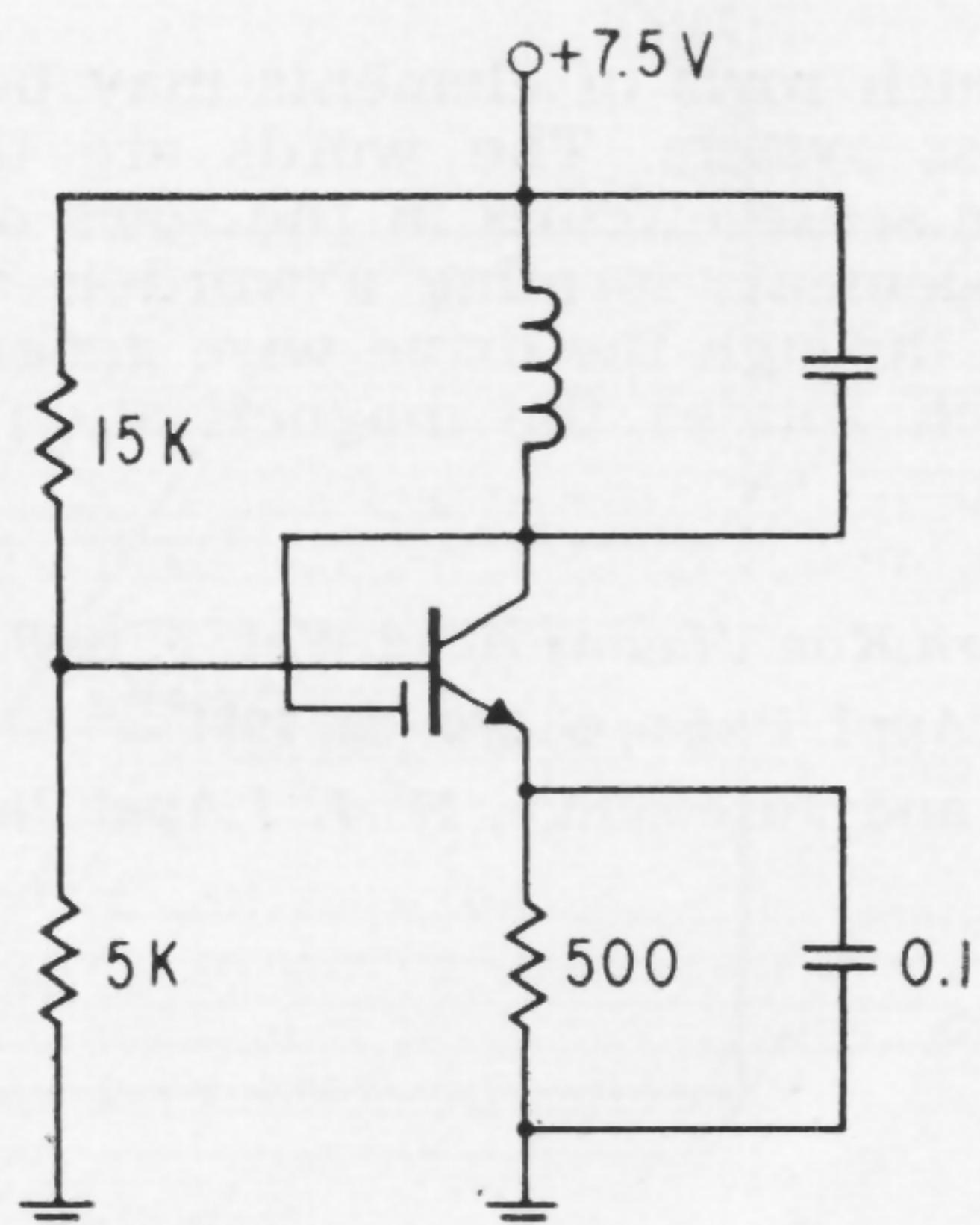


Figure 7—SCT oscillator. The noninverting amplification of the SCT is used to obtain oscillation with a very simple circuit configuration.

## SESSION IV: Memory

Chairman: R. H. Baker

MIT Lincoln Laboratory, Lexington, Mass.

## WA 4.1: Magnetoresistive Readout of Thin-Film Memories

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THE MAGNETORESISTANCE of thin films has been studied by a number of authors\* who have shown that it is a convenient means of measuring the magnetic properties of these films. This is particularly so since static measurements are possible. This paper will show that it has also been found possible to use the effect for the readout of thin-film memories. It is well known that the resistance of a thin magnetic film varies with the angle between the measuring current through the film and its magnetization. An exaggerated dependence of  $R$  on this angle is illustrated in Figure 1. The resistance is maximum at  $0^\circ$  and  $180^\circ$ , and is minimum at  $90^\circ$ .

In uniaxial films, obtained by evaporation in a magnetic field, the magnetization is only stable in one of the two possible easy directions. This can be used for binary storage by denoting a 1 and a 0 to these directions; Figure 2. When the resistance is measured by means of dc through the film, no difference is found. If, however, the current is chosen to develop a  $45^\circ$  angle with the easy axis, the result changes when the magnetization is rotated out of the easy direction by an external field. The external field can be chosen best in a direction perpendicular to the easy axis. For a 1 stored the resistance increases and for a 0 stored it decreases. From Figure 1 it will be noted that the difference is maximum when the rotation is over  $45^\circ$ . The resistance changes are equal and of opposite sign and can be detected as voltage changes over the element or over a passive element in series with it. Thus a sense circuit is constituted.

To build a memory which can be read out in this manner a number of magnetic film elements must be connected electrically and a current supplied through them at  $45^\circ$  to the easy direction. Figure 3 shows a possible arrangement. The transverse field should be applied through a drive wire on top of the element. The drive wire is parallel to the easy direction and at right angles to the line connecting the elements to reduce inductive coupling between the drive wire and the sense circuit.

A matrix of such rows of elements may be operated in the word-address system. The words are then lying in columns and the sense circuits in the rows of the matrix. On top of the elements forming a word is a drive wire. A current pulse through the drive wire generates a transverse field which rotates the magnetization of all these

elements. In every row the resistance changes either positive or negative depending upon which bit has been stored in the specific element. The voltage change over the row can be detected, for example, over a transformer in series with the row and transmitted to a readout amplifier. Therefore a readout amplifier is connected to every row.

Writing in is accomplished by means of a coincidence between the transverse field supplied by the drive wire and a longitudinal field parallel to the easy axis, supplied by a digit wire on top of the elements in the row. Figure 4 shows the critical fields for rotation from a 1 to a 0 or vice versa. The value of the transverse field which is used for rotating the magnetization over  $45^\circ$  is  $H_T = .7 H_K$ . It would be preferable to use this field, too, for writing in, but it is possible that the necessary longitudinal field will be too high; one must be sure that other elements in the row do not alter their information due to creeping of domain walls. If this creeping occurs, a higher transverse field should be used for writing so that a smaller longitudinal field may be applied.

It is possible to build a memory by placing a number of matrices upon each other, as indicated in Figure 5, where the same rows of the different matrices are connected to one readout amplifier. The optimum number of matrices is not yet known, but it appears that we can obtain about 30 matrices with each 30 elements in a row.

Below are typical results from a matrix with 12 elements in a row—element size being  $.5 \times .5 \text{ mm}$ —

- (1) Drive current pulse =  $.3 \text{ a}$ , 50 nsec
- (2) Digit current pulse =  $.1 \text{ a}$
- (3) Output pulse =  $2 \text{ mv}$ , 100 nsec
- (4) Cycle time = 200 nsec

The system has certain advantages over the more conventional magnetic readout method, noted below:

- (1) Small elements and high bit densities
- (2) High signal-to-noise ratio
- (3) Output pulse independent of the switching time, lasting as long as the drive pulse is present
- (4) Readout essentially nondestructive

The method has also two disadvantages: (1) Heat dissipation in the memory by dc through the elements, and (2) smallness of the effect.

It will also be shown that the system is attractive for memories with cycle times down to 100 nsec and capacities up to some thousand 30-bit words.

\* Dupré, A., *Verh.Kon.Vlaams.Acad Wet*, 5, 1959.

West, F. G., *J.Appl. Phys.*, p. 290; 32, 1961

Coren, R. L., and Juretschke, H. J. *J.Appl.Phys.*, p. 292; 32, 1961.

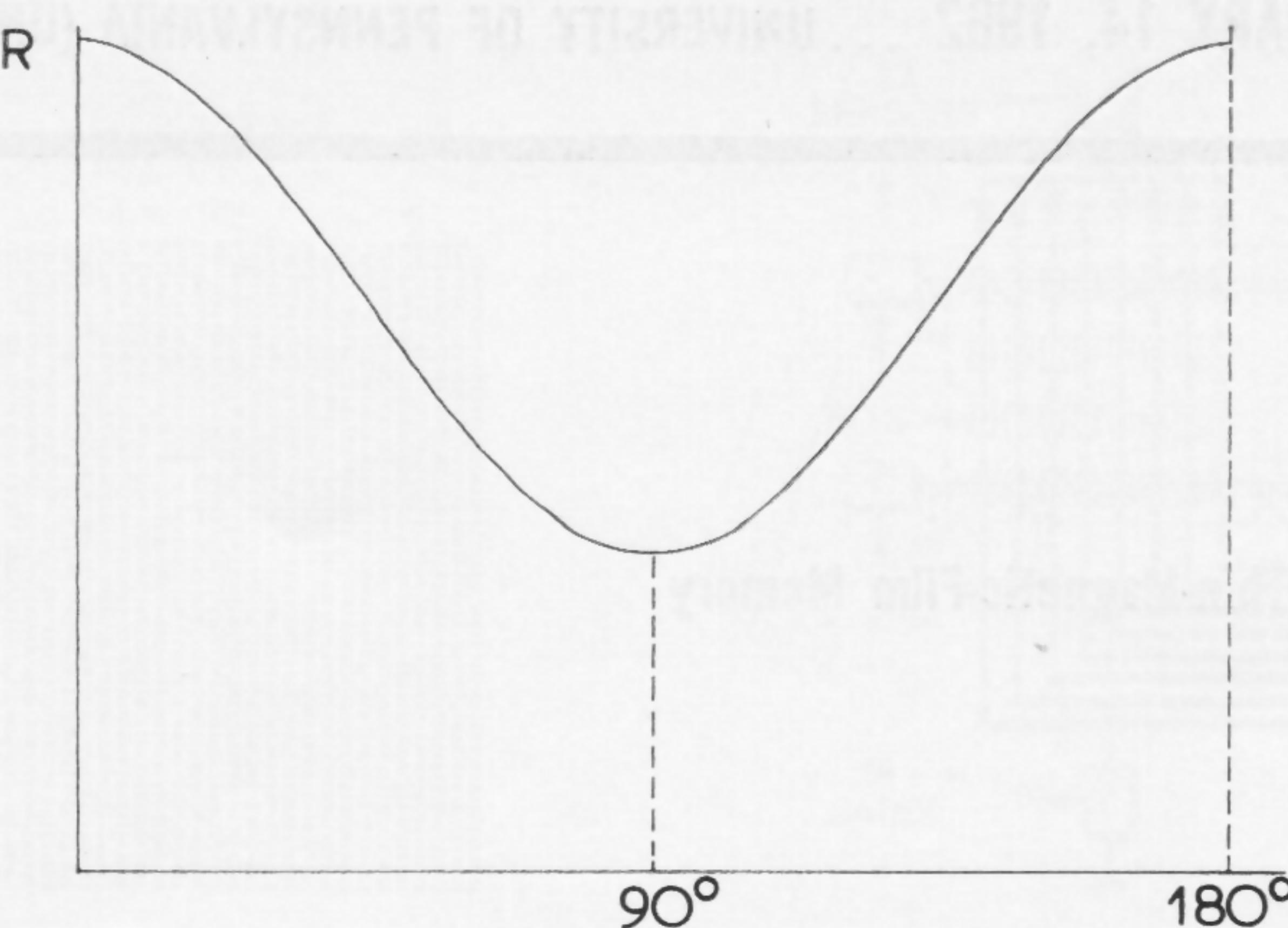


Figure 1—Resistance of a thin film as a function of the angle between the measuring current and the magnetization (exaggerated in the vertical sense).

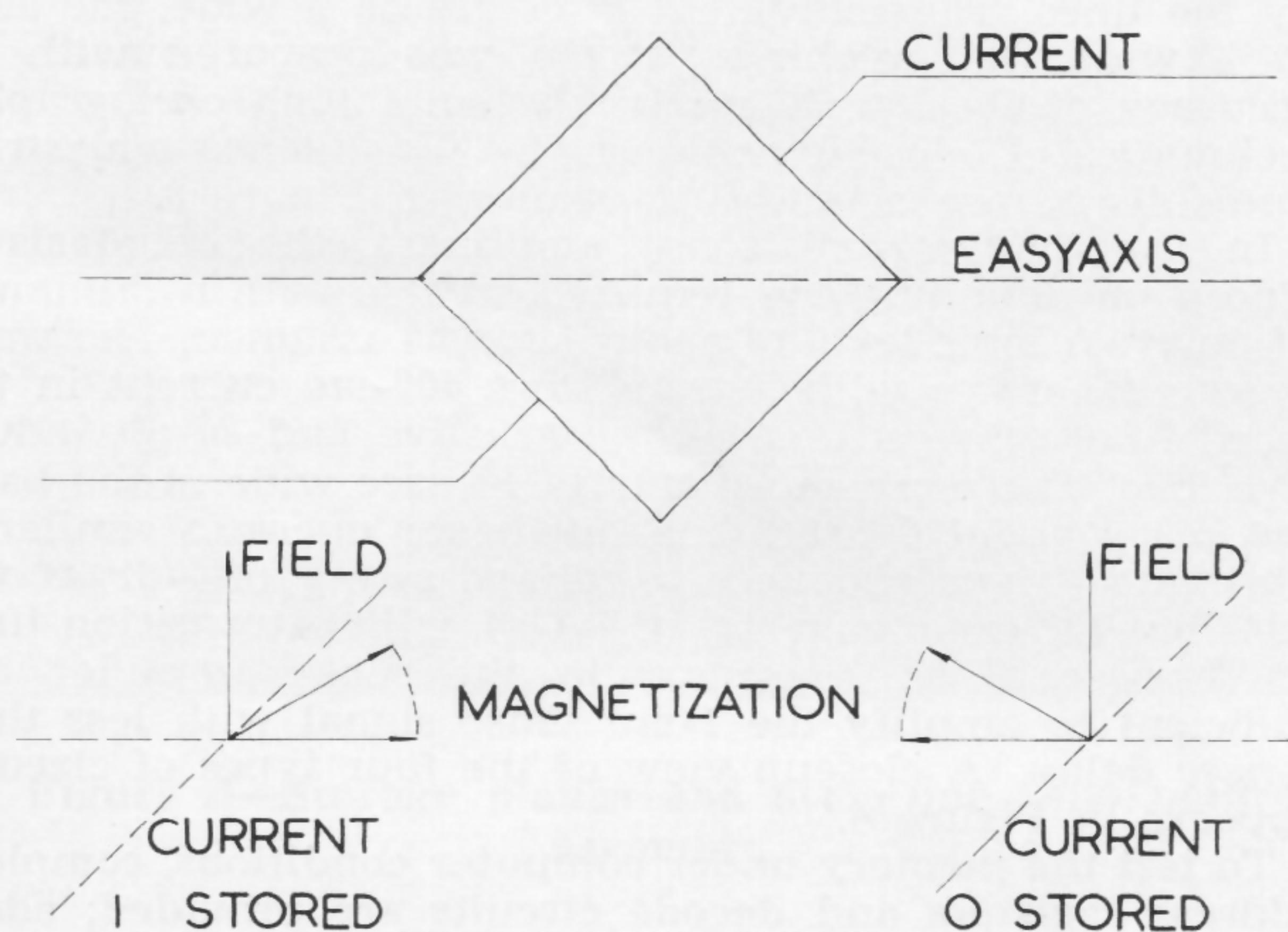


Figure 2—Illustration of magnetoresistive readout of a single bit.

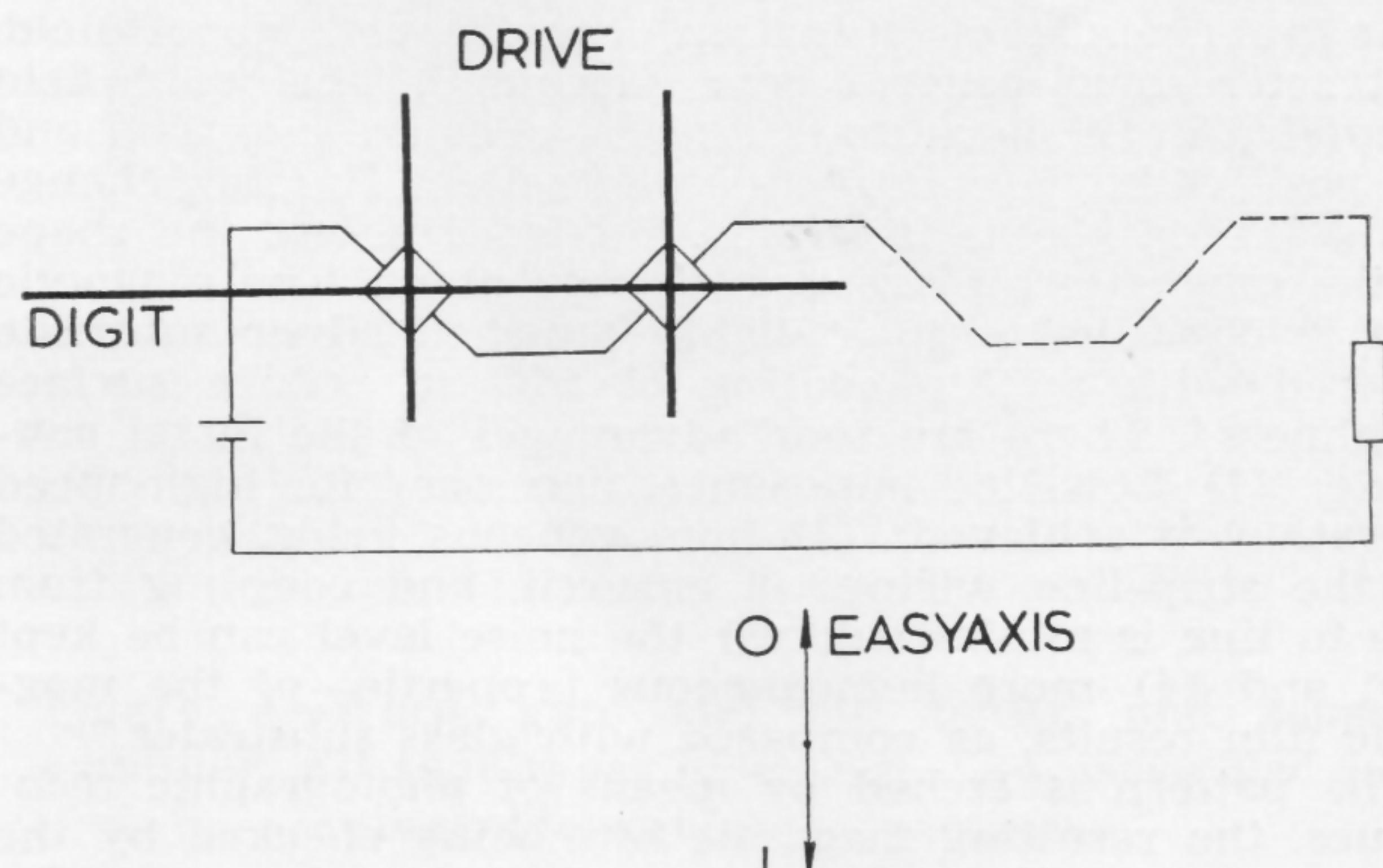


Figure 3—Arrangement for magnetoresistive readout of a number of elements.

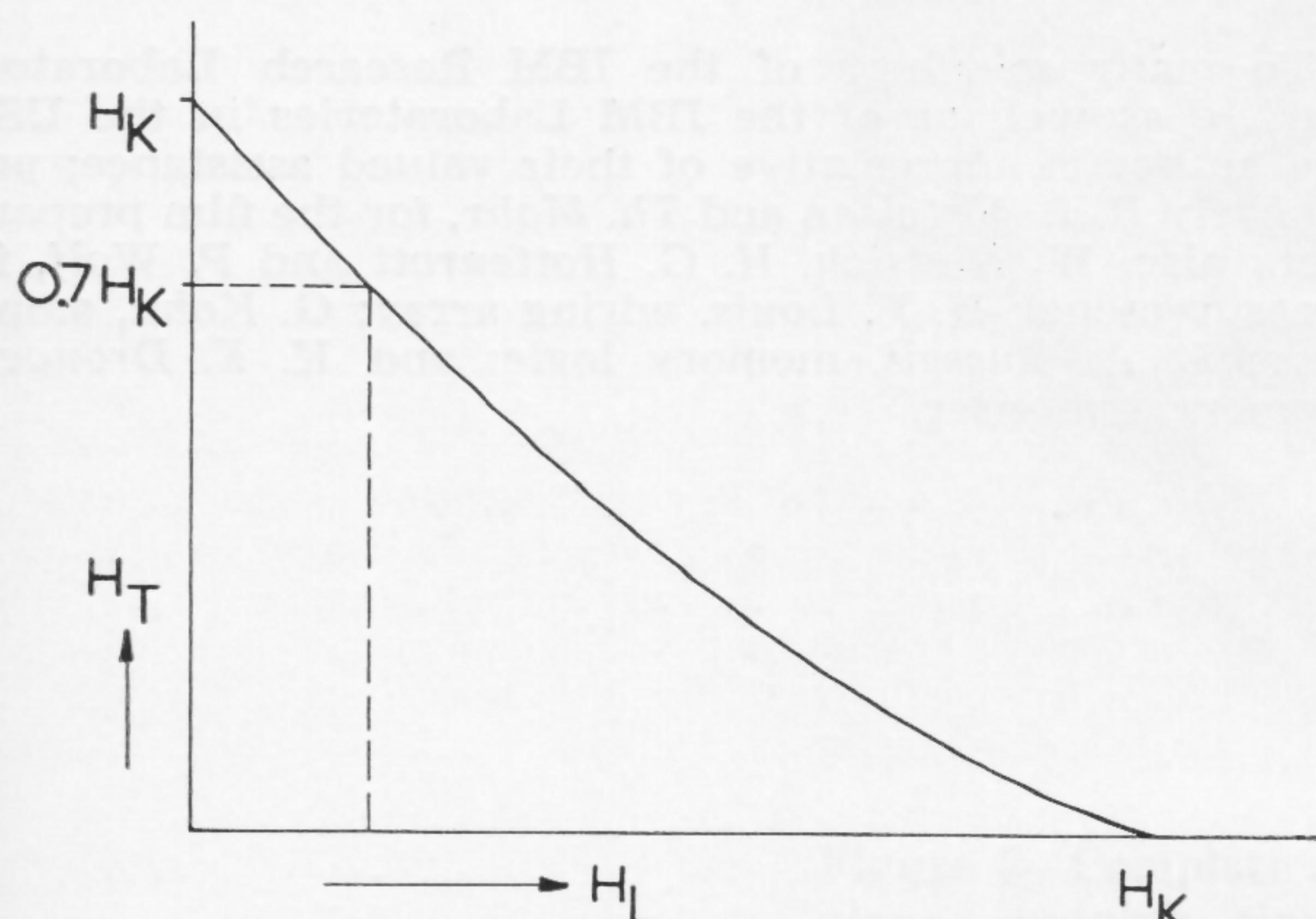


Figure 4—Critical transverse and longitudinal fields for writing information into a thin film by rotation.

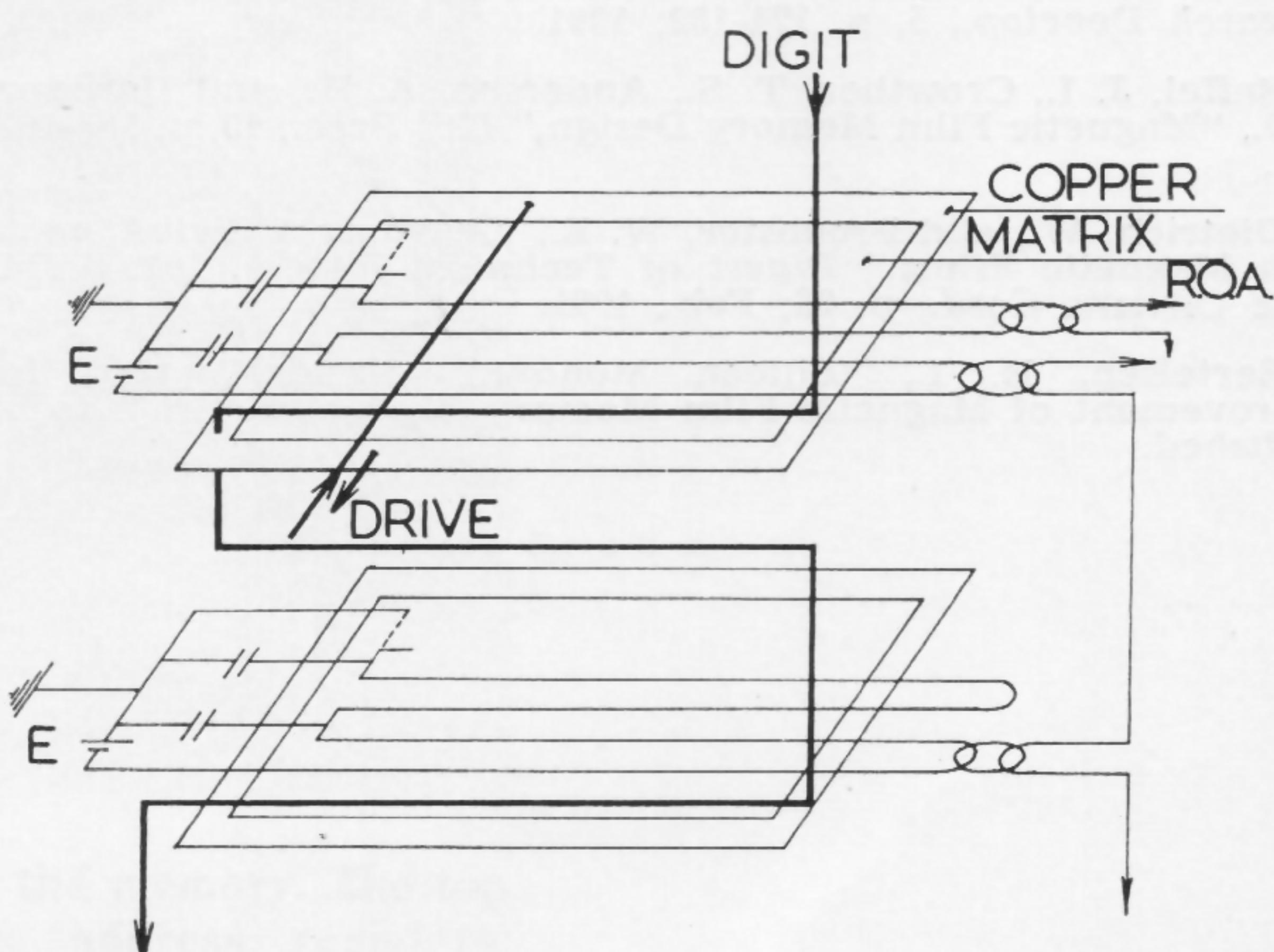


Figure 5—A thin-film memory featuring readout by means of the magnetoresistive effect.

## SESSION IV: Memory

## WA 4.2: The Design of a High-Speed Thin-Magnetic-Film Memory

W. E. Proebster

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Adliswil-Zurich, Switzerland

THIS PAPER will outline the design of a magnetic film memory which has been found to be—still at a capacity reasonable for computer use—considerably faster than existing random-access destructive read memories<sup>1</sup>.

The target is a cycle time of 100 nsec at a capacity of 256 words of 72 bits each, resulting in a total of 18,432 bits. To meet this objective it was necessary to investigate and optimize the performance of the memory element itself, as well as that of the associated components and circuits.

As a principle of operation, the 2D orthogonal field, destructive-read concept was selected<sup>2,3</sup>. The word field is applied in the hard direction, the negative bias field and the positive bit field in the easy direction. The flux change along the easy axis is sensed. Figure 1 shows the shape of the magnetic bit and one storage plane. The magnetic film is deposited onto a highly polished silver substrate covered with a thin coating of SiO to reduce surface roughness<sup>4</sup>. There are four advantages of the metal substrate: (1) Low-line impedance, necessary for high-speed operation, is achieved; (2) homogeneous fields, generated by the strip-line wiring, is ensured, and coupling from line to line is minimized; (3) the noise level can be kept low; and (4) more homogeneous properties of the magnetic film results, as compared with glass substrates.

The pattern is etched by means of photographic techniques, the resulting magnetic bits being checked by the magneto-optical Kerr-effect. Characteristic values are: Coercive force  $H_c \approx 2$  oe, minimum word field  $H_w \approx 4$  oe, minimum bit field  $H_b \approx .5$  oe, deviation of the easy axis from the edge line  $\Delta\alpha \leq \pm 3^\circ$ . Pulse measurements result in the following typical values: Minimum word current  $I_w = 400$  ma; minimum bit current  $I_b = 150$  ma; and output pulse  $\sim 1$  mv at 10-nsec basewidth.

Array wiring with drivers and sense amplifiers is illustrated in Figure 2. Eight storage planes form the planar

storage array with two planes in the bit dimension, and four planes in the word dimension. The sequence of the wiring above the storage planes is sense lines, word lines, bit lines. All lines are etched out of copper clad, epoxy fiber glass. The strip lines are slotted to minimize eddy currents by the switching film and by the fields generated by the lines. The individual lines are 55  $\mu$  wide, the slots 45  $\mu$  wide. The etching pattern was prepared with an accuracy of 50  $\mu$  at 20-cm length employing cartographic techniques. A closeup view of the film planes and strip-line foils before assembly is shown in Figure 3.

In the drivers and sense amplifiers, the emphasis is placed on obtaining the required signals with a minimum of delay. A logic level of about 1 v was assumed. The word driver generates with 3 transistors 400-ma current in the word line, representing 5-ohm resistive and 20-nh inductive load. The word pulse is only 10-nsec wide at the base; the delay about 6 nsec. The bit driver operates similarly. The gate driver produces a voltage swing of  $\sim 6$  v at the gate bus having a capacity of  $\sim 1$  nf, with a transition time of 20 nsec. Five transistors in the sense amplifier are sufficient to amplify the 1-mv sense signal with less than 5-nsec delay. A closeup view of the four types of circuits appears in Figure 4.

To test the memory under computer conditions, complete address registers and decode circuits are provided; additionally, an exerciser for the operation and check of a number of information circuits has been included. Figure 5 shows the complete assembly of the memory.

To test the basic ideas, an experimental single plane memory with 32 x 21 bits has been constructed and operated successfully with cycle times as short as 100 nsec. The full size memory is under test. Initial results indicate that a cycle time of 100 nsec is possible with an access time of 60 nsec.

## Acknowledgments

To many members of the IBM Research Laboratory, Zurich, as well as of the IBM Laboratories in the USA, the author is appreciative of their valued assistance; particularly *B. I. Bertelsen* and *Th. Mohr*, for the film preparation; also, *W. Dietrich*, *H. G. Hottenrott* and *P. Wolf*, for measurements; *H. P. Louis*, wiring array; *G. Kohn*, amplifiers; *L. A. Russell*, memory logic; and *K. E. Drangeid*, memory exerciser.

<sup>1</sup> Rhodes, W. H., Russell, L. A., Sakalay, F. E., and Whalen, R. M., "A 0.7-Microsecond Ferrite Core Memory," *IBM J. Research Develop.*, 5, p. 174-182; 1961.

<sup>2</sup> Raffel, J. I., Crowther, T. S., Anderson, A. H., and Herndon, T. O., "Magnetic Film Memory Design," *IRE Proc.*, 49, p. 155-164; 1961.

<sup>3</sup> Dietrich, W., and Proebster, W. E., "A Study of Switching in Thin Magnetic Films," *Digest of Technical Papers, Int. Solid-State Circuits Conf.*, p. 66; Feb., 1961.

<sup>4</sup> Bertelsen, B. I., "Silicon Monoxide Under-Coating for Improvement of Magnetic Film Memory Characteristics"; to be published.

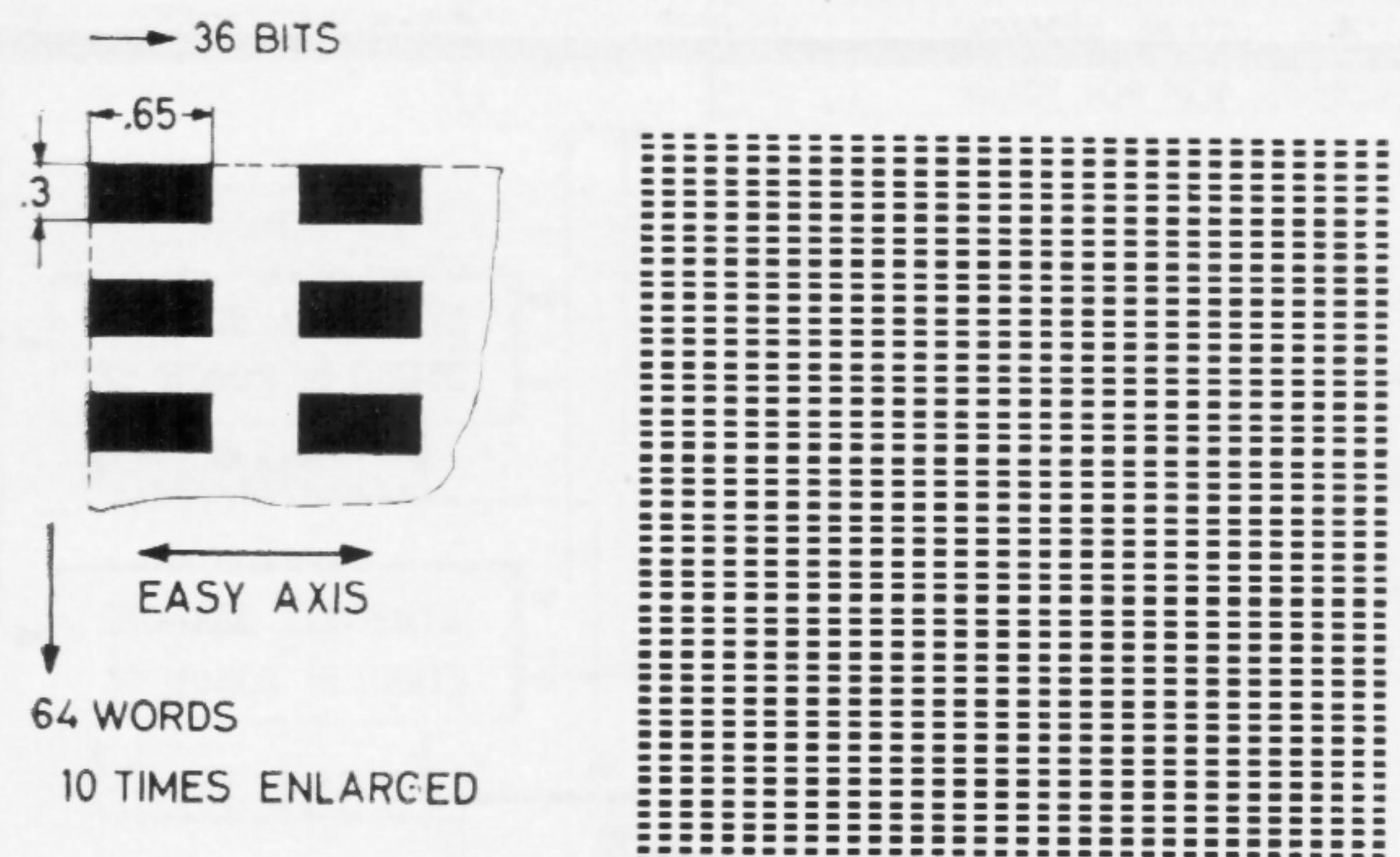


Figure 1—Shape of magnetic bit and storage plane. Film size is  $.3 \times .65$  mm; film thickness  $\sim 50$  nm ( $1$  nm  $= 10^{-9}$  m). Metal substrate size is  $5 \times 5$  cm with  $64 \times 36 = 2304$  bits placed on one substrate.

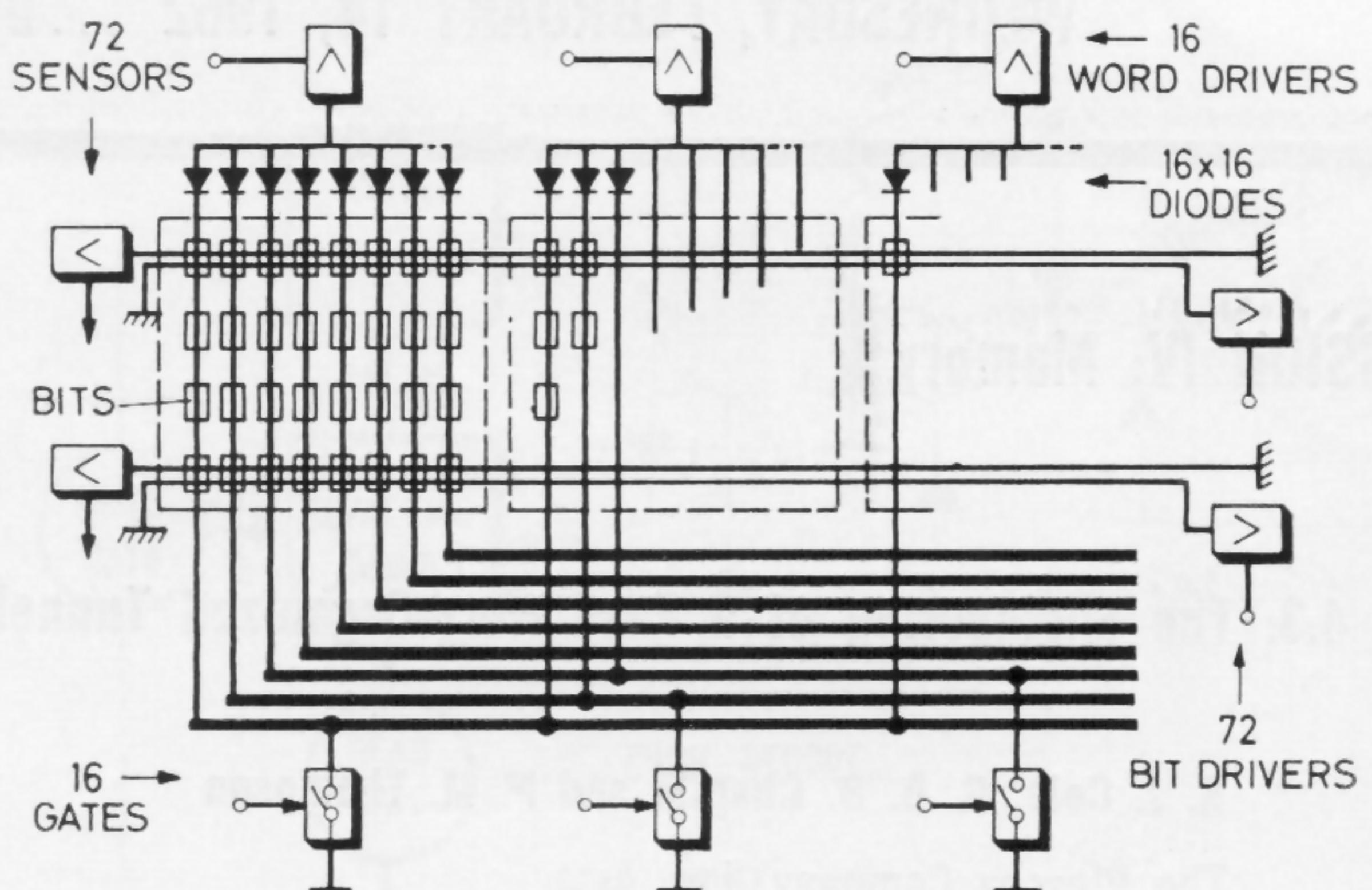


Figure 2—Schematic diagram of array wiring with drivers, decode, and sense amplifiers.

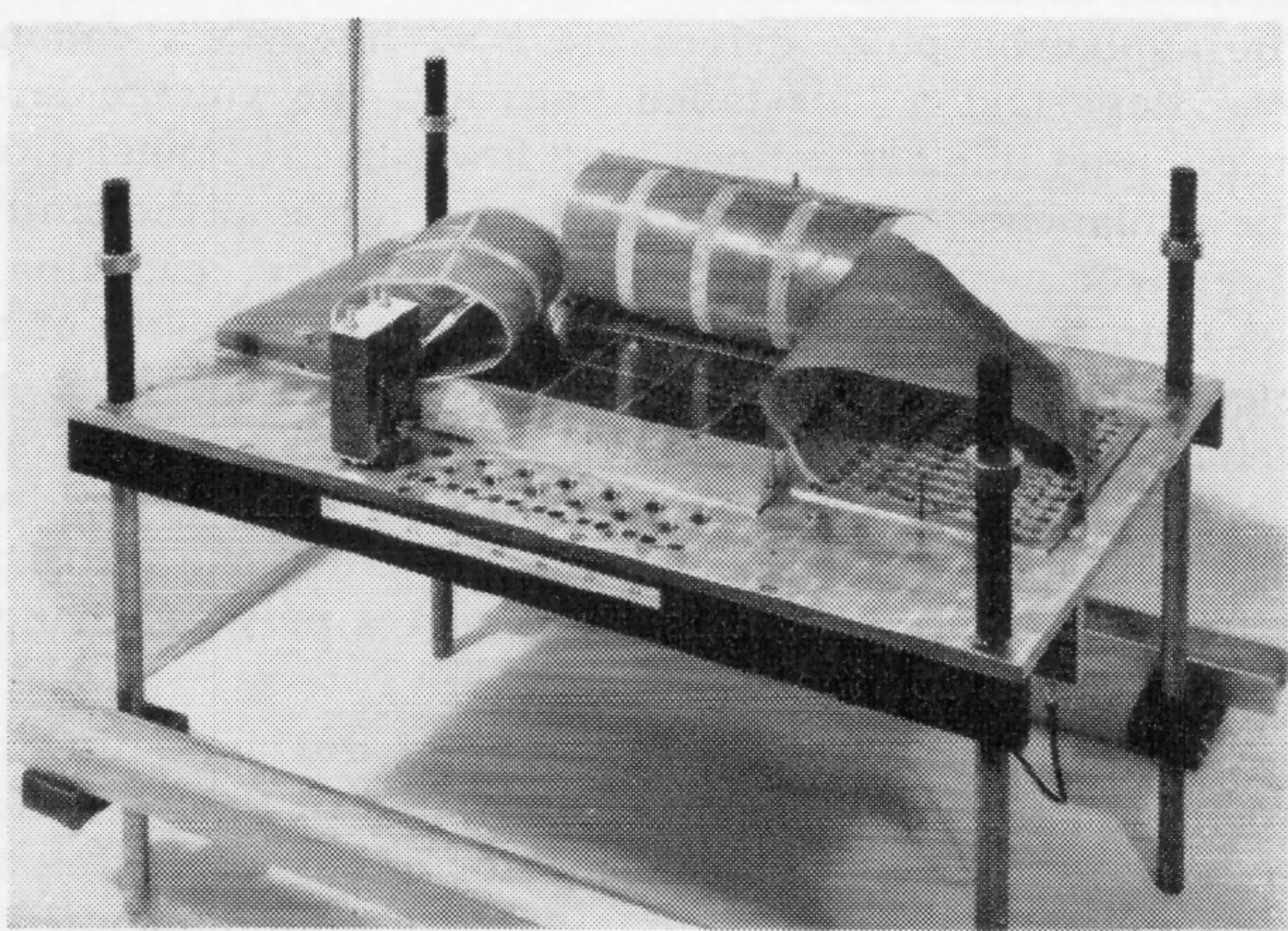


Figure 3—Storage planes and strip-line foils before assembly.

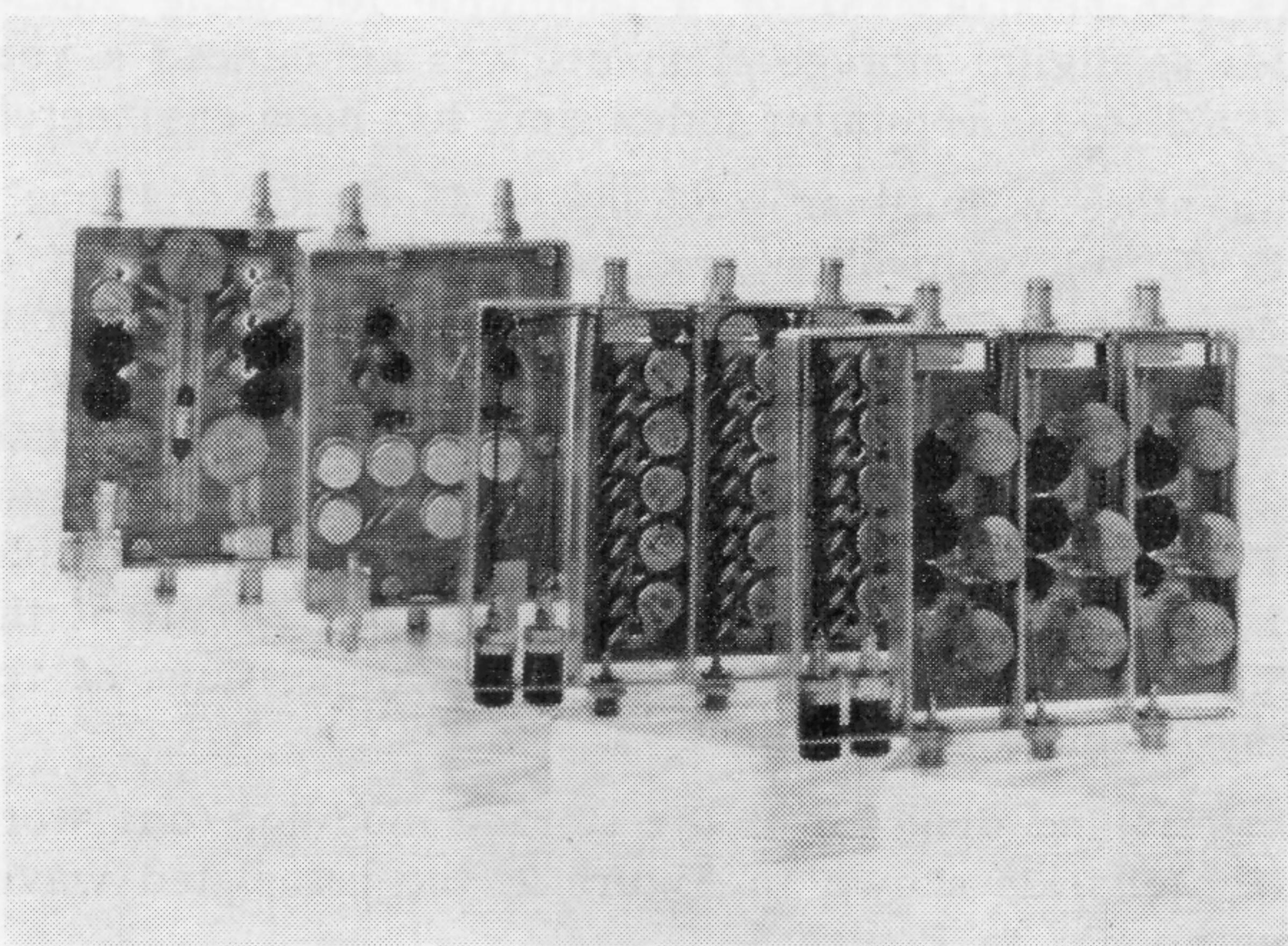


Figure 4—Word, gate and bit driver, and sense amplifier. All four types of circuits are assembled in pluggable miniature package.

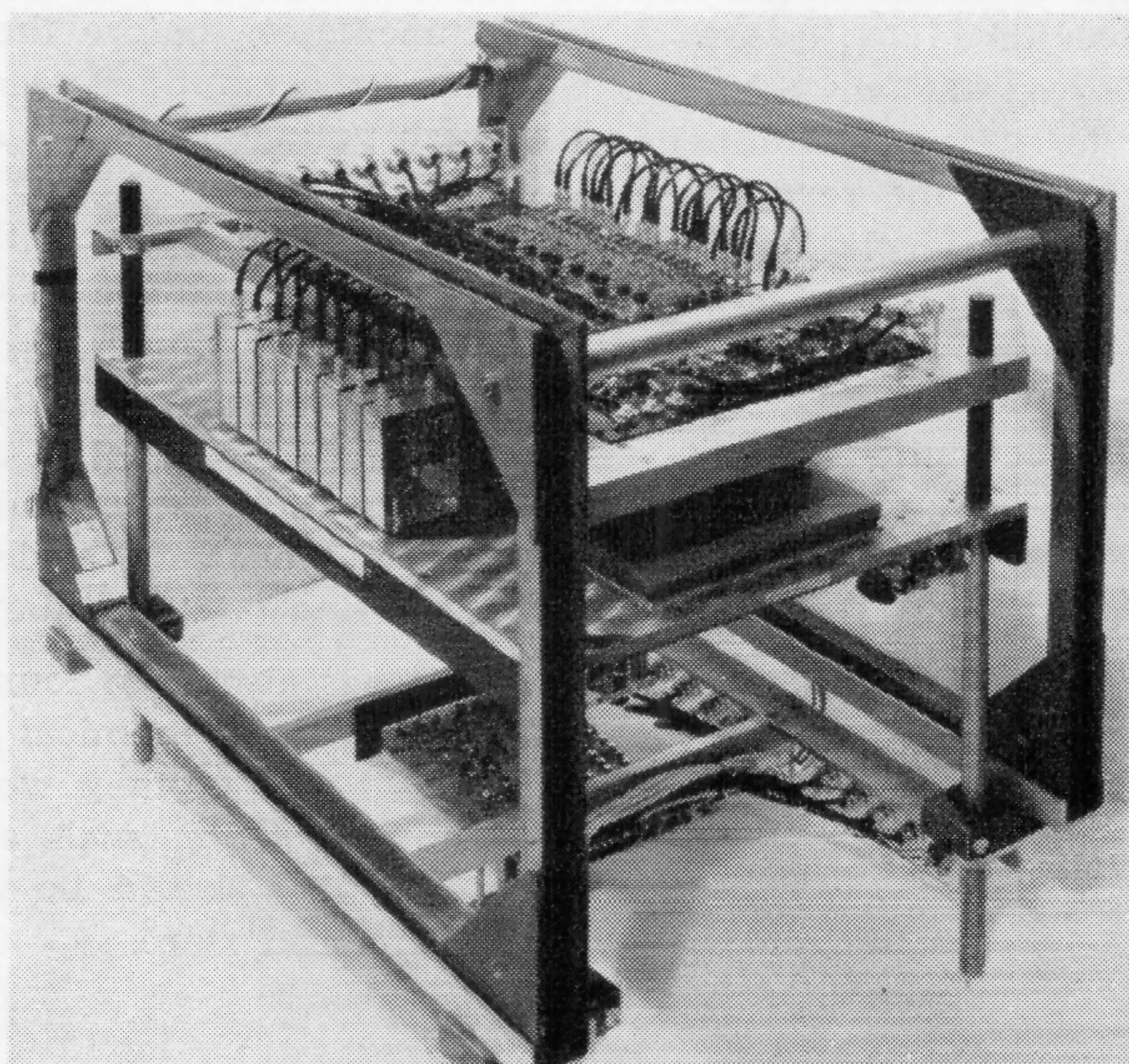


Figure 5—Complete assembly of the memory. The top plane contains timing circuits, address registers, decode circuit for word and gate drivers. The center plane contains storage array, wiring, drivers and amplifiers. The lower plane holds one pluggable information circuit card.

## SESSION IV: Memory

### WA 4.3: The Engineering of a Fast Word-Organized Tunnel-Diode Store

A. J. Cole, G. B. B. Chaplin and P. M. Thompson

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Romsey, Hampshire, England

SINCE THE DEVELOPMENT of a technique for using tunnel diodes as digital storage elements was announced a year ago<sup>1</sup>, a 32-word computer index store has been engineered.

This store is built as modules of 16 digits, and has a fairly flexible control arrangement allowing the start of the separate parts of the cycle to be delayed to correspond with external arithmetic operations, if necessary. Engineering the store involves not only the design of the tunnel-diode storage elements, but also the development of high-speed driving and timing techniques, so that, for example, read pulses arrive at the appropriate digit circuit at the correct time independent of the physical positions of the storage element addressed.

A simplified diagram of the storage module, (one word of 16 digits) is shown in Figure 2; the associated waveforms appear in Figure 3.

Now let us consider a single element. To read, the read line is driven negative .5 v so that if the tunnel diode is in the low voltage state, (storing a 1), the rectifier diode conducts and transmits a pulse down the digit line, where it is detected by the digit circuit. To write a 0, the digit line remains at -.1 v, and to write a 1, is driven to -.6 v. Following this, the tunnel diode is switched to its low-voltage state by a 4-v negative pulse on the write line. Then, when the write line returns to +2 v, the tunnel diode is set into its appropriate state, and the read line and digit line are reset to their quiescent levels. As the read pulse is short, and the digit circuit requires a narrow strobe, a minimum variation must prevail in the time taken for a signal to travel from the control through the selected storage module on to the digit circuit; the technique for achieving this is illustrated in Figure 4, while the read-line drive circuit is shown in Figure 5.

The input from the read pulse line is via a diode which absorbs energy from the line only if the module has been

selected; in this case the avalanche transistor is triggered. The avalanche pulse drives the read line via a common base stage and a long-tailed pair, and the voltage levels on the read line are defined by a low current tunnel diode. The avalanche pulse also sets a tunnel diode at the emitter of the common base stage, which holds the read line at -.5 v until the end of the cycle. The spare collector of the long-tailed pair provides a signal which energizes the write gate, where a similar avalanche transistor generates the pulse for the write line. In this system, the address input is required only when the read avalanche transistor is triggered. Following this, the address may be changed in preparation for the next cycle.

A simplified digit circuit capable of discriminating between a 1 and 0 read signal is illustrated in Figure 6. Here the discriminating level is 1 ma for 5 nsec; resetting the voltage level of the digit line 15 nsec later as shown in Figure 3c.

Transistor  $J_1$  in Figure 6 has two functions; as a common base amplifier for read signals, and also as an emitter follower for setting the voltage levels of the digit line. The collector of  $J_1$  is connected to long-tailed pair  $J_2 J_3$ , which amplifies the read pulse with respect to the digit line level immediately before the pulse. Tunnel diode  $E_2$  discriminates the amplified read-pulse level, and switches into the high voltage state if a 1 signal is present. The output current of  $E_2$  provides the digit output signal via  $J_4 J_5$  and  $J_6$ , and if required, sets the digit line voltage level via the diode gate, the tunnel diode clamp  $E_1$ , and transistor  $J_1$ .

The read-line drive circuit, and the digit circuit have been given as examples of the circuit techniques used in the store. The control circuits use similar avalanche transistors and gates, and also tunnel-diode staticizers, in conjunction with a delay line constructed as a printed strip line on a standard printed-circuit board.

It has also been found that tunnel diodes can form the basis of an economical small fast store. However, although it is felt that they would not be economical for a high capacity store, such as a computer working store, the techniques should be valuable when constructing a large high-speed store.

<sup>1</sup> Chaplin, G. B. B. and Thompson, P. N., "A Fast Word-Organized Tunnel-Diode Memory Using Voltage-Mode Selection," *Digest of Technical Papers, Int. Solid-State Circuits Conf.*, p. 40; Feb. 1961.

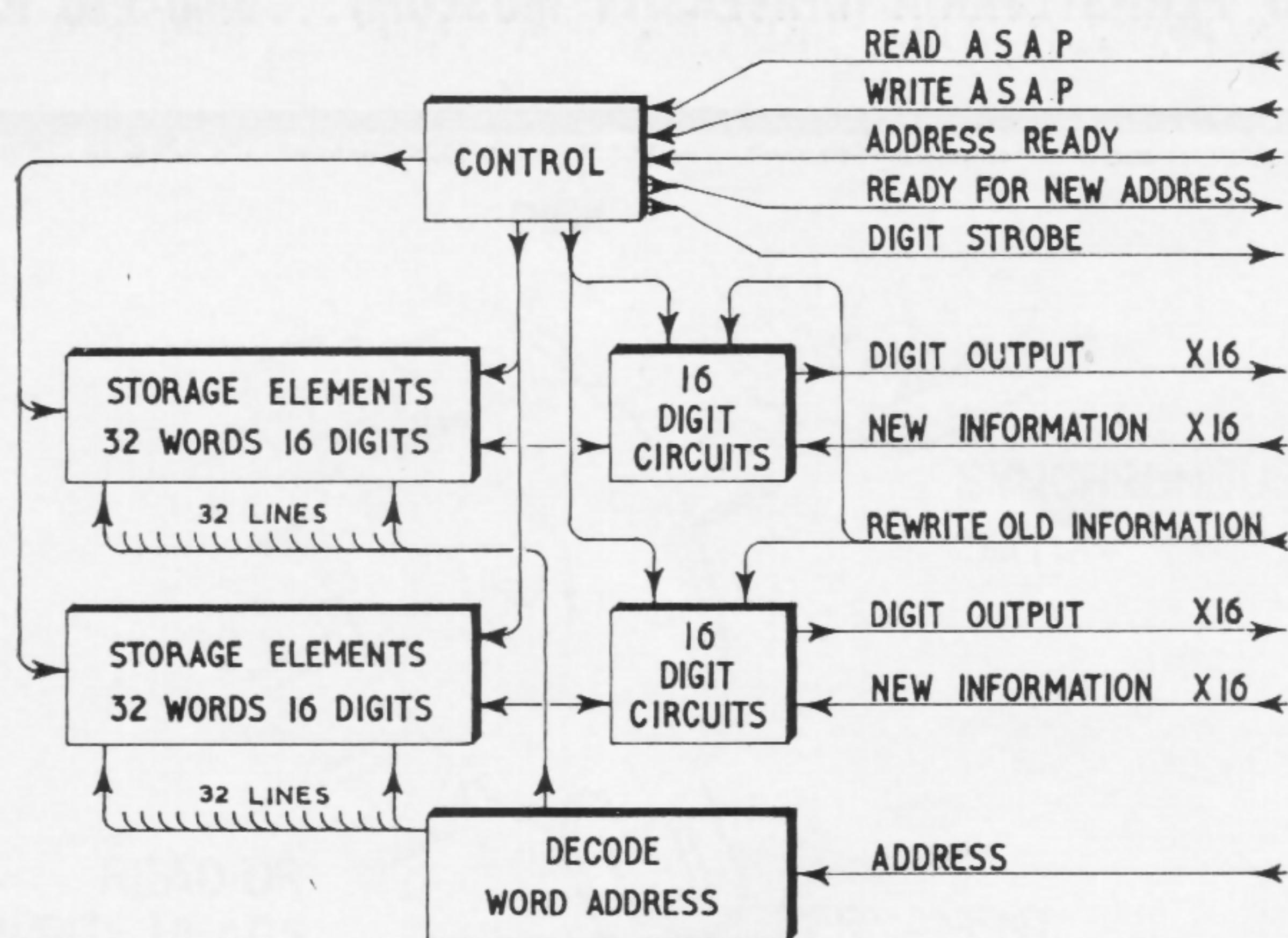


Figure 1—Simplified block diagram of complete tunnel diode store. Shown are 32 words of 32 digits, an average capacity for this technique.

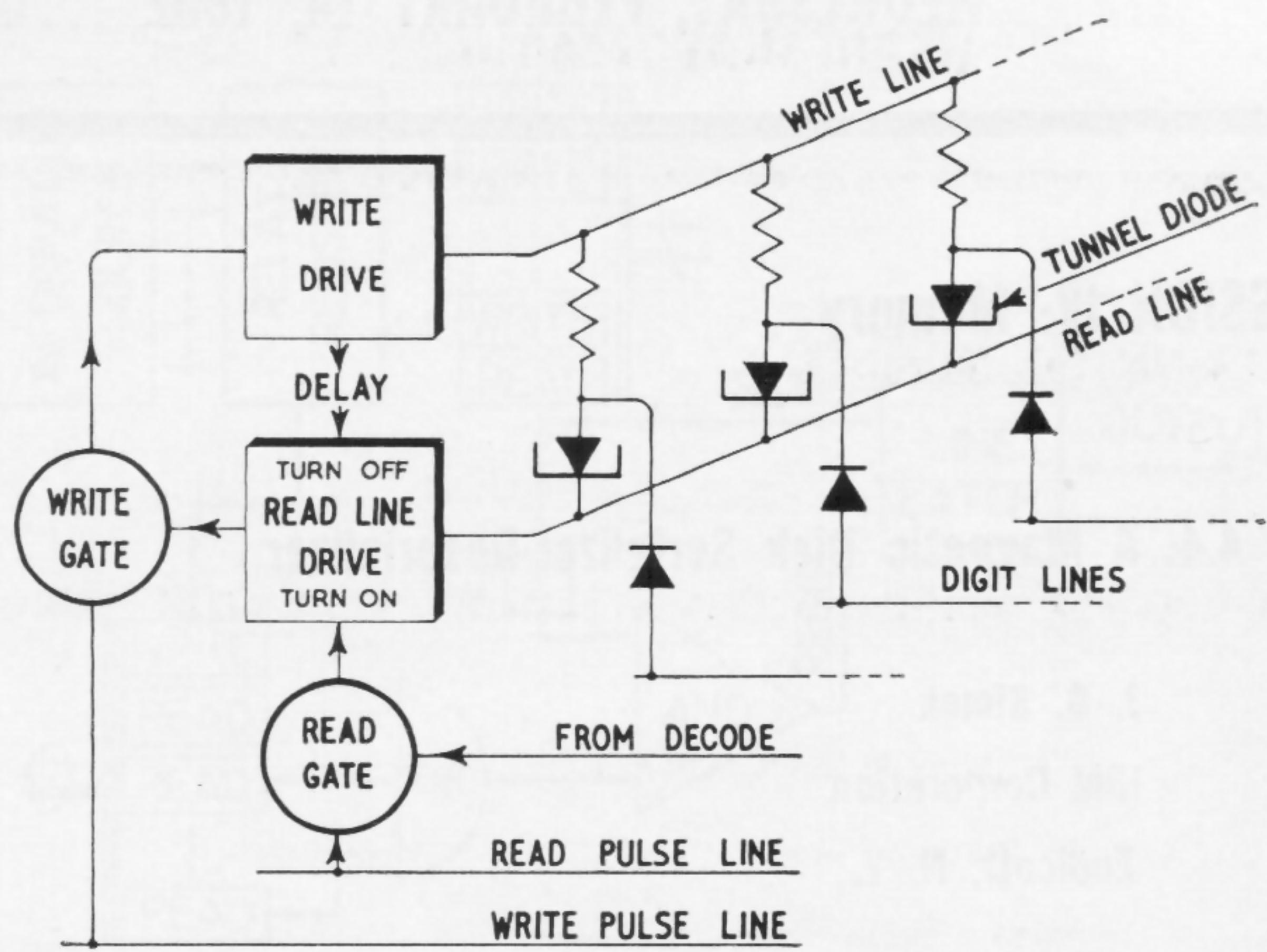


Figure 2—Storage module consisting of 16 digits in a single word complete with drive circuits. Storage element consists of tunnel diode, resistor, and rectifier diode.

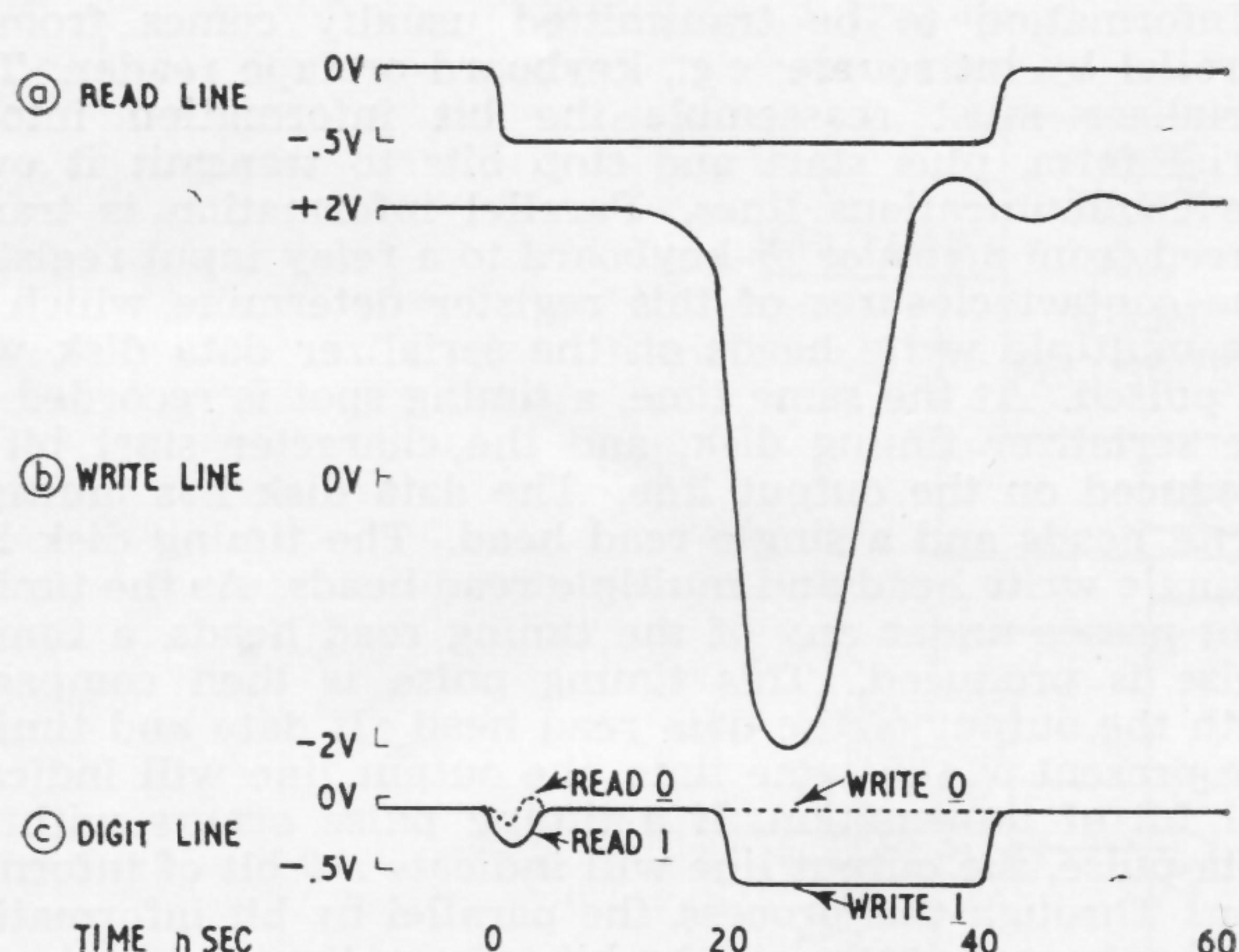


Figure 3—Timing diagram for storage element.

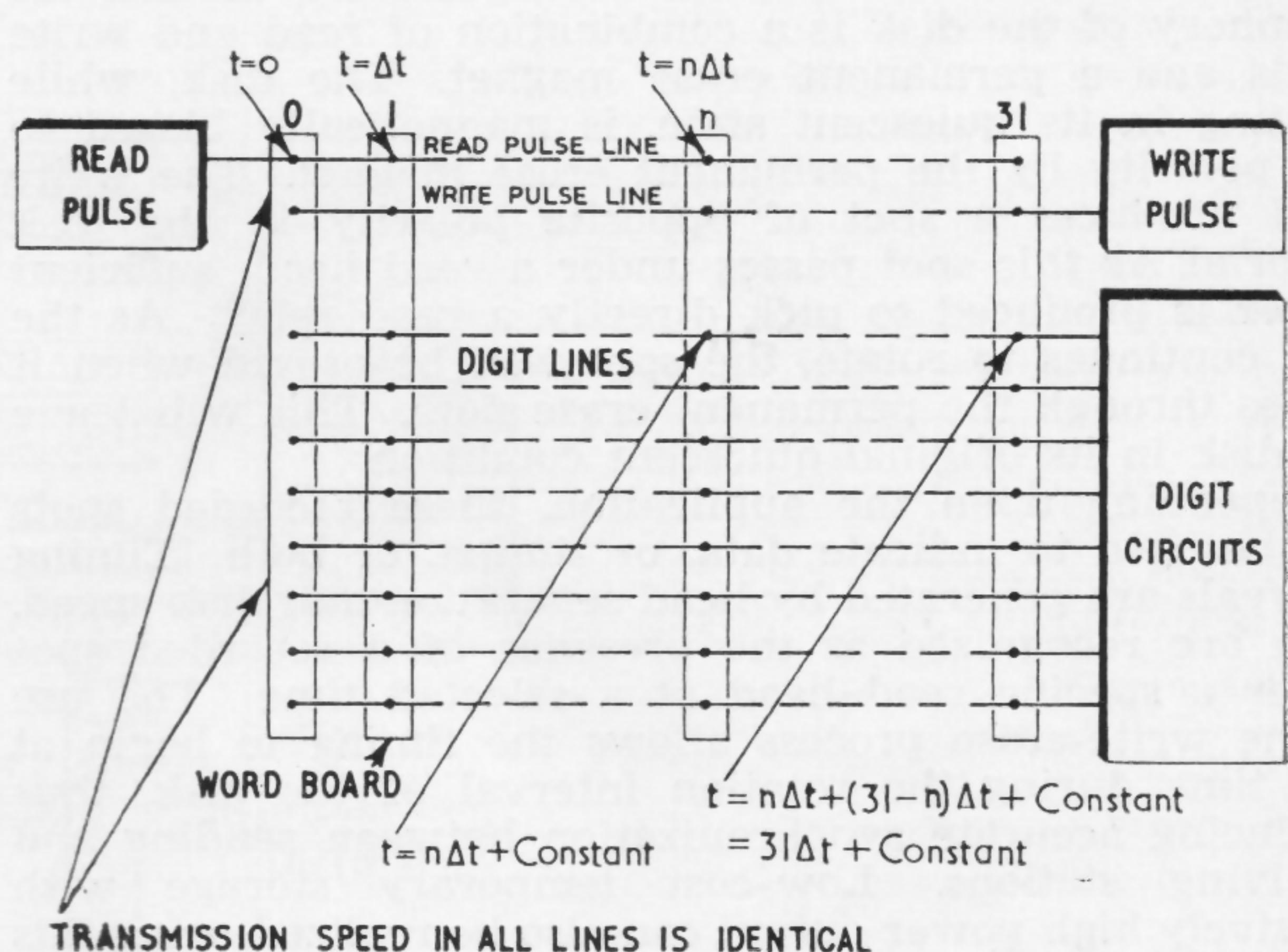


Figure 4—Word drive timing. Unselected boards are connected to lines by reverse biased diodes. Diode capacity and line inductance form a 50-ohm transmission line.

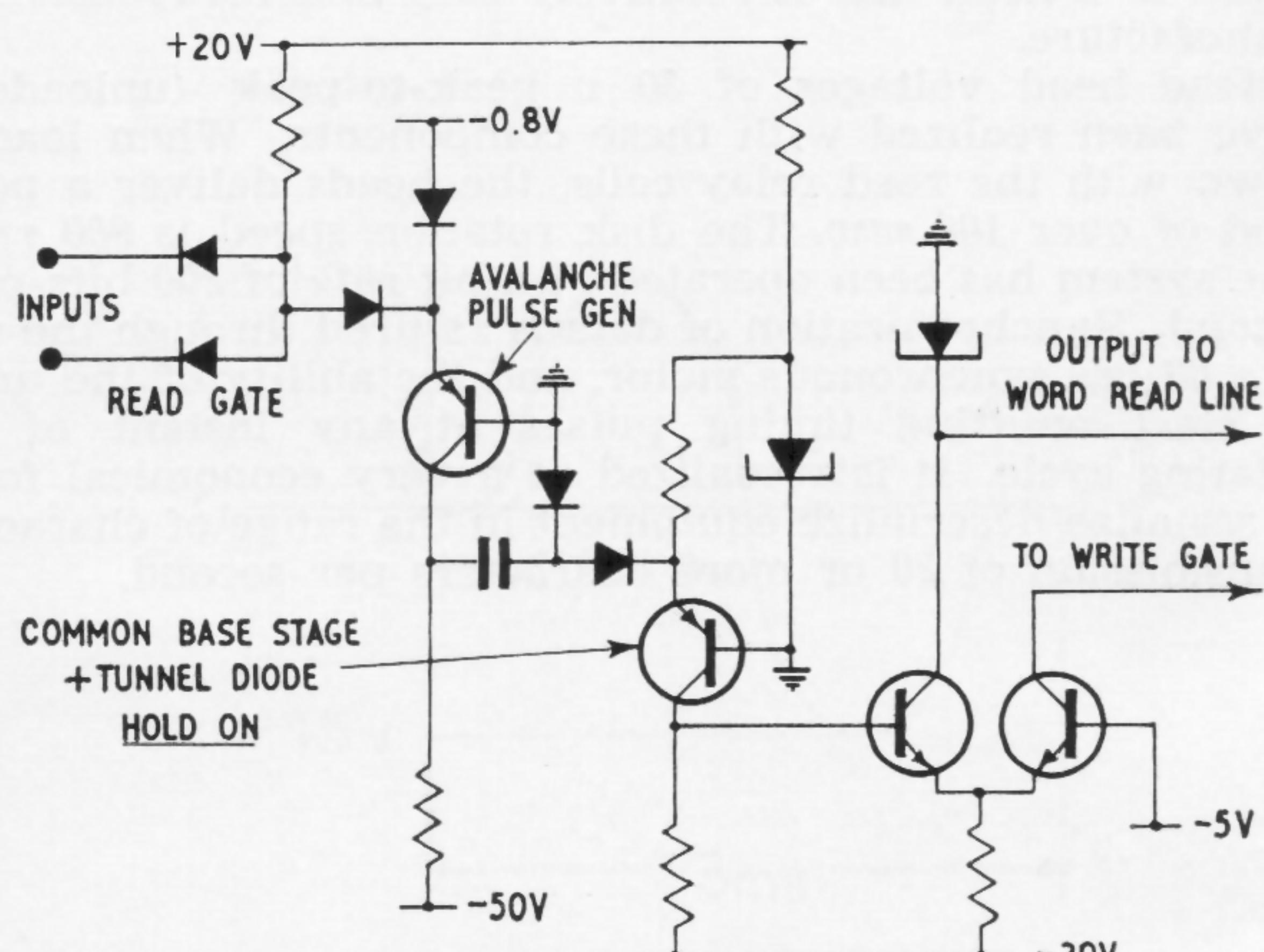


Figure 5—Simplified read-line drive circuit.

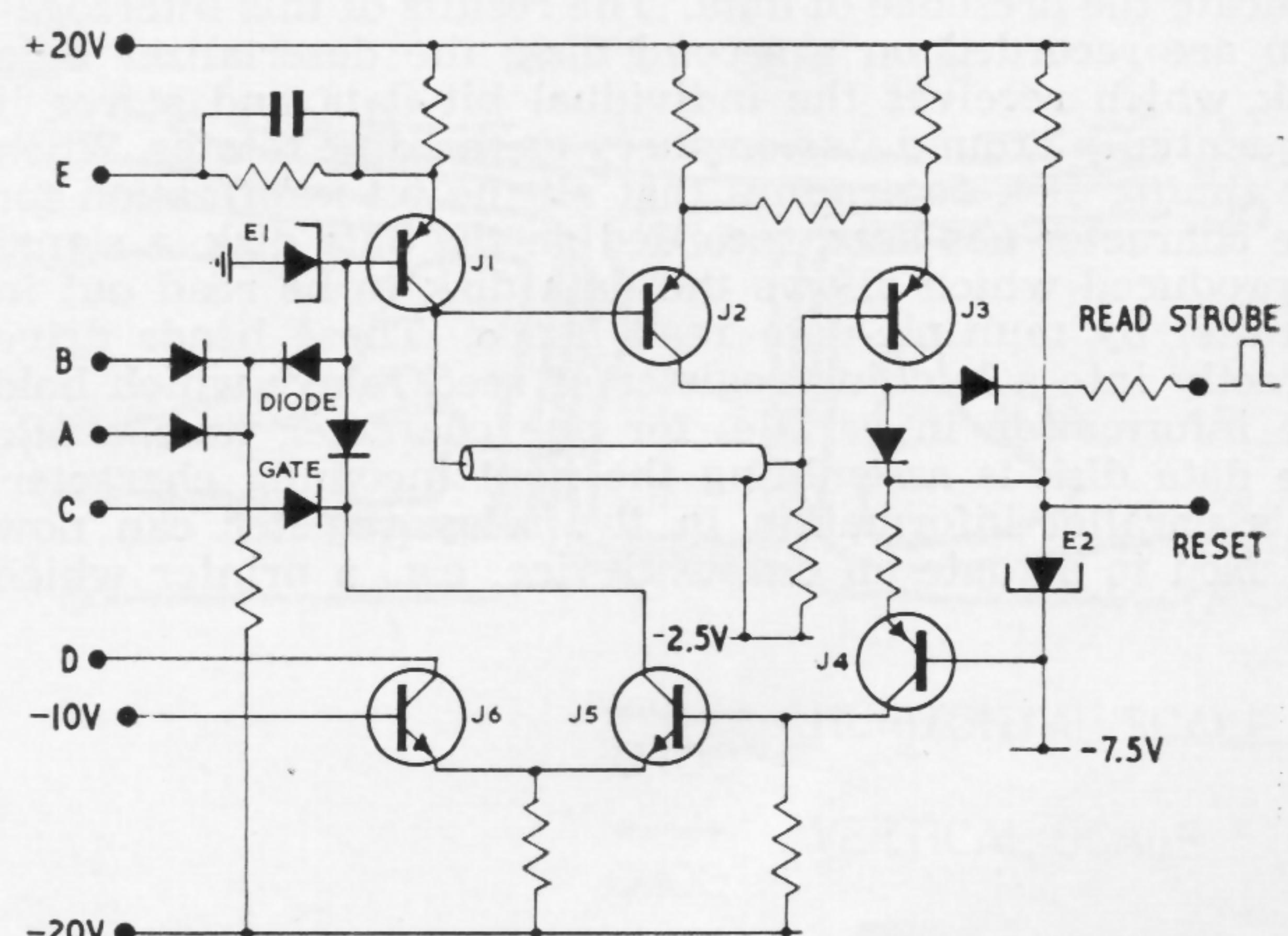


Figure 6—Simplified digit circuit.

## SESSION IV: Memory

## WA 4.4: A Magnetic Disk Serializer-Deserializer

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IBM Corporation

Endicott, N. Y.

VARIOUS ELECTRONIC and mechanical arrangements have been devised for serializing and deserializing data. This paper will describe an arrangement using a disk of permanent magnetic material, inexpensive read and write heads, reed relays, and transistor circuitry.

The disk arrangement consists of a synchronous motor drive and a rotatable magnetic disk. Located around the periphery of the disk is a combination of read and write heads and a permanent erase magnet. The disk, while rotating in its quiescent state, is magnetically biased to one polarity by the permanent erase magnet. The write head produces a spot of opposite polarity in the disk material. As this spot passes under a read head, sufficient power is produced to pick directly a reed relay. As the disk continues to rotate, the spot will be erased when it passes through the permanent erase field. This will leave the disk in its original quiescent condition.

Depending upon the application, these recorded spots can be used to indicate data, or timing, or both. Timing intervals are generated by head separation and disk speed. Data are recognized as the presence of a recorded spot under a specific read head at a selected time. The use of the write-erase process allows the timing to begin at any time during the rotation interval of the disk, thus producing accurate synchronization between sending and receiving stations. Low-cost temporary storage with relatively high power output can also be realized using this type of disk arrangement.

To transmit information serially over communications lines, a means to designate the start of an incoming character must be developed. A familiar solution to this problem is the addition of a start and a stop bit to the information bits of the transmitted character. The recognition of the start bits indicates that information bits will follow at predetermined intervals. Thus, at start bit time, a spot can be written on the deserializer timing disk which, when it passes the individual timing read heads, will produce timing pulses that indicate the various data times. These timing pulses are added with the data line to indicate the presence of data. The results of this interrogation are recorded on a second disk, the deserializer data disk which receives the individual bit data and stores it sequentially around its periphery as the disk rotates. When the timing disk determines that all the bit information for one character has been recorded on the data disk, a signal is produced which allows the data disk to be read out in parallel by multiple-data read heads. These heads drive directly into a latching register of reed relays which hold the information in parallel for one character time, while the data disk is assembling the next incoming character. This parallel information in the relay register can now be used to actuate an output device; e.g., a printer which

normally uses parallel information only. The ability of the deserializer timing disk to start generating synchronized timing pulses at any point during its rotation, plus the capability of the read heads driving a relay storage register with no need of amplification, are two of the chief advantages of the disk scheme.

Information to be transmitted usually comes from a parallel by bit source; e.g., keyboard or tape reader. The serializer must reassemble the bit information into a serial form, plus start and stop bits to transmit it over the communications lines. Parallel information is transferred from a reader or keyboard to a relay input register. The contact closures of this register determine which of the multiple write heads on the serializer data disk will be pulsed. At the same time, a timing spot is recorded on the serializer timing disk, and the character start bit is produced on the output line. The data disk has multiple write heads and a single read head. The timing disk has a single write head and multiple read heads. As the timing spot passes under any of the timing read heads, a timing pulse is produced. This timing pulse is then compared with the output of the data read head. If data and timing are present at the same time, the output line will indicate a 1 bit of information. If a timing pulse occurs with no data pulse, the output line will indicate a 0 bit of information. Through this process, the parallel by bit information is transformed into serial by bit information and sent over the output lines to the receiving station in NRZ form.

The disk can be made from a number of different materials which have coercive forces in the range of 1000 to 1600 oersteds, residual flux densities from 1600 to 2200 gauss, and maximum energy products in the range of  $.7 \times 10^6$  to  $2 \times 10^6$  gauss oersteds. Disk sizes of 3" to 6" in diameter and  $1/64"$  to  $1/4"$  thick have been used, depending upon the particular application and speed ranges required. The read and write heads are of a vertical bar shape using air as a return flux path. Typical gap distances between head and disk range from  $.003"$  to  $.010"$ . The simple shape plus relatively loose gap tolerances result in a head that is relatively easy and inexpensive to manufacture.

Read head voltages of 30 v peak-to-peak (unloaded) have been realized with these components. When loaded down with the reed relay coils, the heads deliver a peak load of over 100 mw. The disk rotation speed is 900 rpm. The system has been operated at a bit rate of 200 bits-per-second. Synchronization of data is assured through the use of a 60-cps synchronous motor, and the ability of the units to start emitting timing pulses at any instant of its rotating cycle. It is visualized as a very economical form of serialize-deserialize equipment in the range of character transmission of 20 or more characters per second.

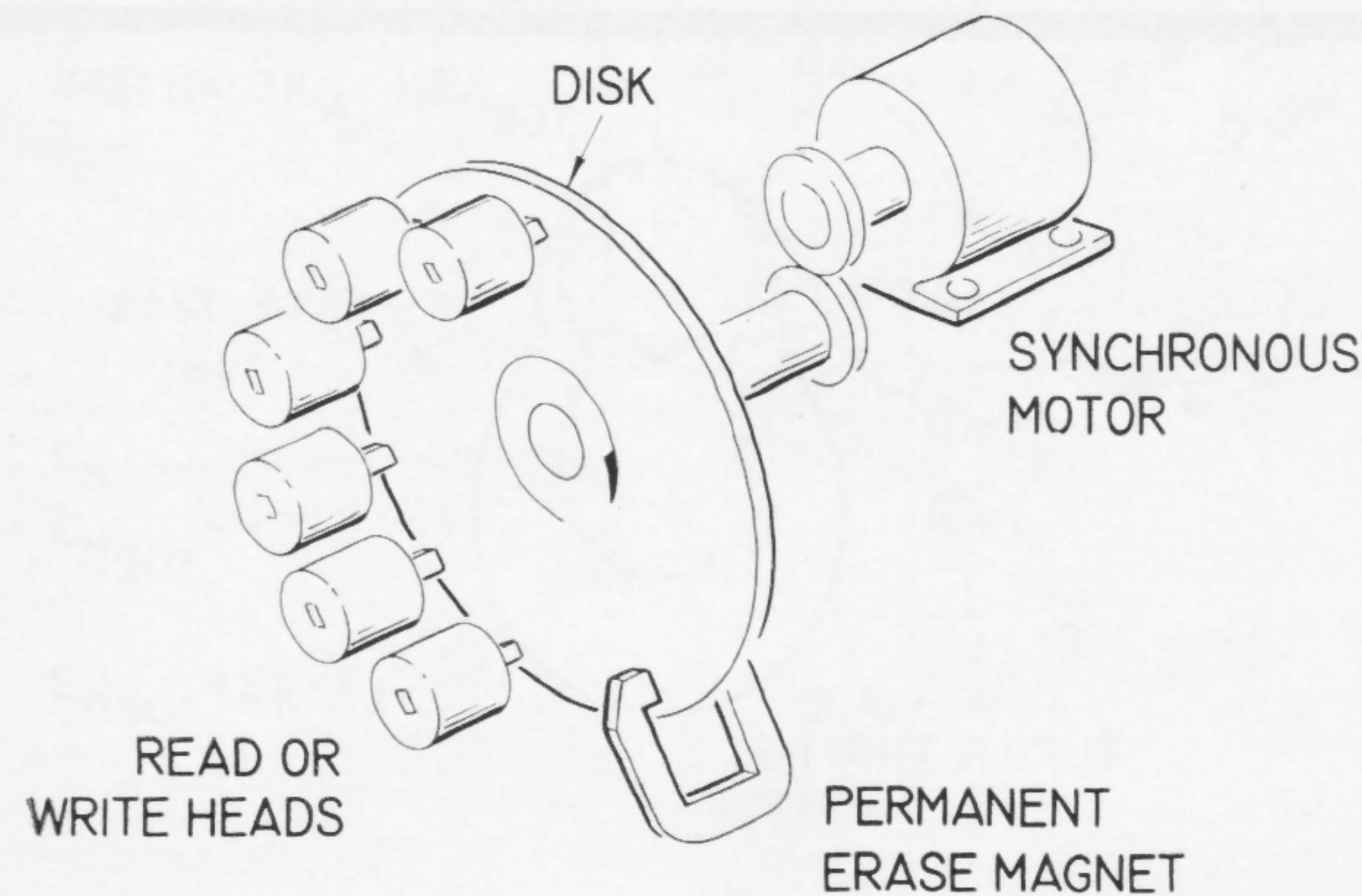


Figure 1—Schematic of the serializer-deserializer.

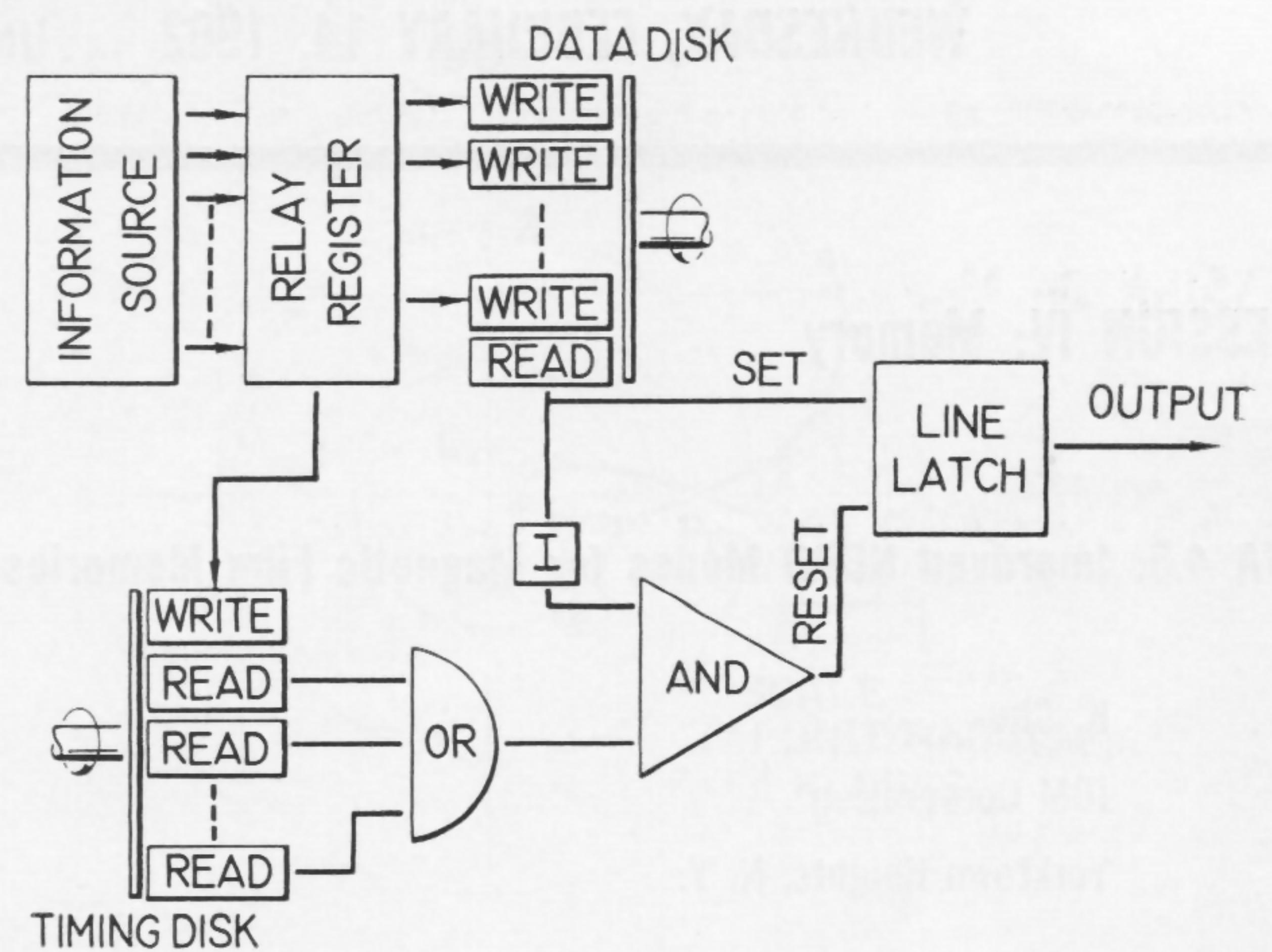


Figure 2—Serializer logic diagram.

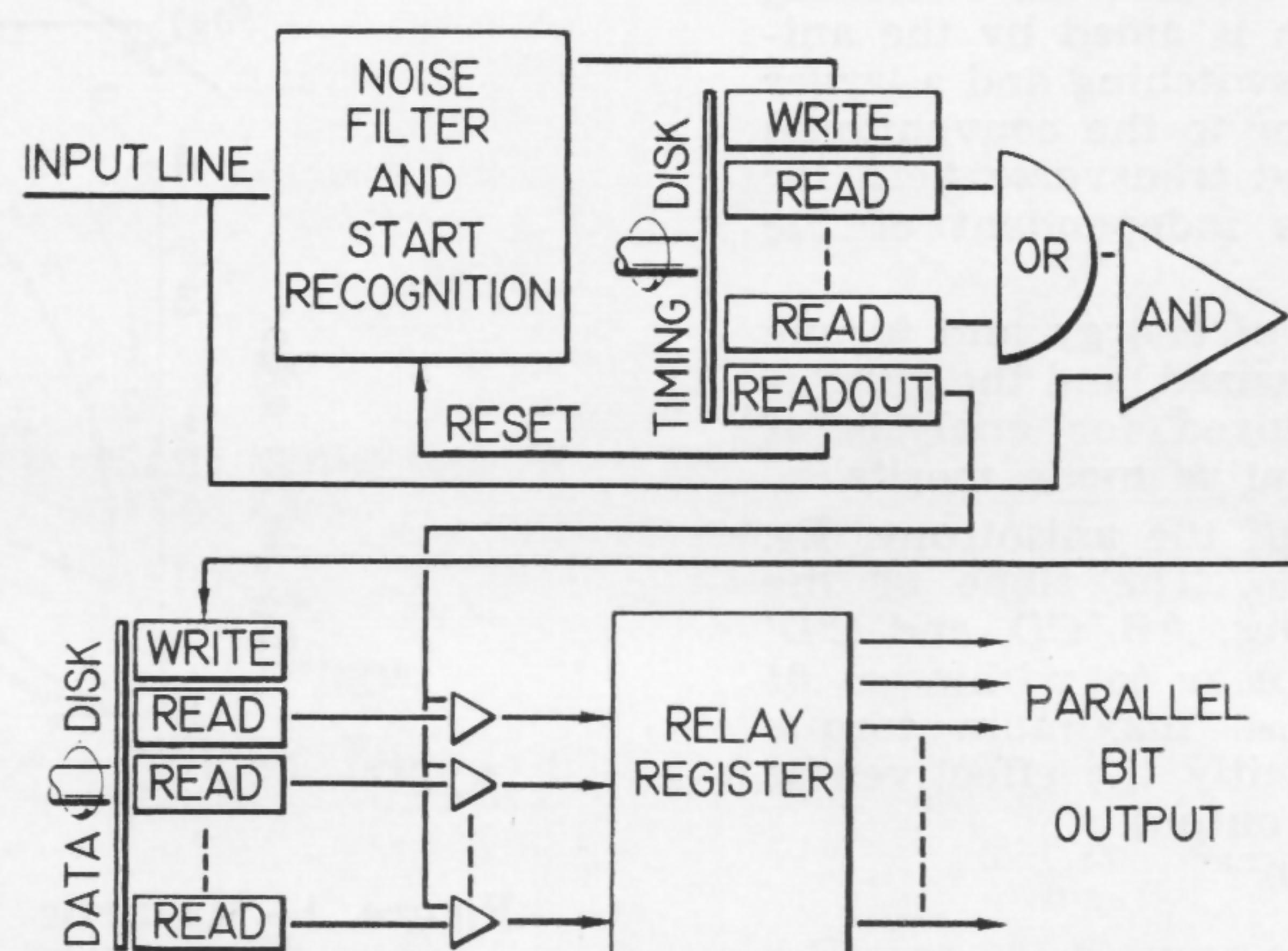


Figure 3—Deserializer logic diagram.

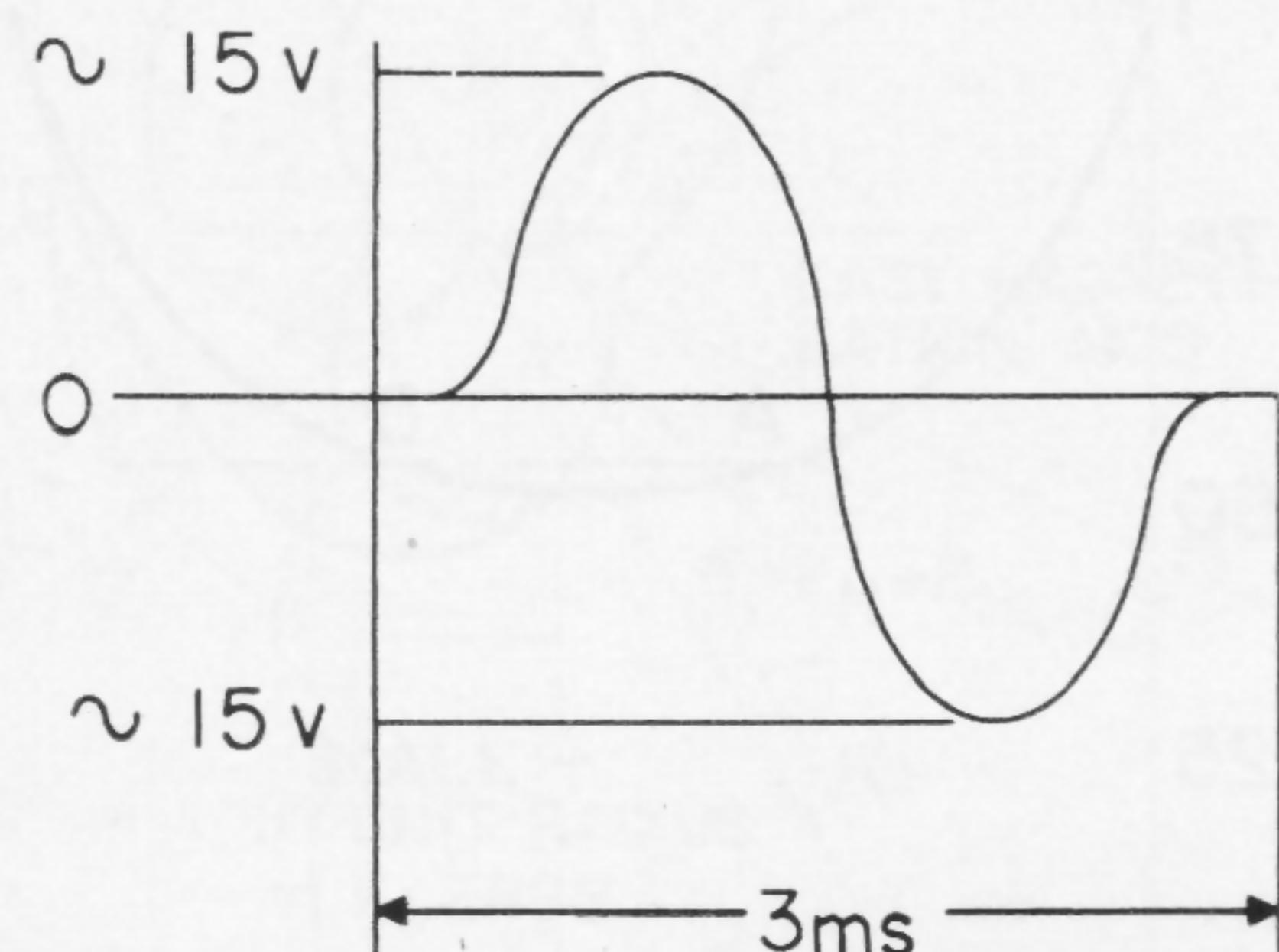


Figure 4—Unloaded read head output.

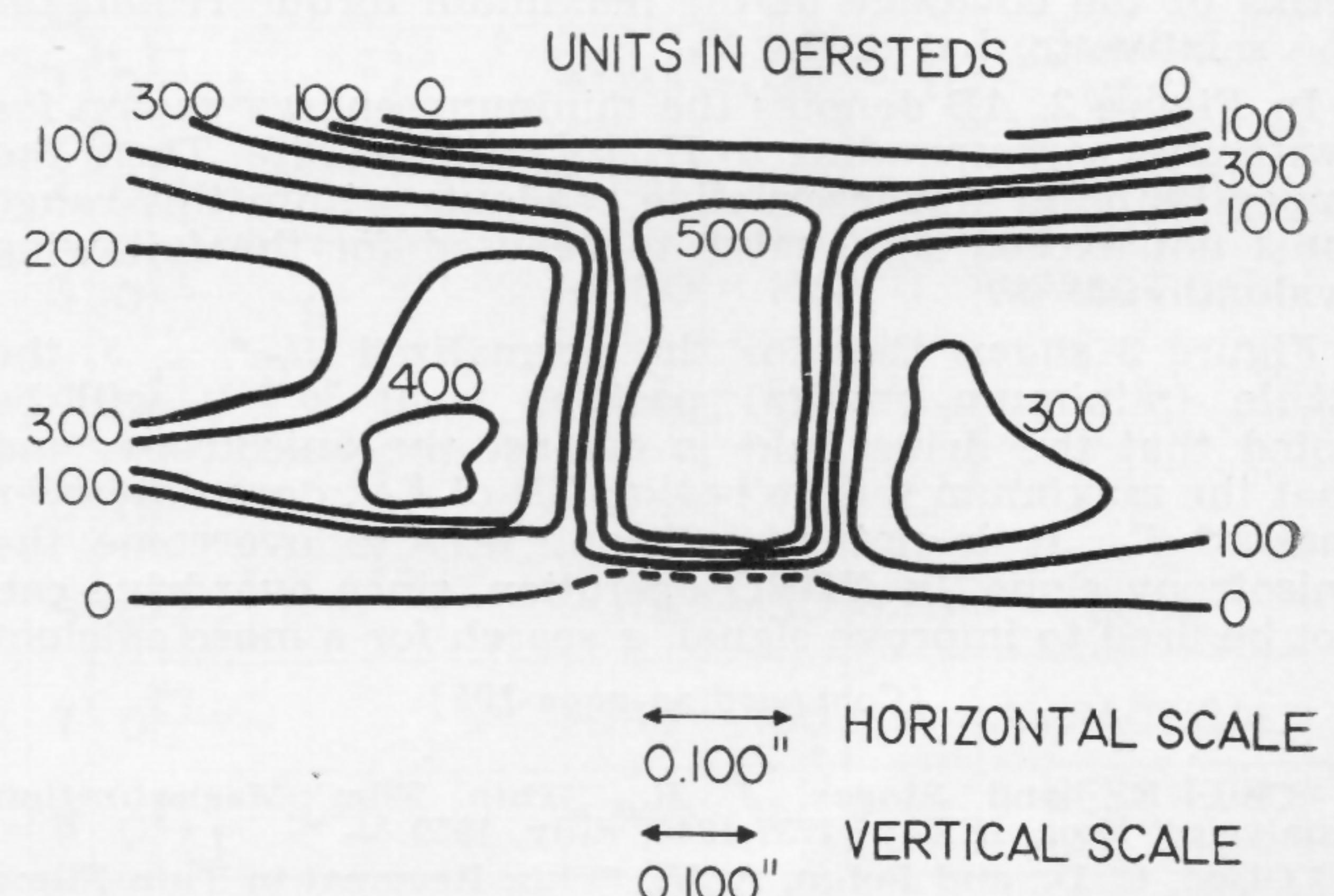


Figure 5—Flux map of a magnetic spot.

## SESSION IV: Memory

## WA 4.5: Improved NDRO Modes for Magnetic Film Memories

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IBM Corporation

Yorktown Heights, N. Y.

A NEW MODE of NDRO (nondestructive readout) using field-reversal on uniaxial films will be proposed in this paper.

The drive field consists of a positive pulse followed directly by a negative pulse. During the positive drive pulse the switching of the film is opposed by the anisotropy field, but during the negative pulse the switching of the already rotated magnetization is aided by the anisotropy of the film, resulting in fast switching and a larger output voltage. This mode is superior to the conventional mode, i.e., the use of unipolar-pulsed transverse field for the NDRO interrogation, and it is independent of the drive and sense-line configurations.

In this presentation, the concepts of energy and torque within a magnetic film will be emphasized, and the graphical energy patterns<sup>1</sup> will be employed for analysis of NDRO modes and evaluation of relative mode merits.

Figure 1 shows a Cartesian plot of the anisotropy,  $E_K$ , and the magnetization energies,  $E_{H\theta}$ . The slope of the curve denotes torque. On these curves, AB, CD, and C'D' denote maximum torque regions, linear to within  $\pm .01$  erg. The relative positions of these maximum torque regions of  $E_K$  and  $E_{H\theta}$  reveals explicitly the effectiveness of the drive and desirability of the output.

From the Landau-Lifshitz equation<sup>2,3</sup>

$$\dot{\vec{M}} = -|\gamma|(\vec{M} \times \vec{H}) - \left| \frac{\gamma a}{M} \right| \vec{M} \times (\vec{M} \times \vec{H}).$$

two parametric equations may be derived, from which the output voltages and switching times may be found<sup>2,3</sup>. Since the output voltage is proportional to the torque, relative amplitudes of the output voltages for 1 and 0 can be derived graphically from the torque curve.

A plot of  $H_\theta/H_K$  versus  $\theta$  where  $\theta$  is the direction of the applied field appears in Figure 2. Less field is required to perform switching if the drive field is applied at a certain angle<sup>2,3</sup>. This behavior may be explained easily in terms of the coverage of the maximum torque region for  $E_{H\theta}$  relative to that of the  $E_K$ .

In Figure 2, AB denotes the minimum energy region for switching, corresponding to  $H_\theta/H_K = .51 \pm 10\%$ . Then, the upper limit for nondesctructive readouts within this range must not exceed .5, a value to be used for the following evaluations.

Figure 3 shows that for the normalized  $H_{90^\circ}/H_K = .5$ , the stable (minimum energy) position is at  $30^\circ$ . It will be noted that the drive field is against the anisotropy, and that the maximum torque region CD of  $E_{H\theta}$ , does not cover that of  $E_K$ . It is not an efficient way to overcome the anisotropy slope. In NDRO operation, since overdrive can not be used to improve signal, a search for a more efficient

[Continued on page 105]

<sup>1</sup> Chu, K., and Singer, J. R., "Thin Film Magnetization Analysis," Proc. IRE, p. 1237-1244; July, 1959.

<sup>2</sup> Olson, C. D., and Pohm, A. V., "Flux Reversal in Thin Films of 82% Ni, 18% Fe, Journal of Applied Physics, p. 274-282; March, 1958.

<sup>3</sup> Smith, D. O., "Static and Dynamic Behavior of Thin Permalloy Films," Journal of Applied Physics, p. 264-273; March, 1958.

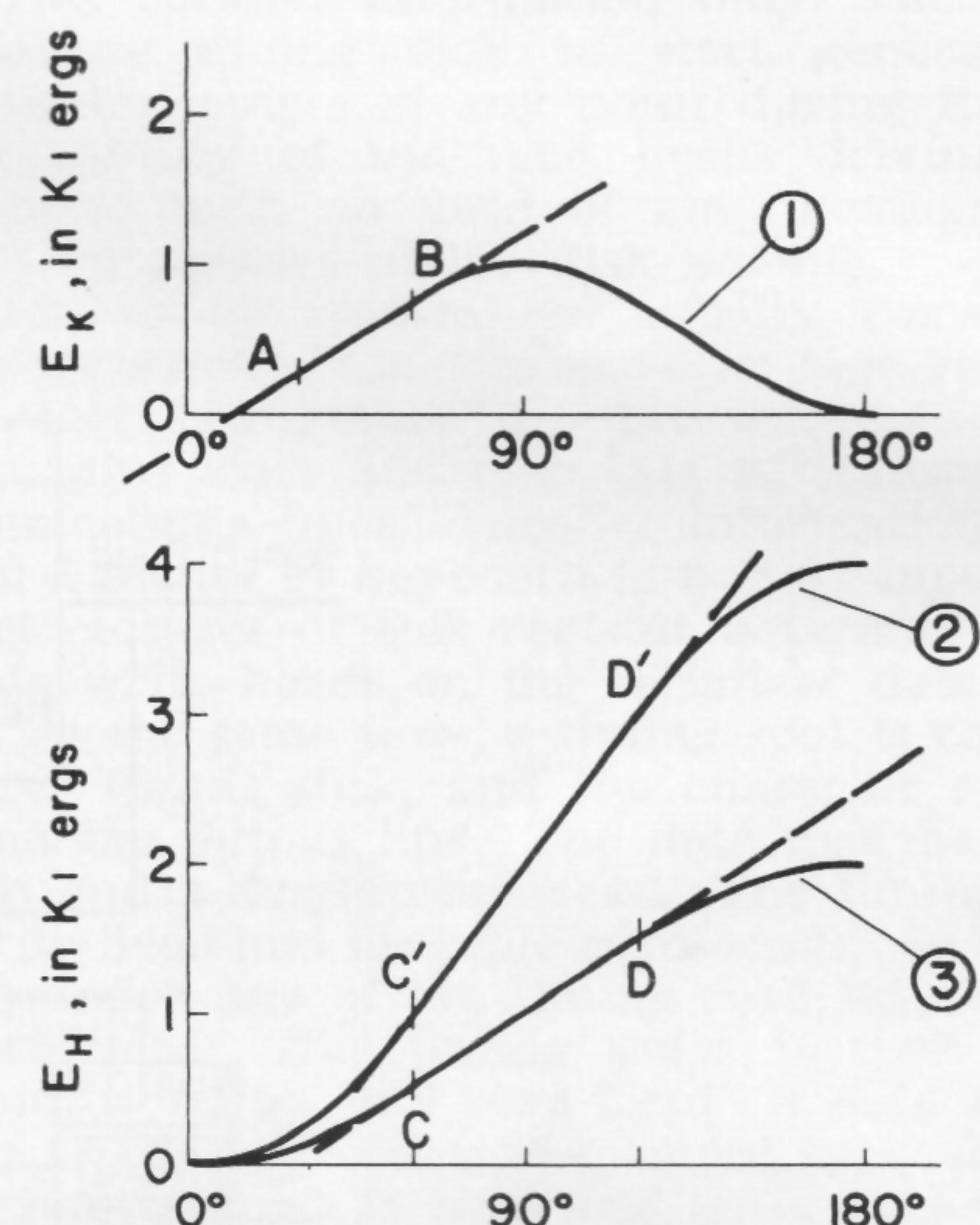
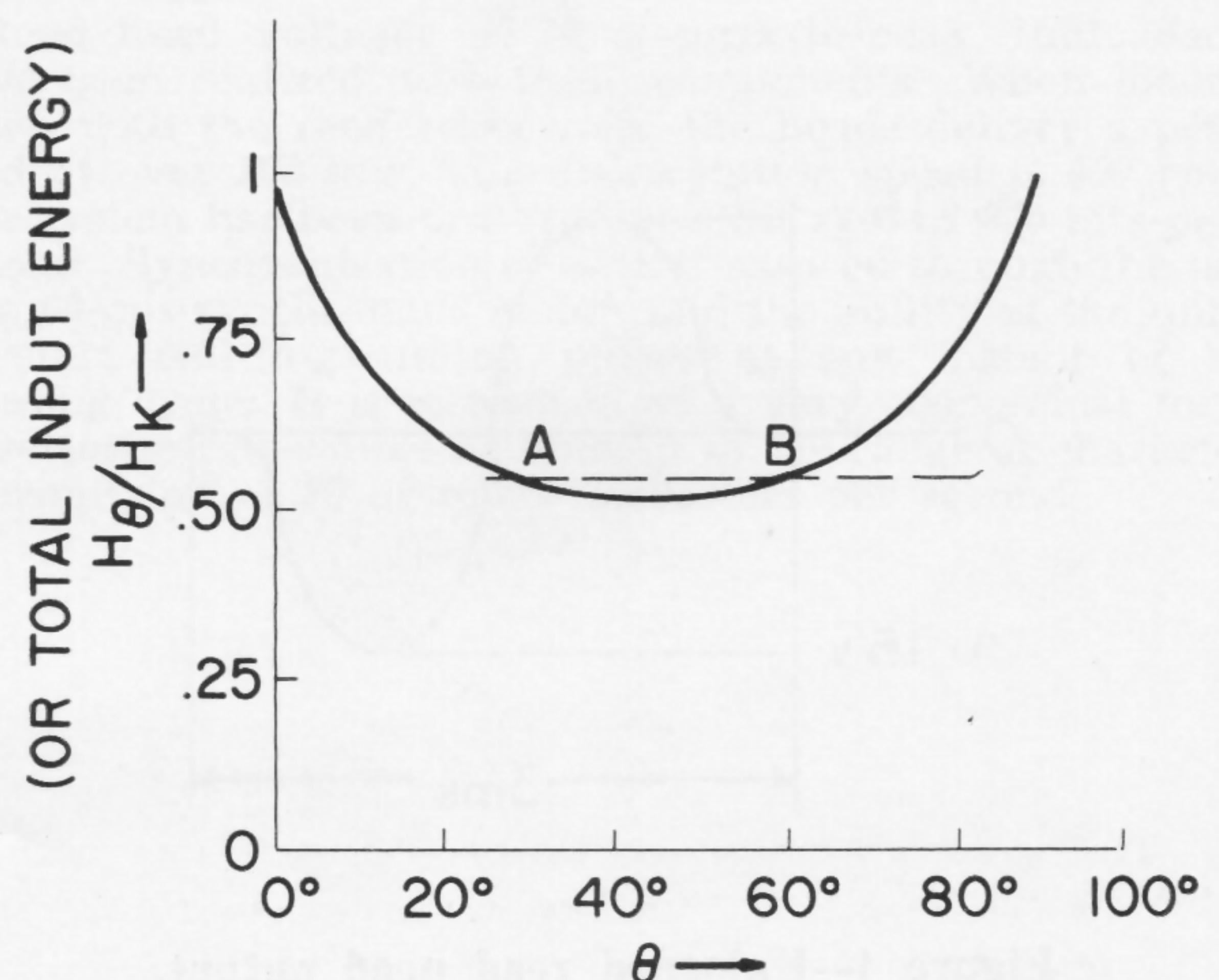


Figure 1—Magnetic energy curves: (1) Anisotropy energy  $E_K = K_0 + K_1 \sin^2\theta$ , and magnetization energies.  $E_{H\theta} = HM_s |\cos(\theta_0 - \theta)|$ ; (2)  $H = K_1/M_s$ , and (3)  $H = 2K_1/M_s$  (Cartesian plot).

(Below)

Figure 2—Curve of normalized angular drive fields  $H_\theta/H_K$  versus the applied field direction  $\theta$ .



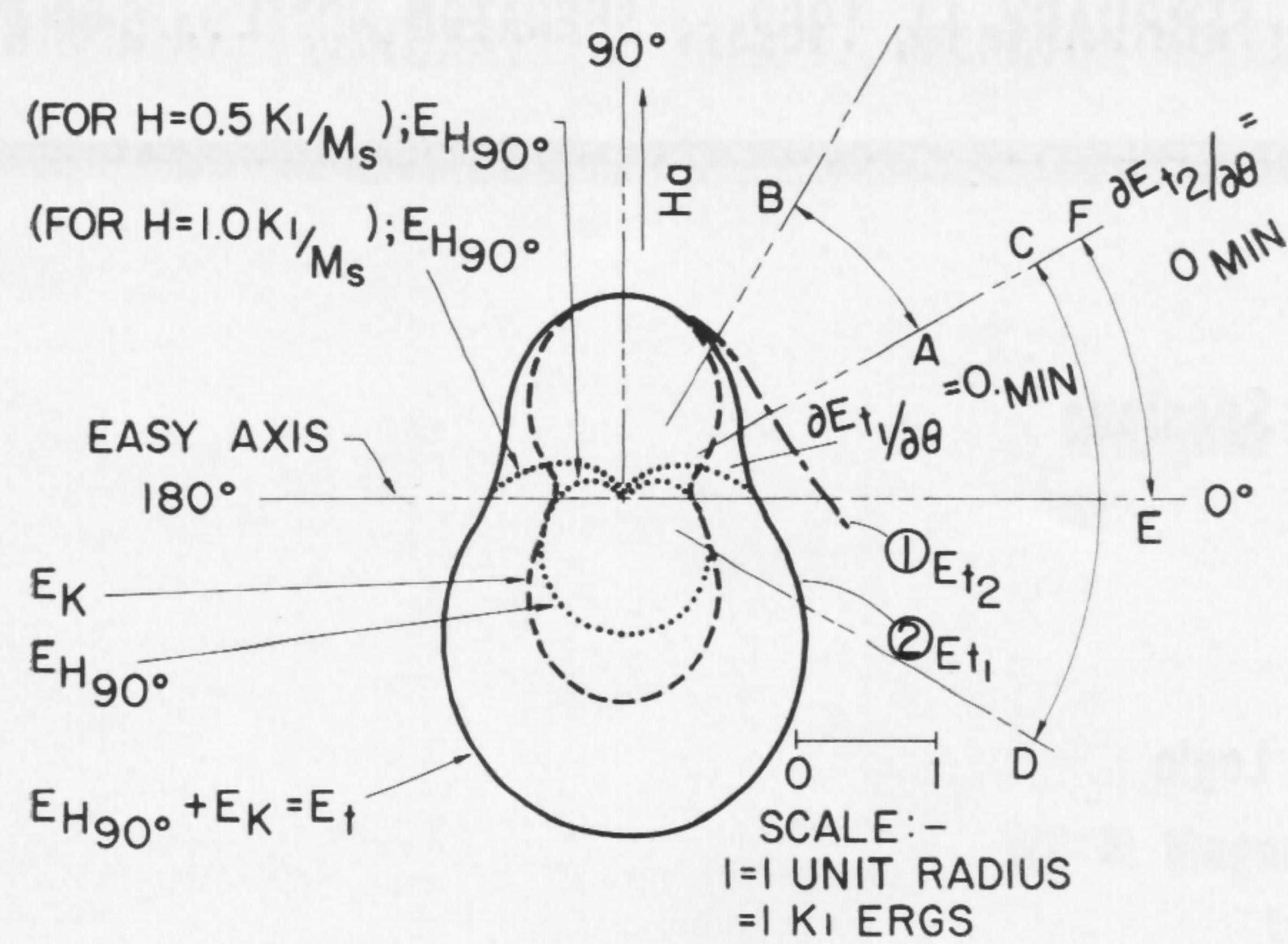


Figure 3—Total free energy curve where  $E_t = E_k + E_{H90^\circ}$ ; (1)  $H_{90^\circ} = .5 K_1/M_s$ , and (2)  $H_{90^\circ} = K_1/M_s$  (Polar plot).

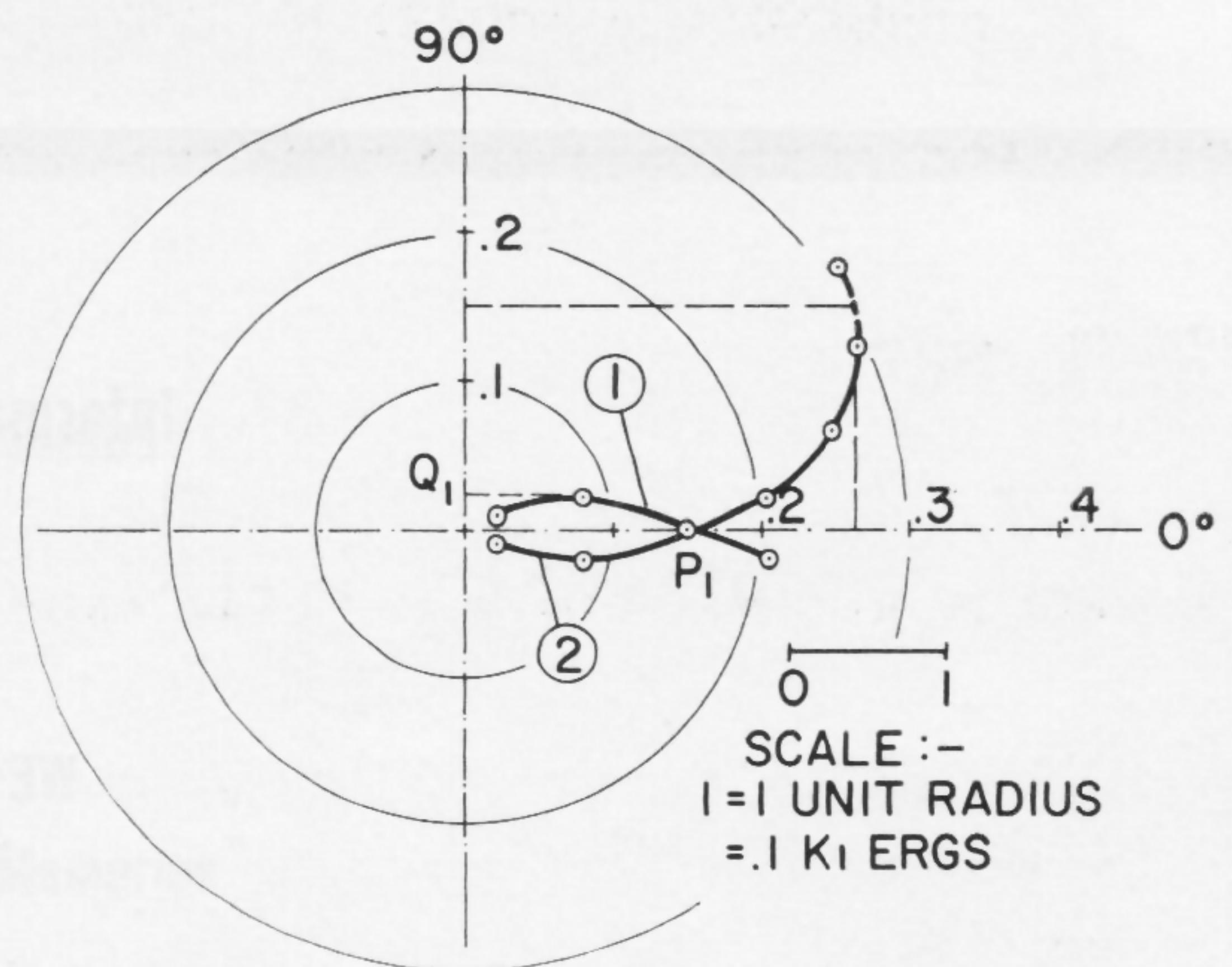


Figure 5—Torque curves under the condition of Figure 3: (1) Conventional NDRO mode and (2) NDRO mode by field reversal.

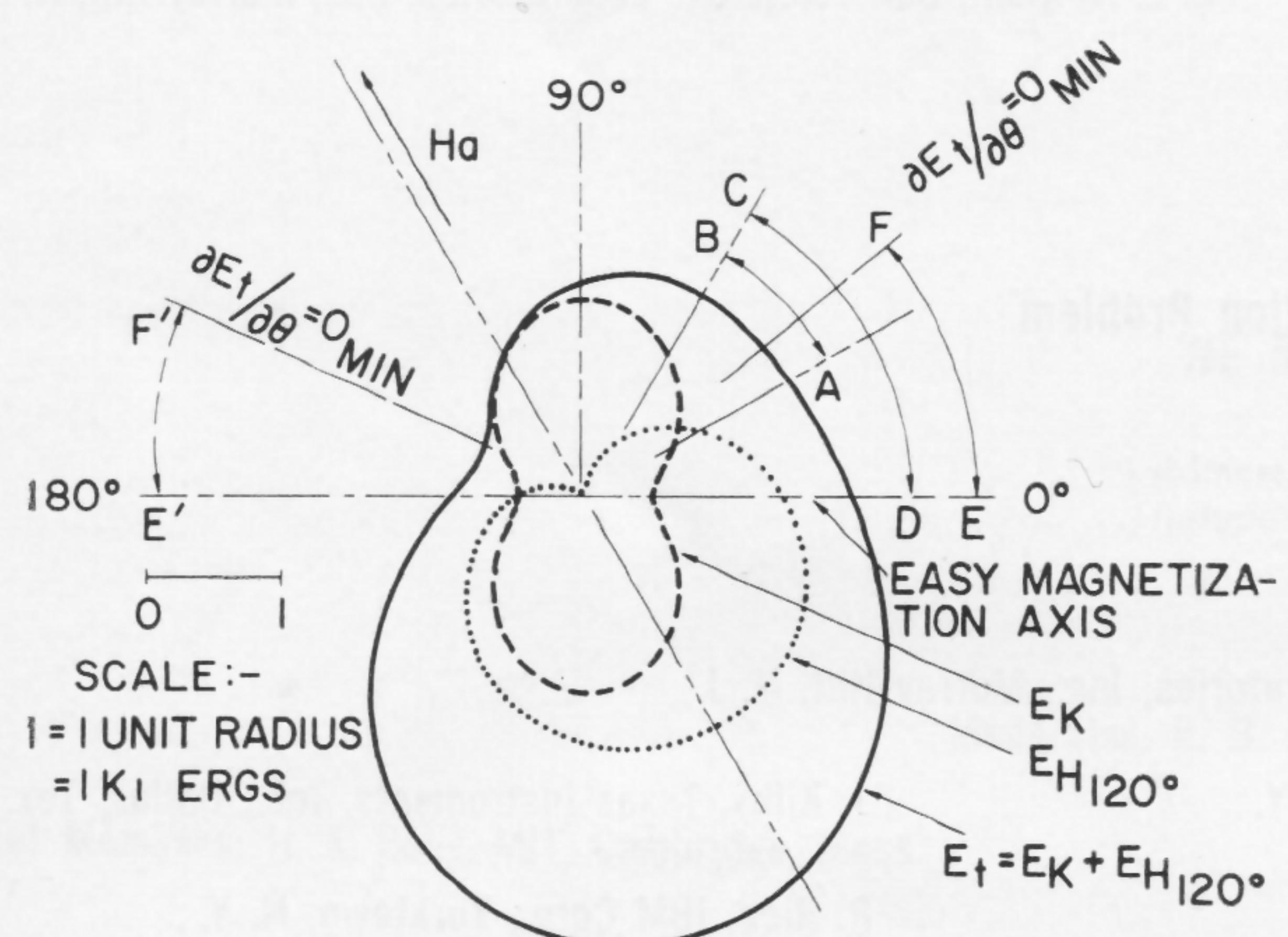


Figure 4a—Total free energy curve where  $E_t = E_k + E_{H120^\circ}$  for  $H_{120^\circ} = K_1/M_s$  (Polar plot).

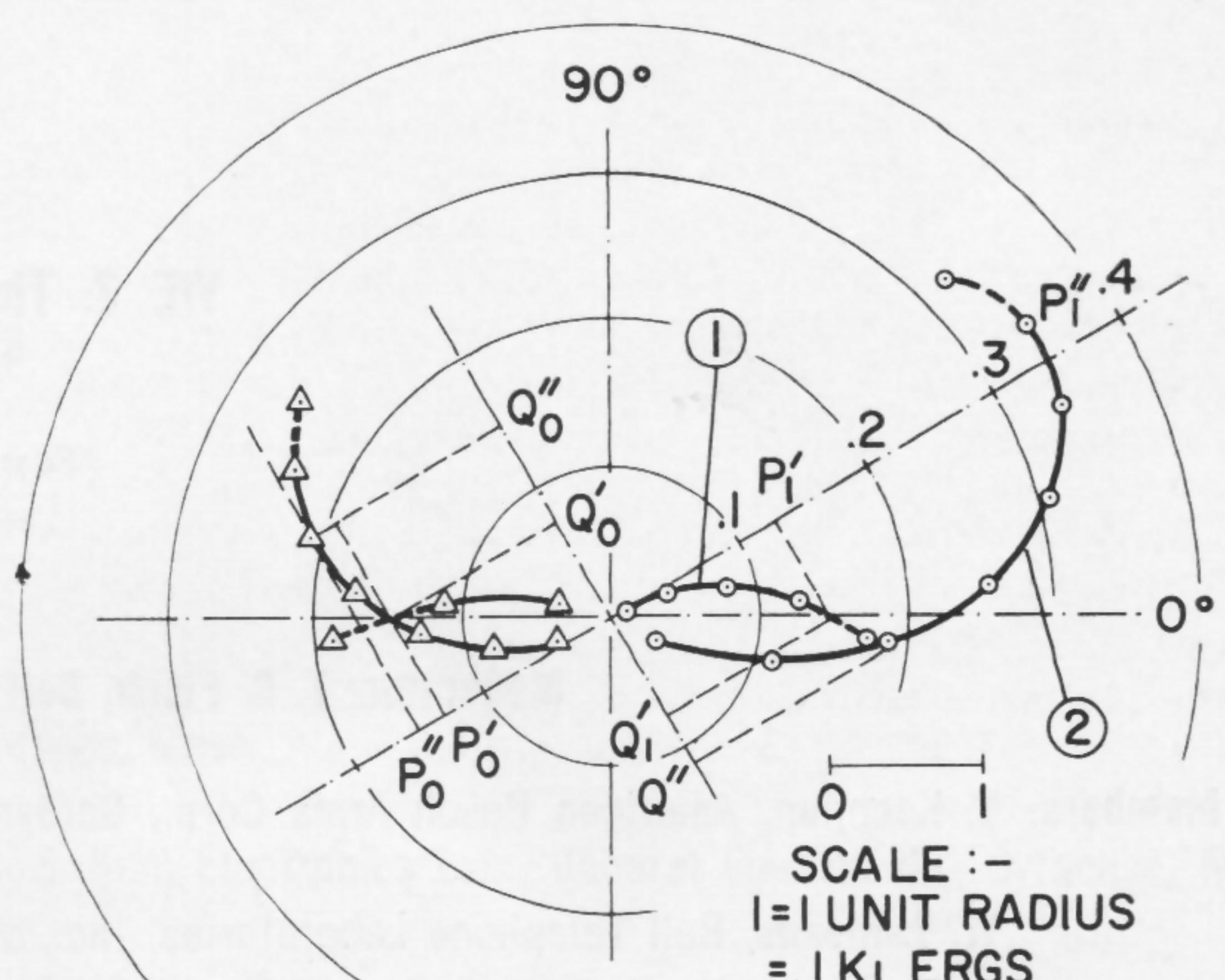


Figure 6—Torque curves under the condition of Figures 4a and 4b: (1) Conventional NDRO mode and (2) NDRO mode by field reversal.

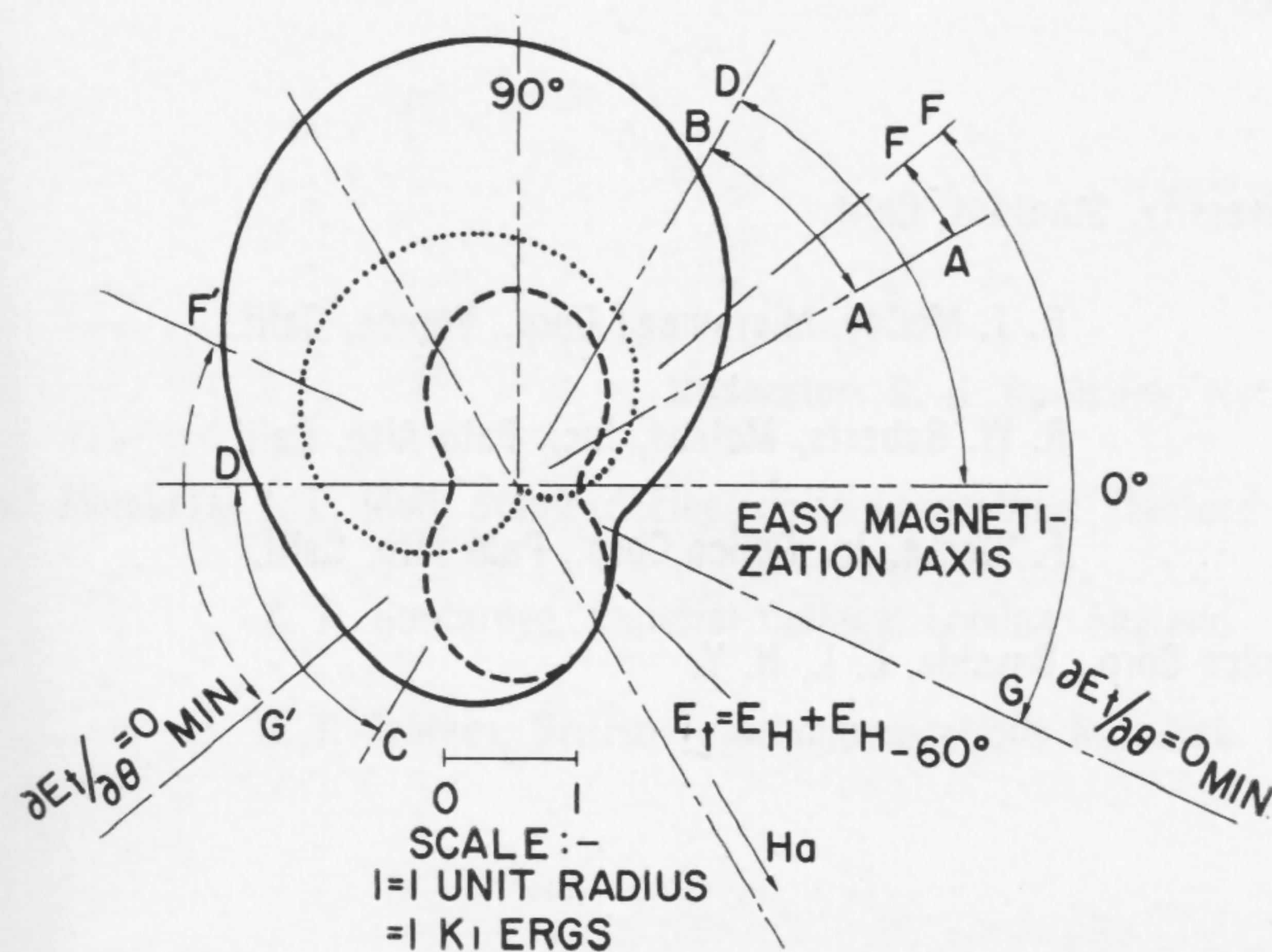


Figure 4b—Total free energy curve where  $E_t = E_h + E_{H300^\circ}$  for  $H_{300^\circ} = K_1/M_s$  (Polar plot).

CASE	CONDITIONS	$V_o$ (PEAK)		RATIO I/O	REMARK
		I	O		
1	$H_0$ $t$ $S$	+.023	-.023	- 1	COMMONLY USED
2	$0$ $D$ $S$	+.150	-.150	- 1	BEST FOR I/O DISC
3	$0$ $S$	-.150	-.150	1	IMPRactical
4	$0$ $D$ $S$	-.260	-.260	1	"
5	$0$ $S$	-.075	-.075	1	"
6	$0$ $D$ $S$	-.112	-.150	0.75	GOOD
7	$0$ $S$ $D$	-.130	-.130	1	IMPRactical
8	$0$ $S$ $D$	-.340	-.150	2.27	BEST FOR MAX SIG

Table I—NDRO modes and merits.

### Informal Discussion Sessions

#### WE 1: Distributed Logic

[West Ballroom]

**Moderator:** E. E. Loebner, HP Associates, Palo Alto, Calif.

**Panel Members:** H. D. Block, Cornell University, Ithaca, N. Y.

R. J. Lee, Adaptronics, Springfield, Va.

M. Hirscher, RCA, Camden, N. J.

P. D. Low, Stanford University, Stanford, Calif.

R. D. Vernot, Philco Research Division, Blue Bell, Pa.

E. E. Newhall, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

#### WE 2: The Interconnection Problem

[East Ballroom and Assembly]

**Moderator:** T. R. Finch, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

**Panel Members:** E. Keonjian, American Bosch Arma Corp., Garden City, L. I., N. Y.

J. Kilby, Texas Instruments, Inc., Dallas, Tex.

W. J. Means, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

R. Rice, IBM Corp., Yorktown, N. Y.

R. Gerhold, Hexagon, Signal Corps Laboratory, Ft. Monmouth, N. J.

A. Coleman, RCA, Camden, N. J.

#### WE 3: Microwave Power Sources

[Pennsylvania West]

**Moderator:** J. B. Angell, Stanford University, Stanford, Calif.

**Panel Members:** A. Uhlir, Jr., Microwave Associates, Inc., Burlington, Mass.

R. T. McCoy, Micromega Corp., Venice, Calif.

F. Sterzer, RCA Laboratories, Princeton, N. J.

R. W. Roberts, Melabs, Inc., Palo Alto, Calif.

R. P. Rafuse, MIT, Cambridge, Mass.

F. Storke, Jr., Philco Corp., Palo Alto, Calif.

W. B. Hauer, General Telephone and Electronics Corp., Bayside, L. I., N. Y.

### Informal Discussion Sessions

#### WE 4: Magnetic Thin-Film Memories

*[Pennsylvania East]*

**Moderator:** A. K. Rapp, Philco Research Division, Blue Bell, Pa.

**Panel Members:** E. E. Bittman, Burroughs Corp., Paoli, Pa.

R. Petschauer, Remington Rand Univac, St. Paul, Minn.

J. I. Raffel, MIT Lincoln Laboratory, Lexington, Mass.

J. A. Rajchmann, RCA Laboratories, Princeton, N. J.

#### WE 5: Noisemanship

*[Independence-Constitution]*

**Moderator:** R. B. Adler, MIT, Cambridge, Mass.

**Panel Members:** H. A. Haus, MIT, Cambridge, Mass.

J. C. S. Kim, Electronics Lab., General Electric Co., Syracuse, N. Y.

A. van der Ziel, University of Minnesota, Minneapolis, Minn.

W. W. Mumford, Bell Telephone Laboratories, Inc., Whippany, N. J.

#### WE 6: Charge-Control Characterization of Semiconductor Devices

*[Delaware Valley Suite]*

**Moderator:** G. H. Goldstick, National Cash Register Co., Hawthorne, Calif.

**Panel Members:** J. L. Moll, Stanford Electronics Laboratory, Stanford University, Stanford, Calif.

C. L. Hegedius, IBM Corp., Poughkeepsie, N. Y.

A. R. Boothroyd, Imperial College, London, England

R. D. Lohman, RCA, Somerville, N. J.

J. J. Sparkes, British Telecommunications Research, Ltd., Berkshire, England

C. E. Simmons, Philco Corp., Lansdale, Pa.

## SESSION V: High Speed Switching

Chairman: V. H. Grinich

Fairchild Semiconductor, A Division of Fairchild Camera and Instrument Corporation,  
Palo Alto, Calif.

### TM 5.1: High-Speed Non-Saturating Switching Circuits Using a Novel Coupling Technique

D. W. Murphy

IBM Corporation

Poughkeepsie, N. Y.

THIS PAPER will describe a circuit family intended for use in a high-speed, parallel scientific computer. These circuits have propagation delays of less than 5 nsec; pulses 5 nsec wide are used for clocking. Power dissipation averages 25-mw per circuit, and with the proposed packaging scheme densities in excess of 10,000 circuits per-cubic-foot can be achieved. With these circuits, it has been possible to design a computer which will process two 64-bit words at an average rate of 1.8 Mc; i.e., add, subtract, multiply, divide, shift, etc.

All components for this circuit family are commercially available. The logic circuits have been designed to use a transistor with an 800-Mc gain-bandwidth product. Tunnel diodes with less than 1-pf/ma of peak current are used for power drivers and storage elements. The only other components are precision film resistors and capacitors.

Transistors, which maintain high-frequency response under the condition of  $V_{cb} < 0$ , are now available, as shown in Figure 1. Two distinct advantages are realized by operating with  $V_{cb} < 0$ . First, the circuitry is quite simple. Secondly, the collectors can be directly coupled to the driven base without saturation effects or the need for external voltage translation.

The circuits are based upon the technique of current switching using cascode transistors. The basic configuration is shown in Figure 2. The most common circuit configuration is one which forms the implication function ( $I = A + \overline{B}$ ). Because of this function, isolated inverters are never used, and it is never necessary to ship both a signal and its complement. By paralleling transistors, the function is extended to  $I = A + C + \overline{B} + D$  shown in Figure 3.

A conventional OR circuit, with both normal and complementary outputs, is obtained if the cascode transistors are omitted from the basic implication circuit.

Since discrete currents are switched, outputs can frequently be wired together to form a positive AND, as in Figure 4, resulting in a level of logic at no cost in com-

ponents. Two of the implication circuits are wired together to form an exclusive OR with six transistors and one level of circuit delay. In addition, when the collectors of the cascode transistors are separated, the circuit can be used as a gate to transmit data to one of several possible destinations.

A weak point in many high-speed circuit families relates to power drivers. These fall into two classes: A driver for large numbers of logic blocks, and a driver capable of driving one or more transmission lines. Both of these requirements can be met by using tunnel diodes. If the load to be driven is shunted by a tunnel diode and the negative resistance of the diode matches the resistance of the load, the diode acts as a current amplifier. Figure 5 shows a line driver using this technique; a pair of diodes is added to any logic block which then can drive up to four transmission lines. This same diode pair is also used as the clamp for a non-orthogonal wired AND; i.e., more than one circuit delivering current at one time.

The register position for this circuit family consists of a simple combination of transistors and tunnel diodes. It has two input lines, one for data and one for a gating pulse. Whenever a pulse is present on the gate input, the data on the data input enters the register and is latched. The register incorporates an indicator and can drive up to three transmission lines.

In this speed range, performance is strongly dependent upon packaging. The packaging technique used is based upon unencapsulated transistors and laminated printed wiring cards. The transistors are .050" square chips with 1-mil wires. Up to six of these are assembled on a circuit module which is .2" by .3". The addition of precision resistors makes the height of this module .4". Up to 240 of these modules have been assembled on a 9" x 10" laminated card. The internal layers in the card are used as a low-impedance dc distribution system and the outer surfaces are reserved for signal wiring. The associated problems of noise on signal wiring and on the dc distribution system will be discussed.

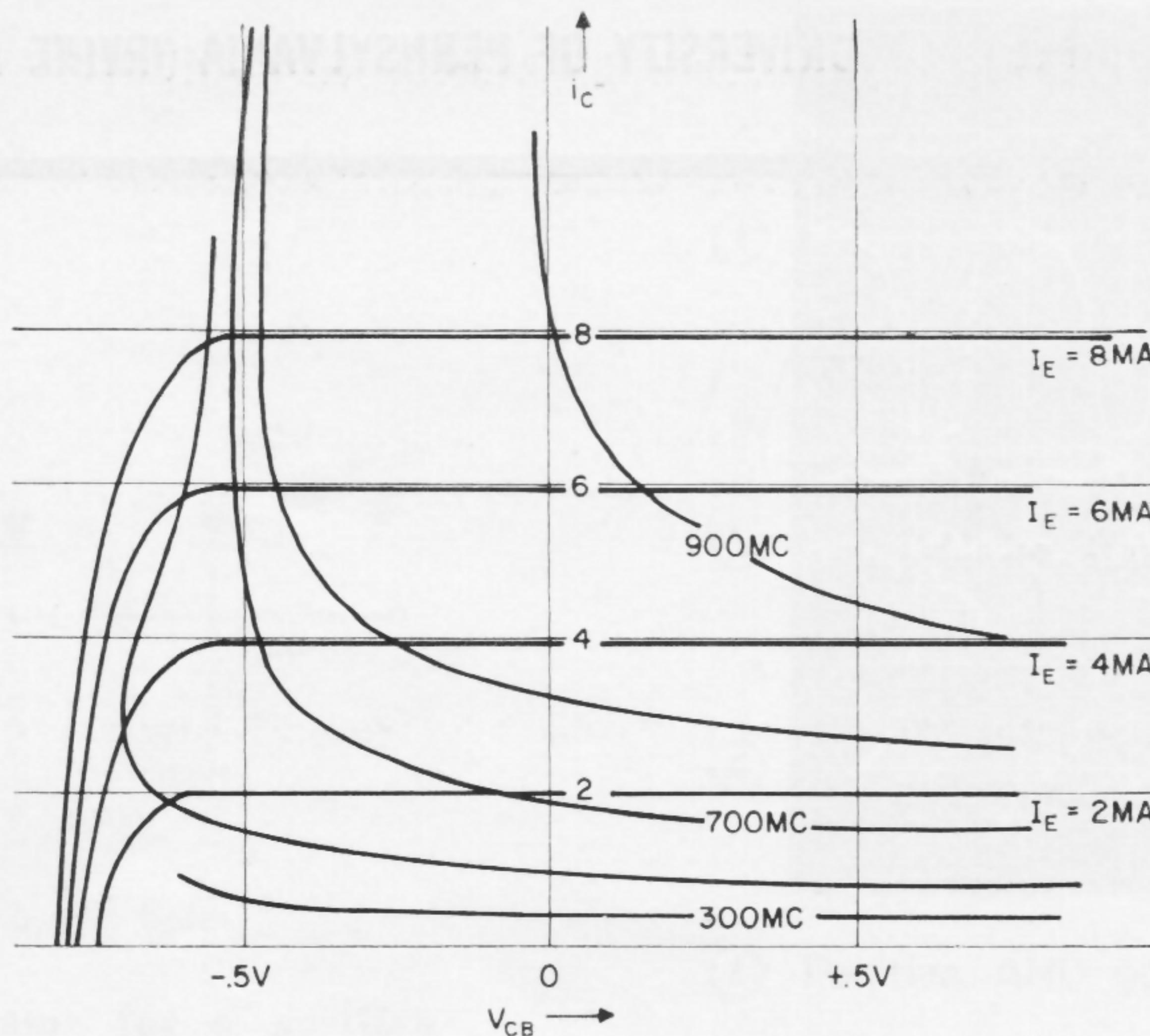


Figure 1—Constant gain bandwidth and constant emitter current curves on the  $i$ ,  $V_{CB}$  plane, demonstrating that the frequency response is high in the forward-biased collector region.

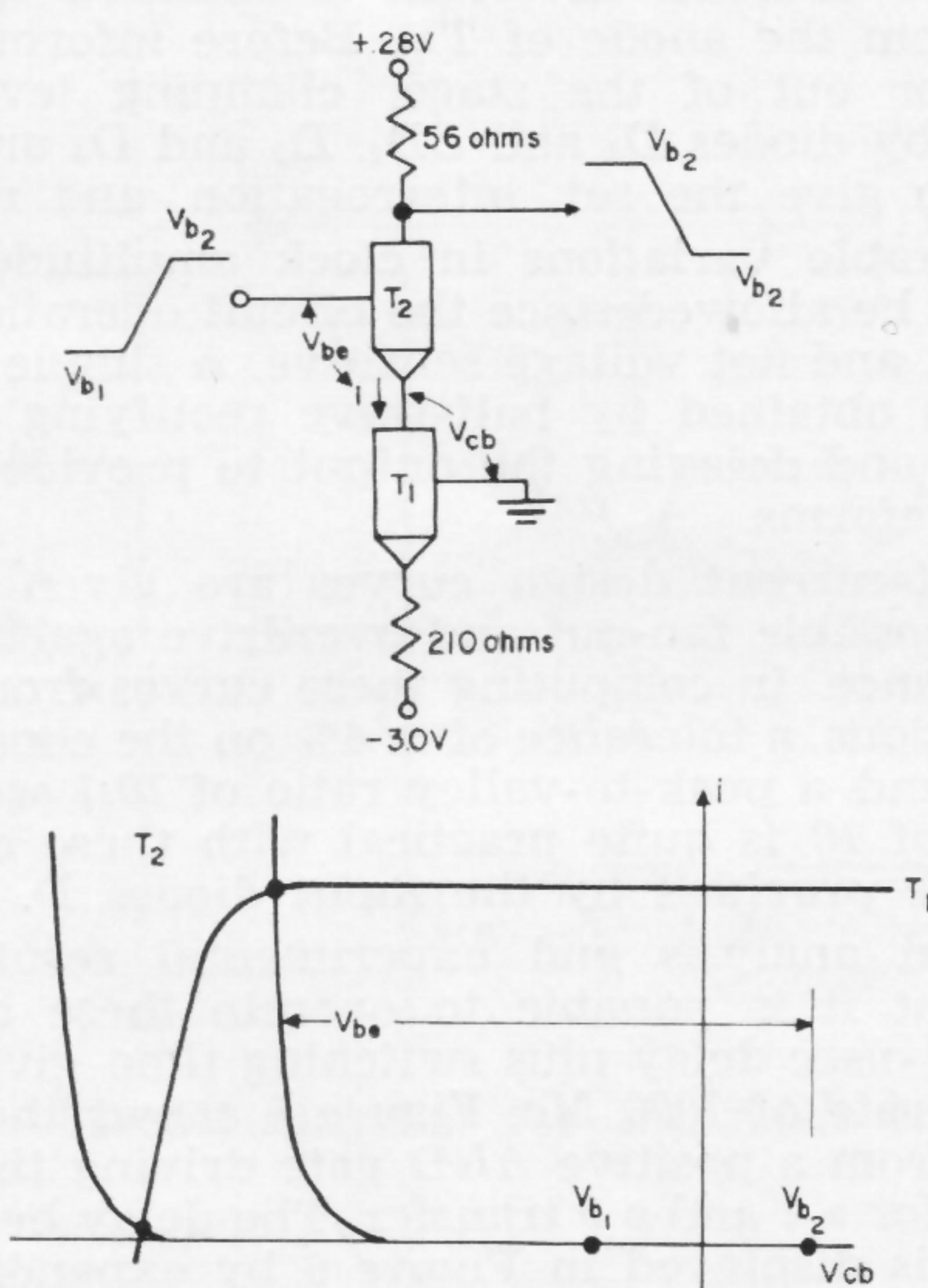


Figure 2—(a—top) Basic cascode inverter. (b—bottom) Load-line diagram showing the operating points for voltage levels  $V_{b1}$  and  $V_{b2}$ .

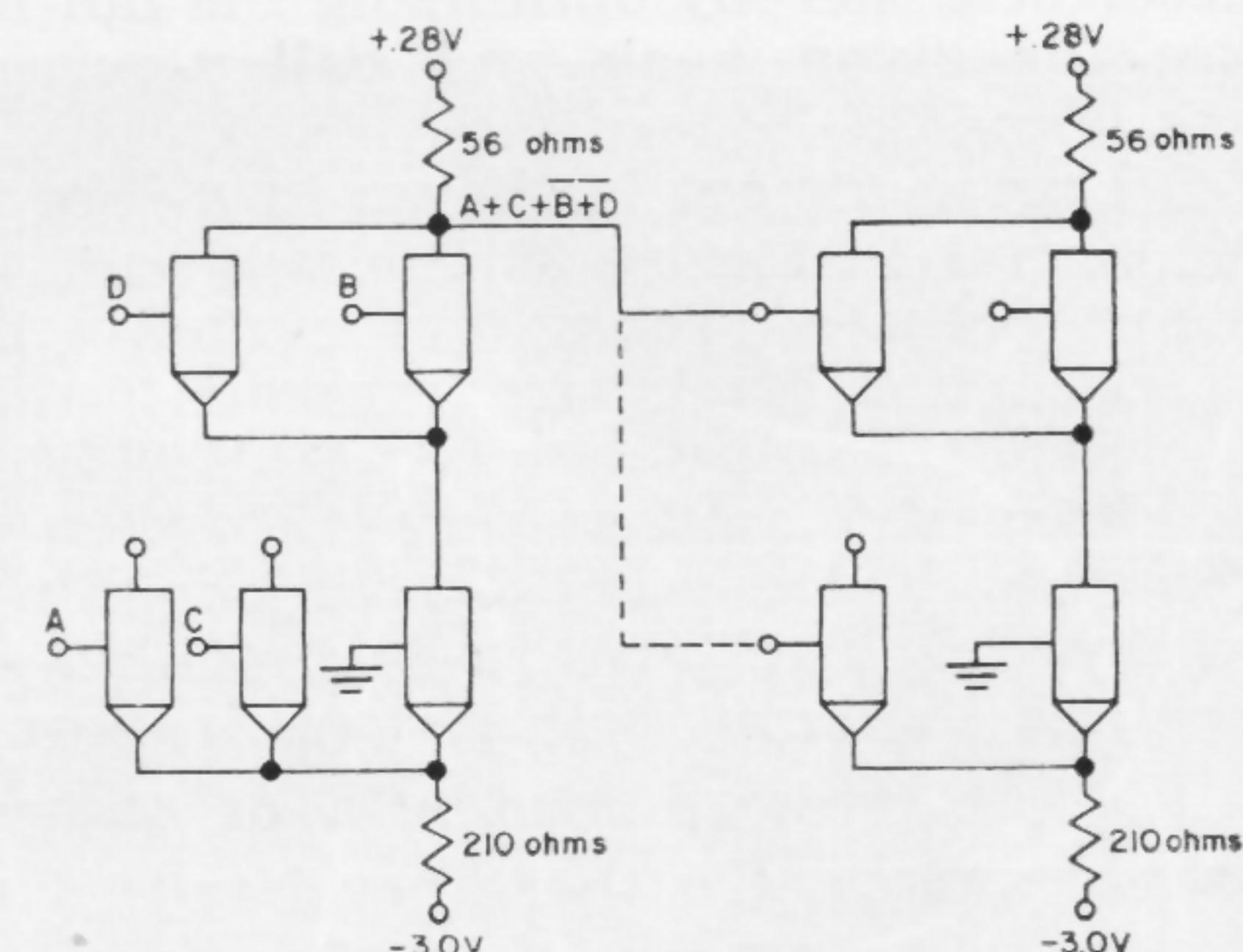


Figure 3—Implication function obtained by paralleling transistors as shown. It will be noted that the collector drives either the top or bottom base directly.

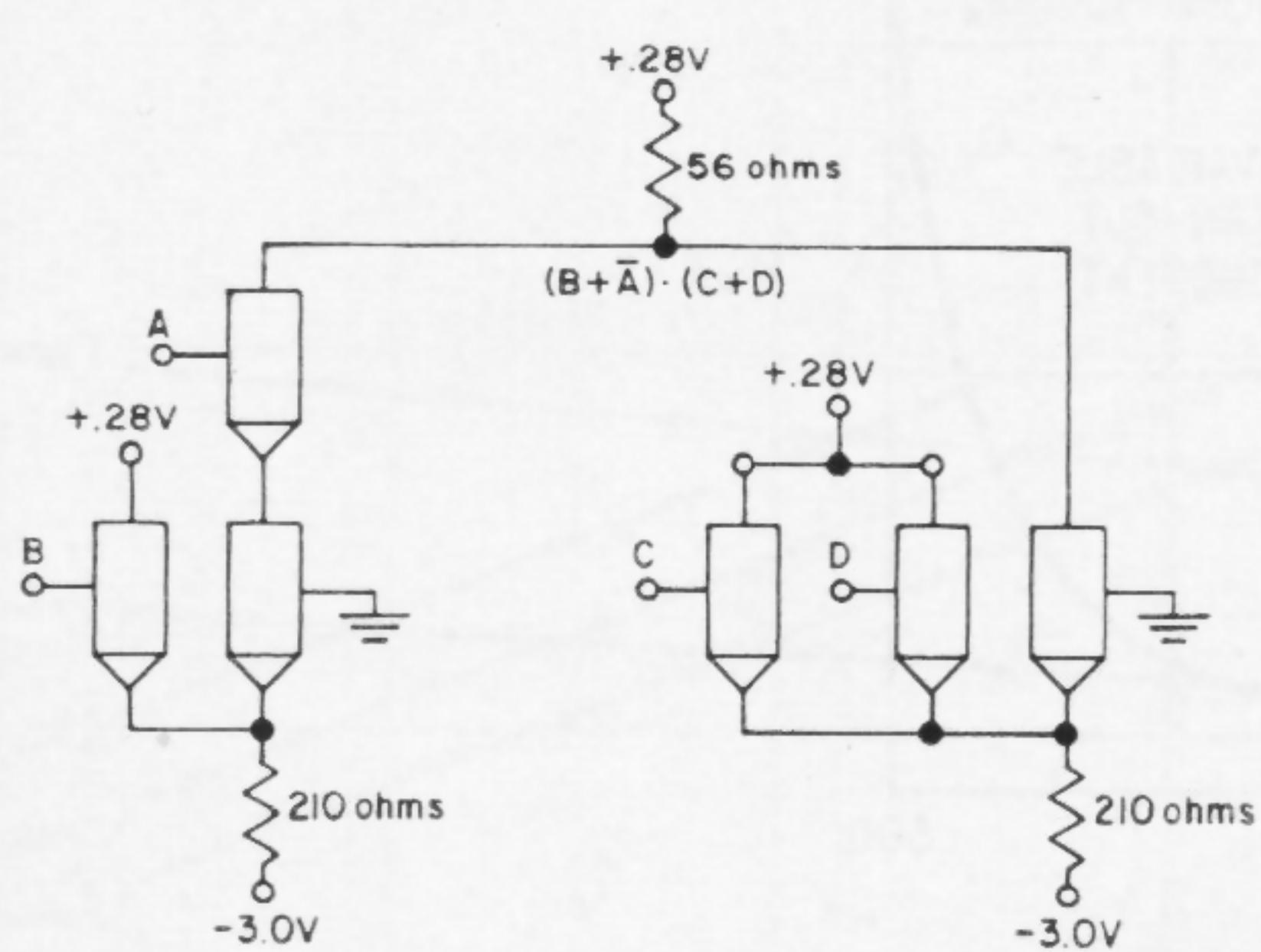


Figure 4—Collectors of a standard current-switching block and an implication-function block wired together to form an AND function.

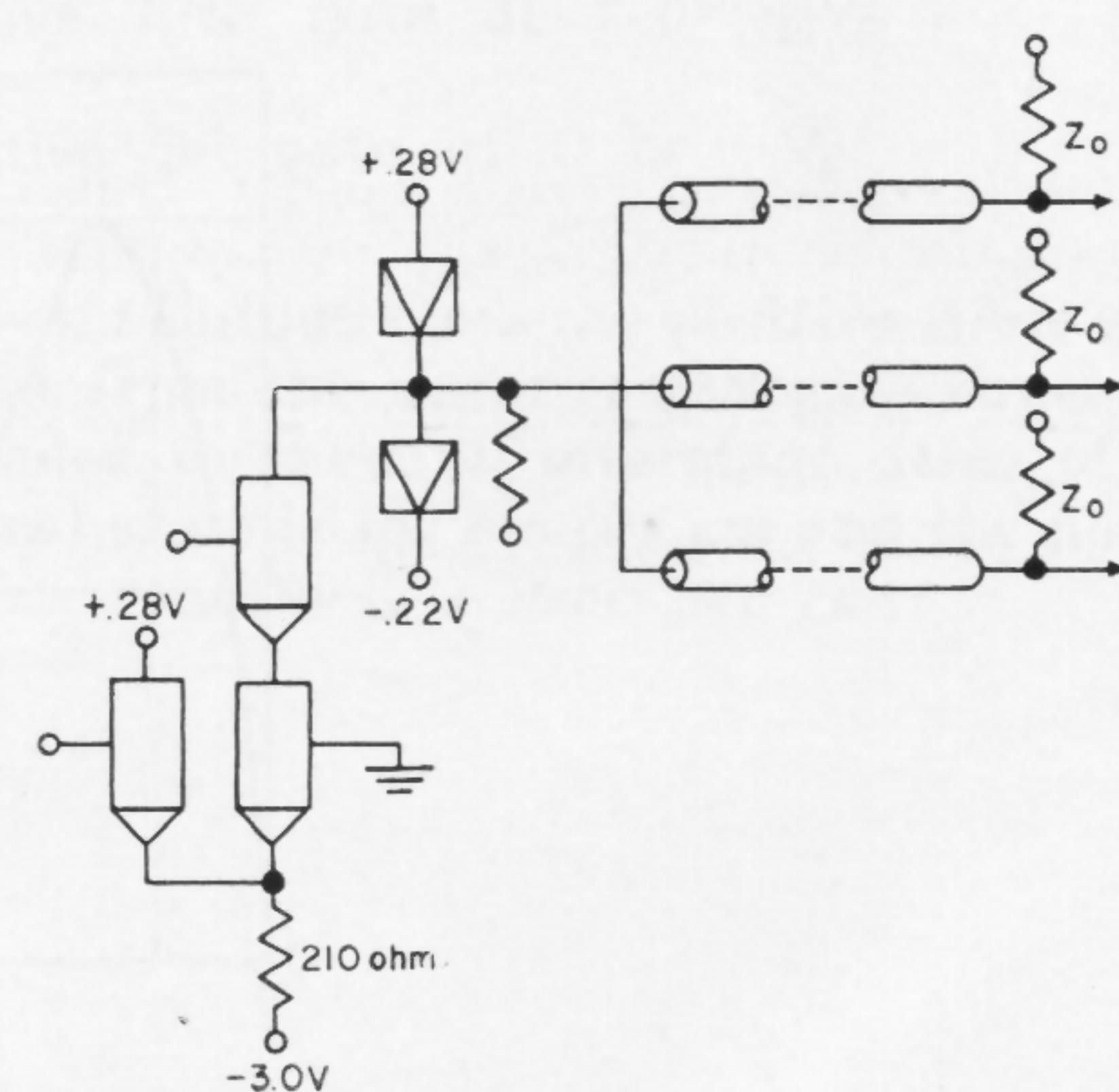


Figure 5—A pair of tunnel diodes connected to a standard logic block which becomes the line driver.

## SESSION V: High Speed Switching

### TM 5.2: Kilomegacycle Tunnel-Diode Logic Circuits

B. E. Sear

Remington Rand Univac, Sperry Rand Corporation  
Blue Bell, Pa.

SINCE THE ADVENT of the tunnel diode, several ways of using its  $V-I$  characteristic to perform logical decisions have been suggested; Figure 1. Invariably, the tolerance requirements placed on a circuit producing a reasonable fan-in/fan-out are impractical and therefore make a large system difficult to design. In general, when the tunnel diode is operated in current mode, there is an optimum fan-out current dependent on peak and valley current tolerances which is hard to achieve. The output current from one stage and the input current to a succeeding stage are usually proportional to the high state voltage which can vary from 350 to 550 mv for germanium units. By allowing a reasonable specification on the voltage characteristics of the tunnel diode considerable output current is lost in tolerance. This dependence of input and output currents on the voltage characteristic has been eliminated by circuits to be described, thereby optimizing the fan-in/fan-out characteristics for given peak and valley-current tolerances; Figures 2 and 3.

The *AND-OR* arrangement is shown in *a-b* of Figure 2, and the *NOR* circuit in Figure 3. The principle of operation is the same for both circuits, but to obtain the inversion, certain clamping levels are included in the *NOR* circuit.

The tunnel diode is biased at point *A* by the constant current  $I_B$ . The constant current  $I_{in}$ , which is made large enough to switch *TD* in Figure 2*a* to the high state, can flow in *D* or *BD*. If the input voltage to *D* is more negative than  $\overline{V_{DF}} + V_p$ , the backward diode *BD* is reverse biased and *TD* does not switch. On the other hand, if the input voltage to *D* is more positive than  $-\overline{V_{DF}} + V_{BDF} + \overline{V_p}$ ,  $I_{in}$  conducts into *TD* switching it to the high state. By alter-

nating the interconnection, as shown by circuit *a* and *b* of Figure 2, compatible levels are obtained for *AND-OR* operation.

Constant bias currents are applied to the anode and cathode of *TD* in Figure 3, and an input current  $I_{in}$  via *BD*<sub>1</sub> to the cathode. Inversion is obtained by taking the output from the anode of *TD*. Before information can be read in or out of the stage, clamping levels must be provided by diodes *D*<sub>4</sub> and *BD*<sub>2</sub>. *D*<sub>2</sub> and *D*<sub>4</sub> are clocked on and off to give the set, interrogation, and reset periods.

Considerable variations in clock amplitude and wave-shape can be allowed since the circuit operation is current dependent and not voltage sensitive. A simple yet effective clock was obtained by half-wave rectifying a sine-wave generator and delaying the output to provide overlapping clock waveforms.

Constant-current design curves are given in Figure 4 showing possible fan-out and overdrive against peak current tolerance. In computing these curves from the *worst-case* equations, a tolerance of  $\pm 4\%$  on the constant-current supplies, and a peak-to-valley ratio of 10:1 were assumed. A fan-in of 10 is quite practical with these circuits since isolation is provided by the input diodes *D*.

Transient analysis and experimental results have revealed that it is possible to operate these circuits with less than 1-nsec delay plus switching time giving an effective digit rate of 1000 Mc. Figure 5 shows the waveforms obtained from a positive *AND* gate driving three negative *OR* gates for a 1 and a 0 transfer. The delay between stages of 1 nsec is displayed in Figure 6 by expanding the time scale and superimposing the 1 output for the positive *AND* gate on the 0 output for the negative *OR* gate.

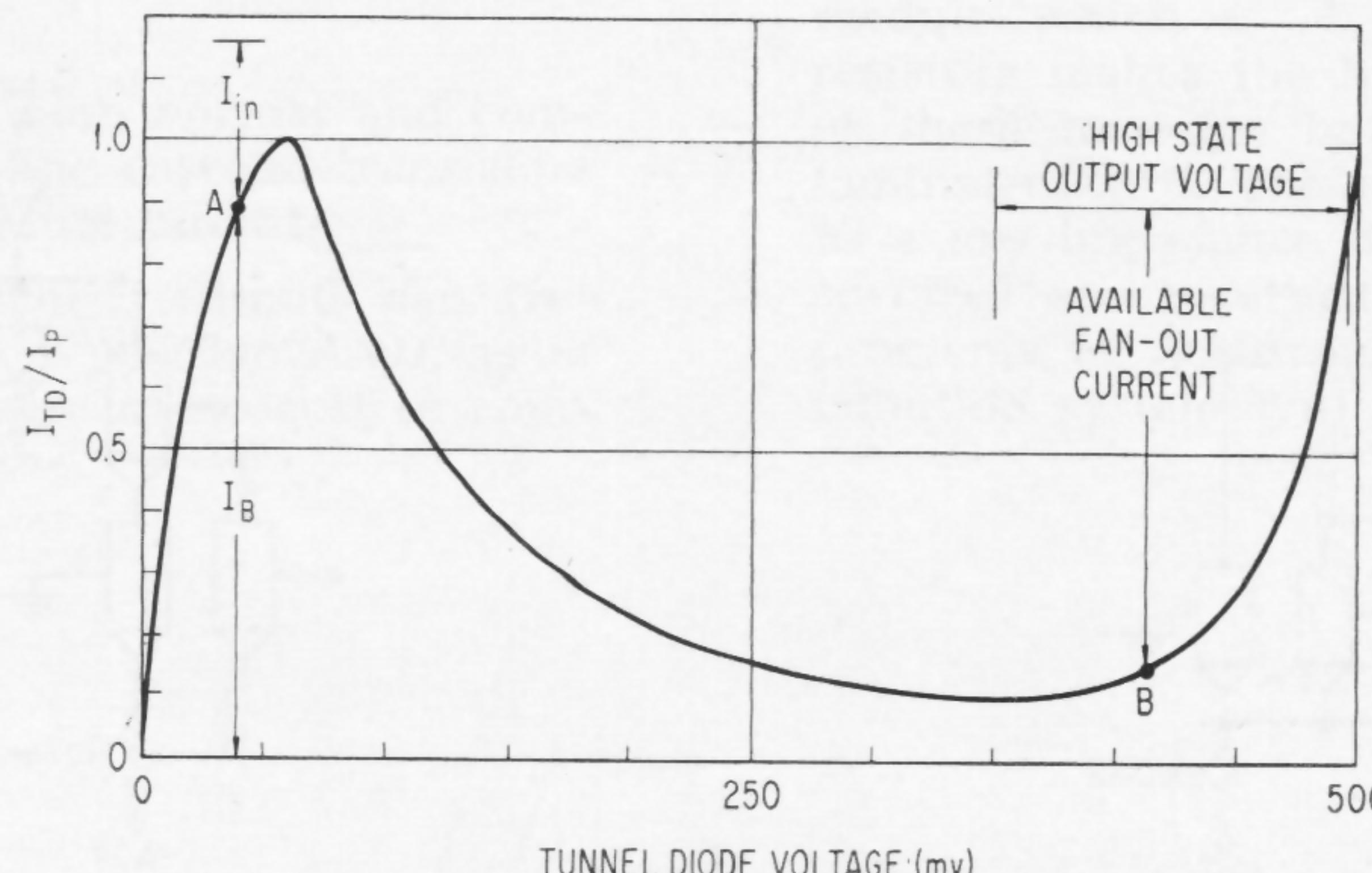
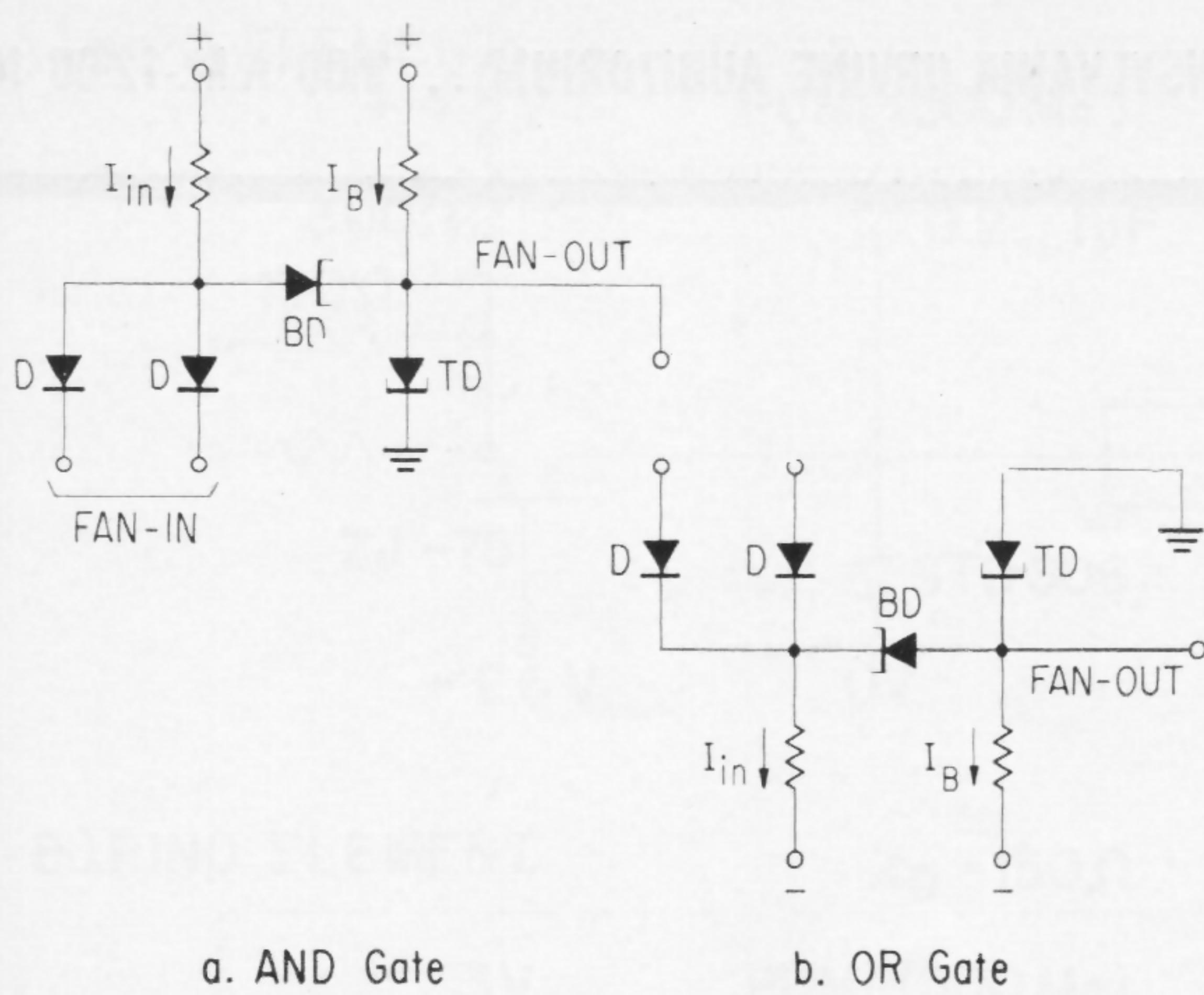


Figure 1—Normalized tunnel-diode *VI* characteristic showing operating points. The high state voltage can vary as much as  $\pm 15\%$  for a 90% yield.



a. AND Gate

b. OR Gate

Figures 2a and b—Circuit diagrams for a positive AND gate and a negative OR gate. The forward voltage characteristic of the coupling diode  $D$  is specified by  $V_{DF}$  at maximum  $I_{in}$  and  $V_{DF}$  at the break point, and the backward diode  $BD$  by  $O$  and  $VBDF$  at maximum  $I_{in}$ .

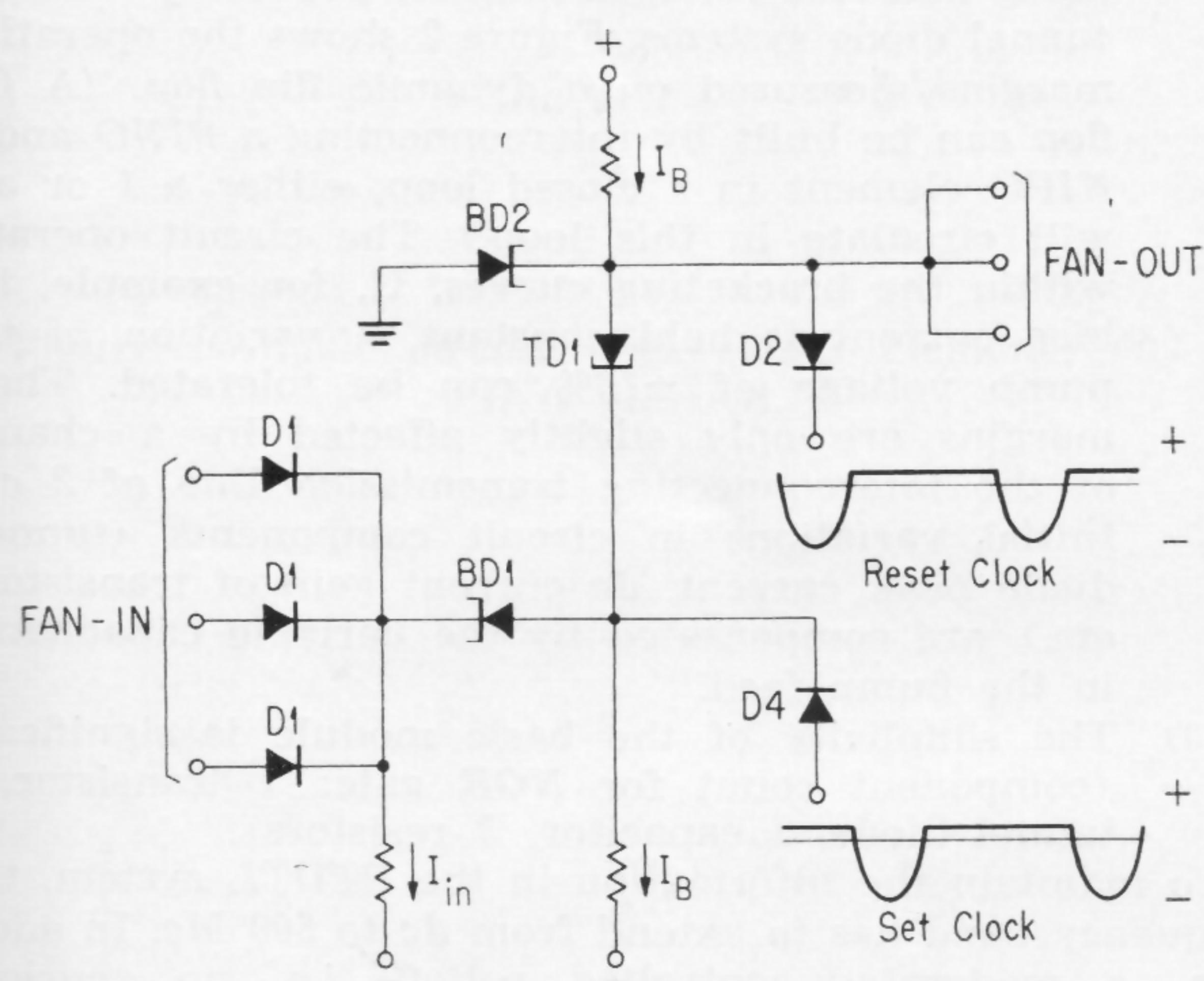
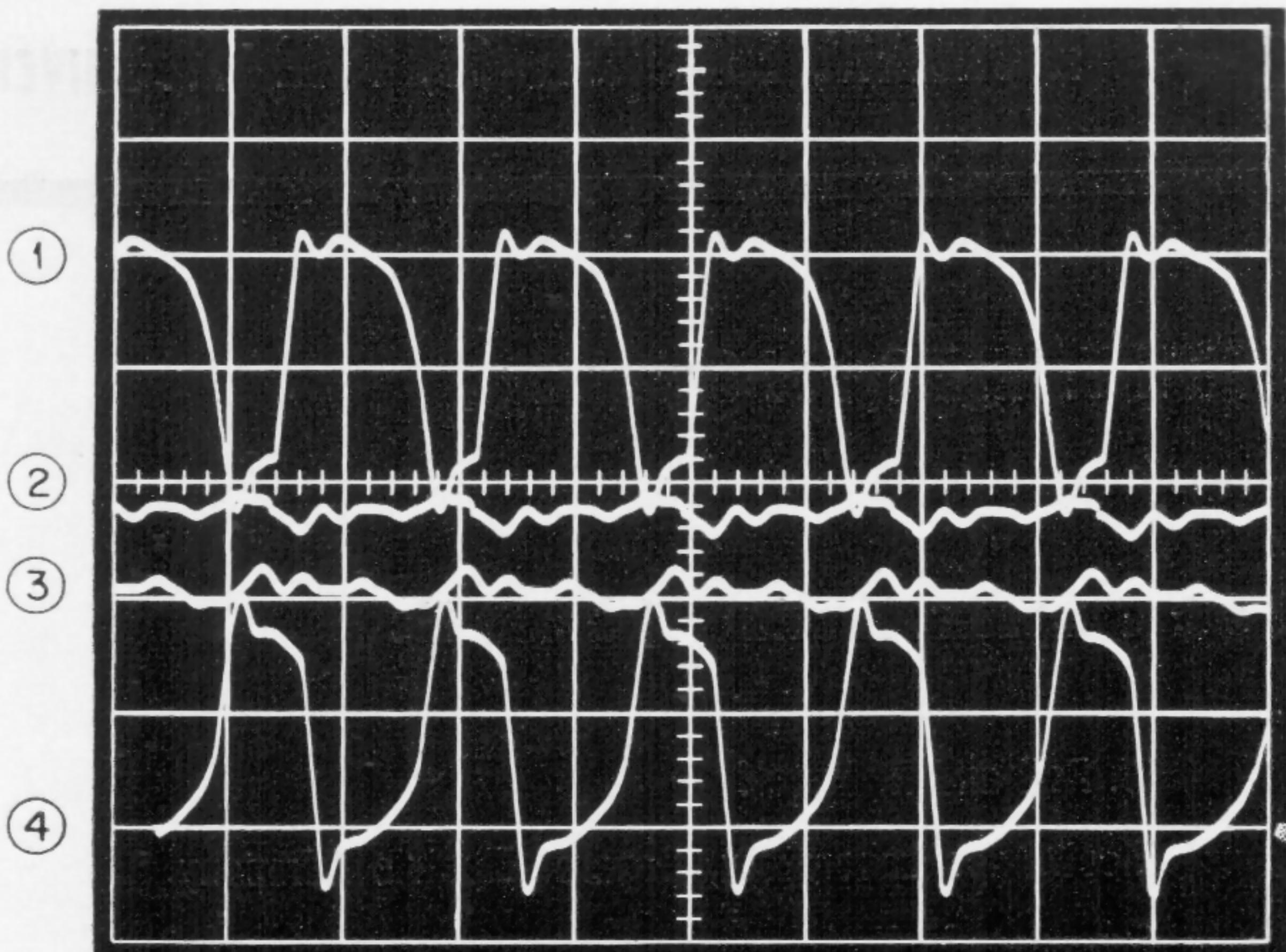
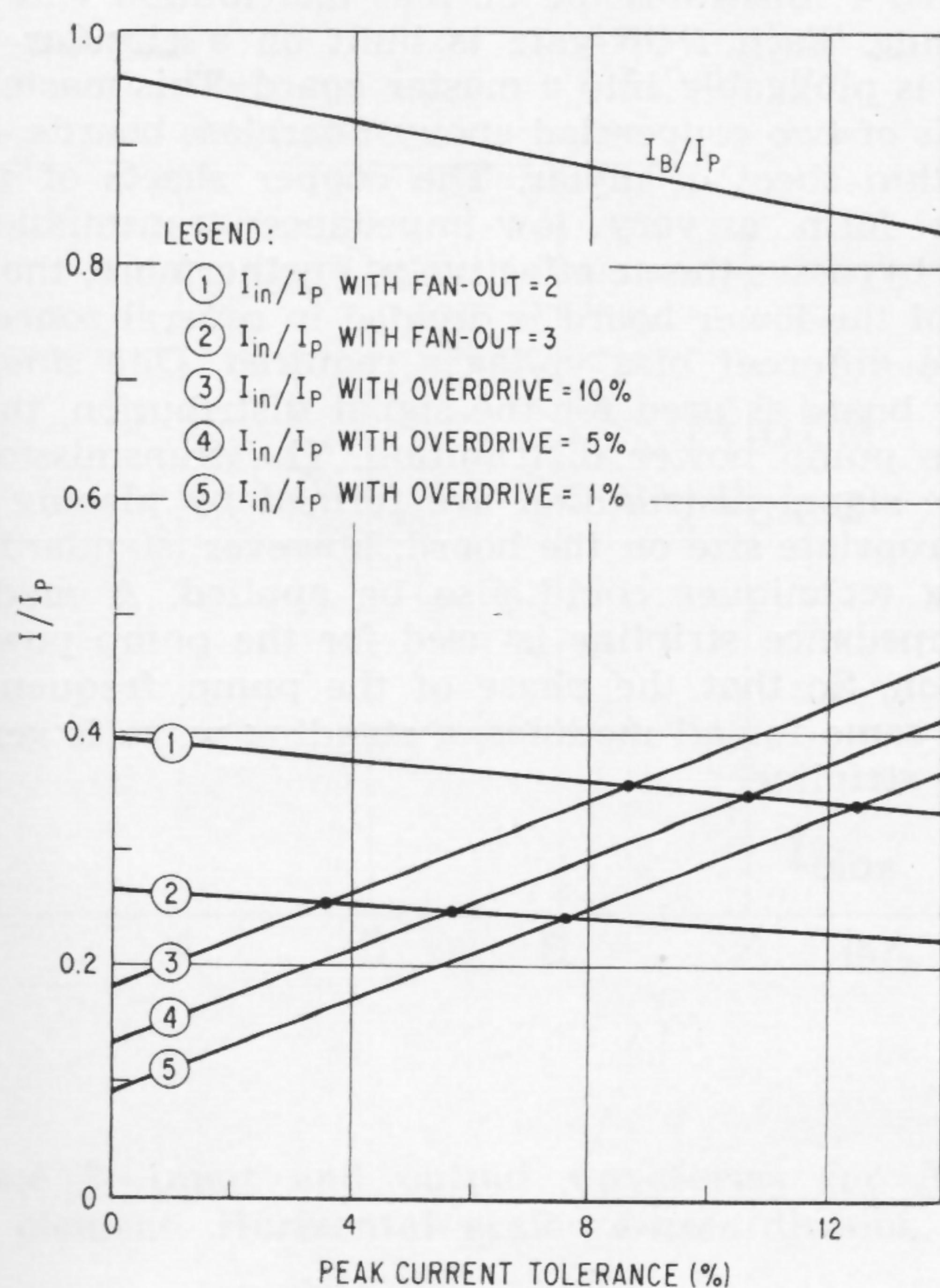


Figure 3—Circuit diagram for the NOR circuit.



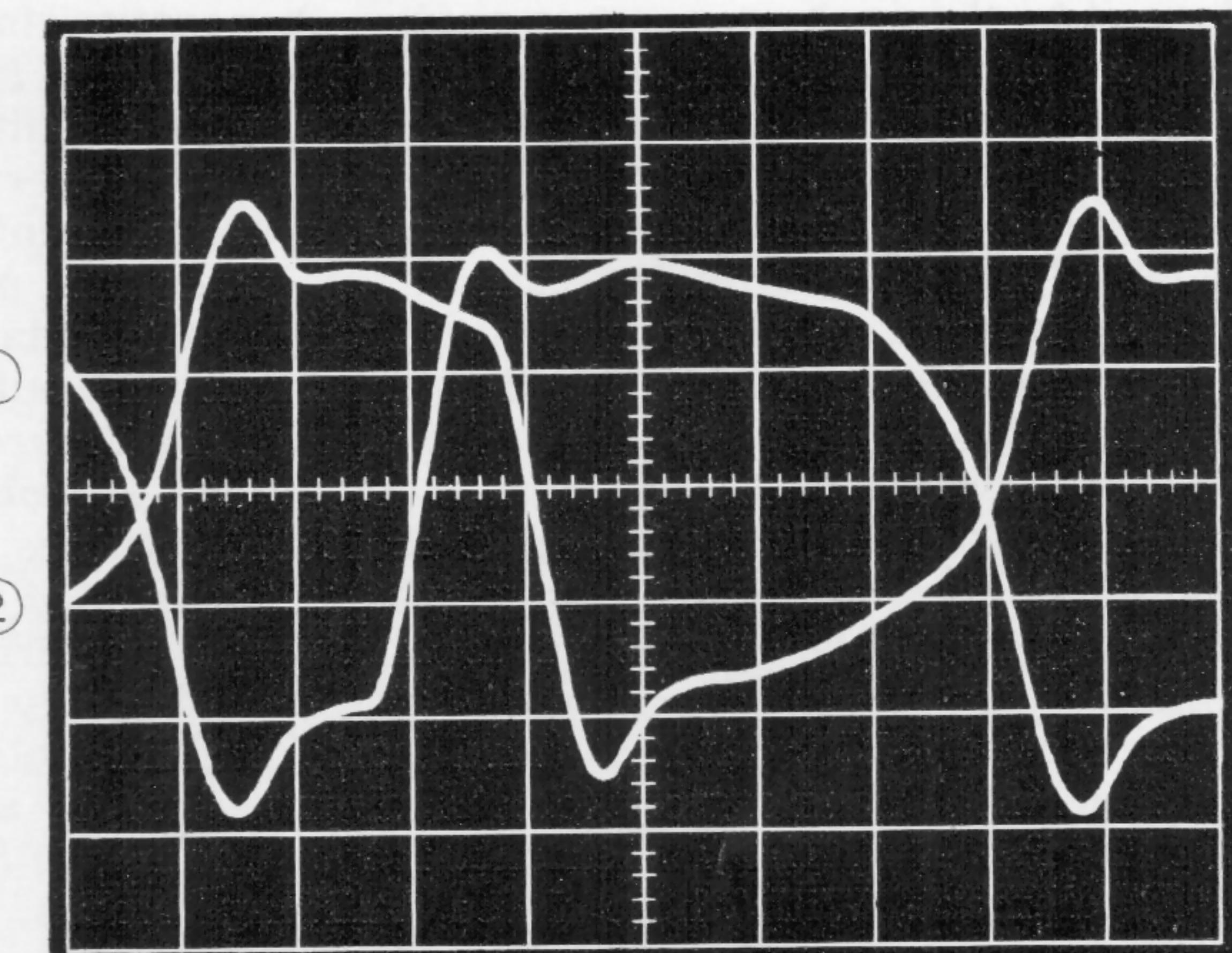
① Positive AND gate at 1 level or  $+V_F$

② Negative OR gate at 1 level or  $-V_P$

③ Positive AND gate at 0 level or  $+V_P$

④ Negative OR gate at 0 level or  $-V_F$

Figure 5—A positive AND gate driving a negative OR gate at a 135-Mc clock rate and an interstage delay of 1 nsec. The vertical scale is 200 mv per cm and the horizontal scale is 4 nsec per cm.



① Positive AND gate at 1 or  $+V_F$

② Negative OR gate at 0 or  $-V_F$

Figure 6—A 1 output from the positive AND gate and a 0 output from the negative OR gate superimposed and expanded to show an interstage delay of 1 nsec. The vertical scale is 100 mv per cm and the horizontal scale is 1 nsec per cm.

(Left)

Figure 4—Constant current design curves showing effect of fan-out and overdrive against peak current tolerance for the AND-OR circuit.

## SESSION V: High Speed Switching

### TM 5.3: Computer Circuitry\* for 500 Mc

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Electronics Laboratory, General Electric Company  
Syracuse, N. Y.

THE PUMPED TUNNEL DIODE—TRANSISTOR LOGIC (PTDTL) system to be described processes data at a rate of 500-Mc by using a hybrid transistor—tunnel diode circuit which combines the high-speed capabilities of both the transistor and the tunnel diode; Figure 1. The transistor provides the isolation between several input channels and the unidirectionality of information flow. However, no gain is required from the transistor and therefore operation close to its cutoff frequency is possible. The tunnel diode which has, as a two-terminal device, no intrinsic isolation capability, provides the gain and the threshold action. Reclocking is achieved by *pumping* the tunnel diode with a 500-Mc sine wave. In the absence of an input signal, the tunnel diode in Figure 1a switches on every positive half cycle of the pump frequency from its bias point below the peak voltage into the high-impedance region. A negative input signal on one or both inputs prevents the diode from switching. Logically, a NOR gate results. The circuit in Figure 1a requires *Negative Input* pulses but generates *Positive Output* pulses (NIPO-element); a complementary element (PINO) is provided simply by using an *npn*-transistor instead of a *pnp* and by inverting the polarity of the tunnel diode; Figure 1b. Typical input and output waveforms for a NIPO element are shown in Figure 2. The gate performs the operation  $C = A+B$ , where  $A = 01110001$ ,  $B = 01010101$  and  $C = 10001010$ . Since the PINO element fires on the negative half cycle of the pump frequency, two levels of logic can be performed during a full pump cycle and data can actually be processed at a 1-kMc rate. A third basic building block, a 1:1 inverting transformer (electrical inverter) is used where a PINO (NIPO) element feeds another PINO (NIPO) element. With these three building blocks any complex logic system can be built.

In performing complex logical operations, the following advantages of the PTDTL system are of special interest:

- (1) Individual gates are interconnected by matched microstrip-type transmission lines. The length of these lines is not critical, since the logic element provides excellent reclocking. Under the assumption that the bias and pump voltages are held constant,

\* The following components were used in constructing this circuit: Fairchild 2N917 (*npn*) and General Electric ZJ-75 (*pnp*) transistors, and General Electric STD606 diodes with a peak current of 10 ma and capacitance of 1 pf.

a phase error of  $\pm 60^\circ$  of the input signal can be tolerated.

- (2) Tolerances on circuit components as well as on pump and bias voltages compare favorably with all-tunnel diode systems. Figure 3 shows the operating margins measured on a dynamic flip flop. (A flip flop can be built by interconnecting a PINO and a NIPO element in a closed loop; either a 1 or a 0 will circulate in this loop.) The circuit operates within the bracketing curves. If, for example, the bias current is held constant, a variation of the pump voltage of  $\pm 16\%$  can be tolerated. These margins are only slightly affected by a change of the interconnecting transmission line of 2 cm. Initial variations in circuit components (tunnel-diode peak current, *dc* current gain of transistors, etc.) are compensated by the variable capacitance in the pump feed.
- (3) The simplicity of the basic module is significant (component count for NOR gate: 1 transistor, 1 tunnel diode, 1 capacitor, 3 resistors).

To maintain the information in the PTDTL system, the frequency band has to extend from *dc* to 500 Mc. In addition, a moderately-controlled rolloff, i.e. no spurious resonances should exist to approximately 1.5 kMc. A combination of lumped and distributed circuit techniques was adopted to meet these bandwidth requirements.

Figure 4 illustrates the *dc* bias distribution and the *ac*-bypassing. Each NOR-gate is built on a circular module which is pluggable into a master board. This master board consists of two copperclad epoxy-fiberglass boards, isolated by a thin sheet of mylar. The copper sheets of the two boards form a very low-impedance transmission line which bypasses the *ac* effectively. Furthermore, the copper sheet of the lower board is divided in several zones carrying the different bias voltages required. One side of the master board is used for the signal distribution, the other for the pump power distribution. The transmission lines for the signal distribution are formed by placing a wire of appropriate size on the board; however, standard photo-etching techniques could also be applied. A moderately low-impedance stripline is used for the pump power distribution. So that the phase of the pump frequency will be the same for all modules, a standing wave is generated on the stripline.

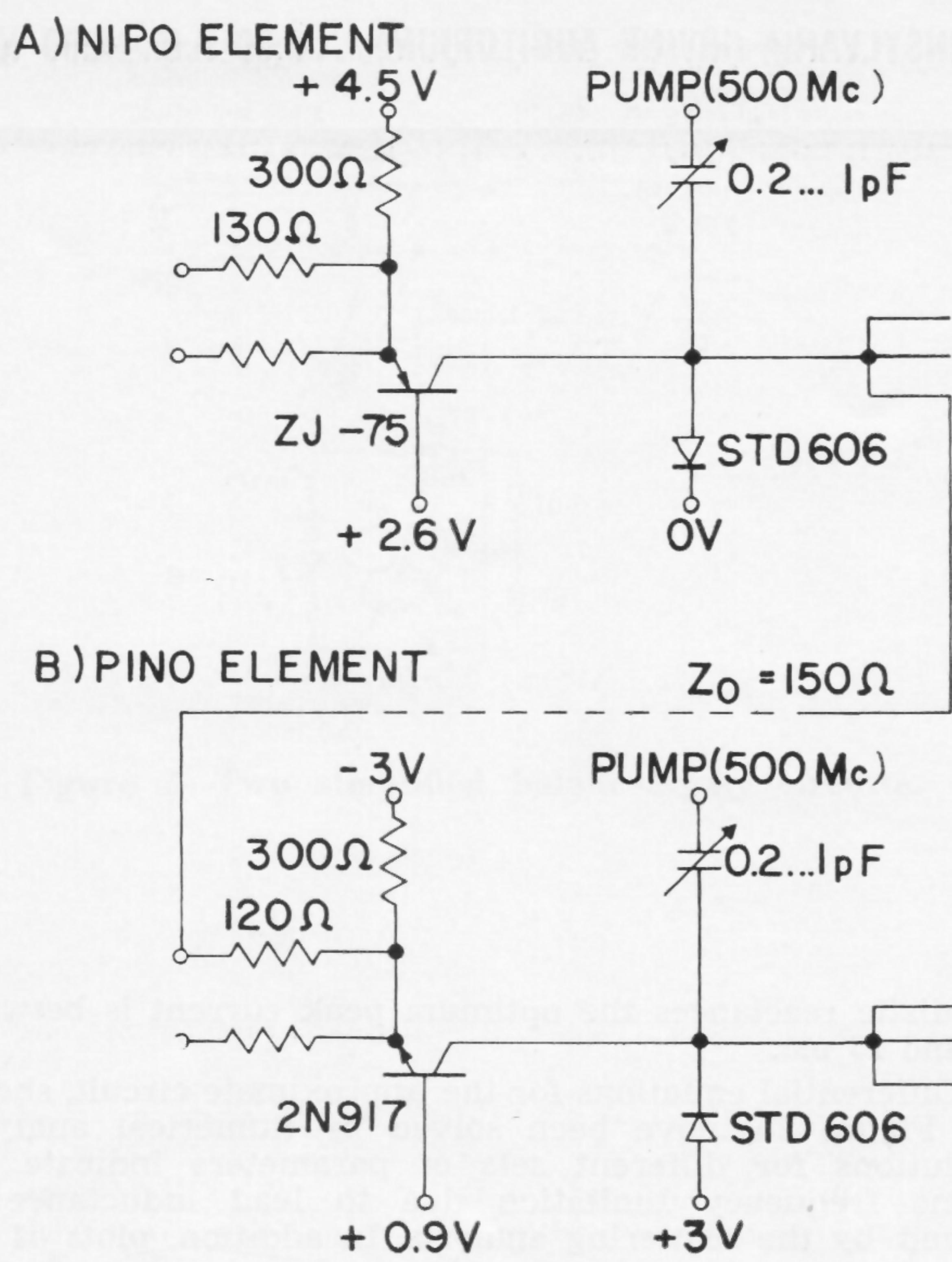


Figure 1—Basic circuit: (a)—NIPO element; (b)—PINO element.

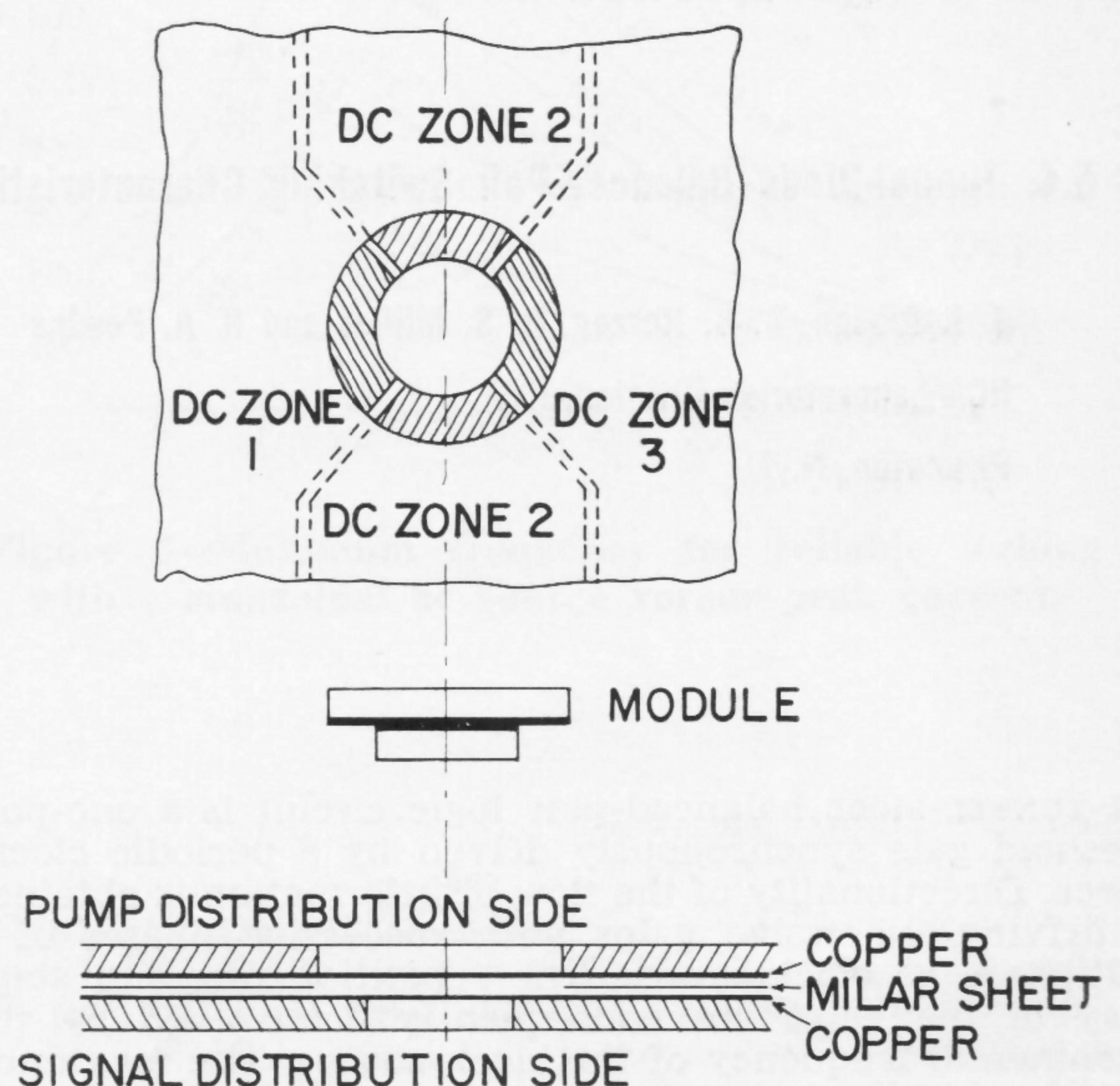


Figure 3—Pump and bias current tolerances for a dynamic flip flop.

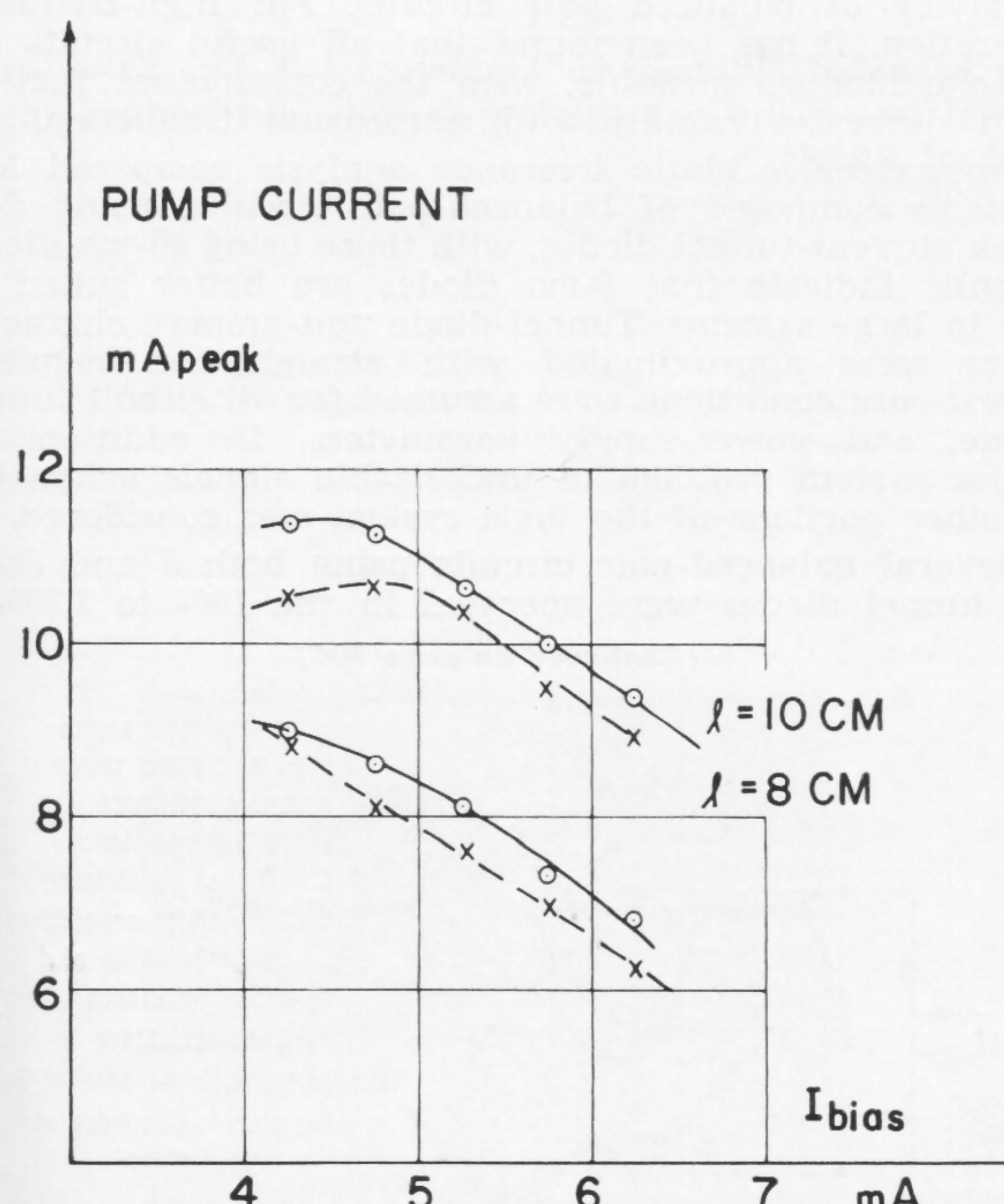


Figure 2—Input and output waveforms for NIPO element. Horizontal scale: 4-nsec/division.

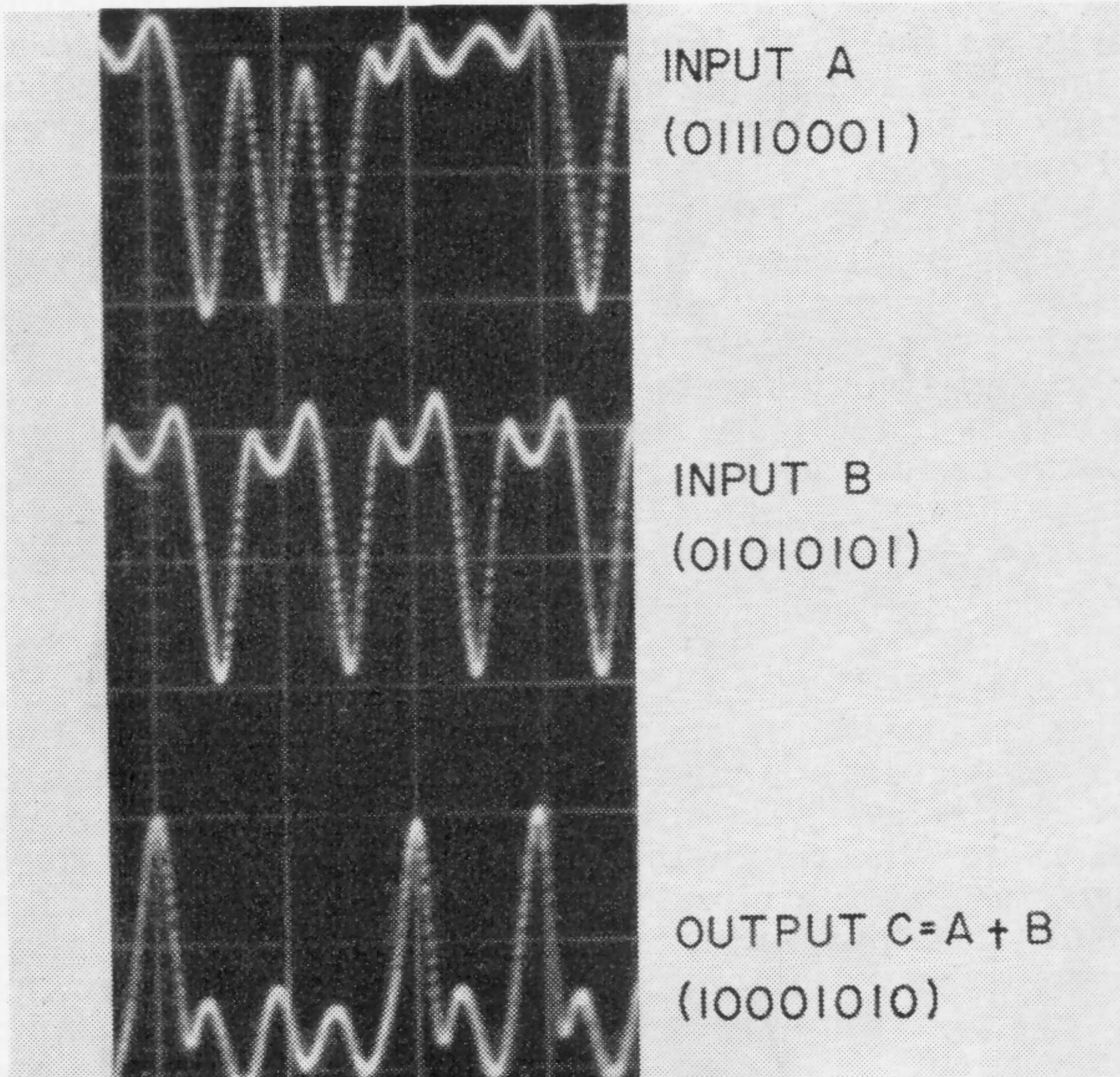


Figure 4—Plots illustrating *dc* distribution and *ac* bypassing.

## SESSION V: High Speed Switching

## TM 5.4: Tunnel-Diode Balanced-Pair Switching Characteristics

J. J. Gibson, G. B. Herzog, H. S. Müller and R. A. Powlus

RCA Laboratories Division, RCA

Princeton, N. J.

THE TUNNEL-DIODE balanced-pair logic circuit is a one-port threshold gate synchronously driven by a periodic *clock-source*. Directionality of the flow of information is obtained by driving successive gates with successive phases of a multiphase *ac clock-source*. The repetition rate and stage delay of the gates are consequently determined by the fundamental frequency of the *clock-source*. The maximum frequency at which the circuit can operate reliably is limited by the effects of unavoidable reactances.

The balanced-pair circuit, including approximate reactances, is shown in Figure 1. A balanced *ac* and *dc* source,  $I$ , applied across the source resistors  $r'$ , drives both diodes in the same direction. A logic input, represented by an equivalent voltage source  $V$ , in series with the equivalent load  $R_o$ , tends to drive the diodes in opposite directions. At the beginning of the *ac* cycle, both diodes are in their low-voltage positive-resistance regions and are driven toward their negative-resistance regions by the *ac* power source. The logic voltage  $V$  favors one of the diodes, say  $TD 1$ , with the consequence that  $TD 1$  reaches its negative resistance region before  $TD 2$ . As  $TD 1$  goes over its peak, it sends an inhibiting signal to  $TD 2$ , which hopefully arrives in time with sufficient strength to turn back  $TD 2$  from its negative resistance region. As  $TD 1$  enters its negative resistance region, a regenerative process starts, switching  $TD 1$  to its high-voltage region and driving  $TD 2$  deeply back into its low-voltage positive resistive region. As a result, a large output voltage having the same polarity as the logic input voltage  $V$ , is obtained across the load  $R_o$ . Later in the *ac* cycle,  $TD 1$  is reset to its low-voltage positive-resistance region and the process can start over again.

The critical part is the locking process which occurs during the small fraction of the *ac* cycle when the diodes go over their peaks. The success of the locking process depends upon the intensity and speed with which the diodes can communicate with each other during this duration over the lossy reactive network shown in Figure 1. Unsuccessful locking results if the diode which is not supposed to switch, say  $TD 2$ , goes too far into its negative resistance region, with the consequence that both diodes may end up in their high voltage states, possibly after a few cycles of oscillations.

The simplified circuit shown in Figure 2a, in which the reactances have been approximated by transmission lines, has been used in an analysis based on the concept of wave scattering. With this analysis, an approximate expression for the maximum frequency has been derived, indicating that the circuit can operate at very high frequencies if output pulses of unreliable shapes are tolerated. However, the maximum frequency for reliable operation with useful output pulses and a sinusoidal *clock-source* is only about 250 Mc at the present state of device and circuit technology. The maximum frequency for reliable operation, as a function of the peak current of the tunnel diodes, is illustrated in Figure 3. An attempt to optimize the circuit parameters indicates that for a wide range of

realistic reactances the optimum peak current is between 5 and 15 ma.

Differential equations for the approximate circuit, shown in Figure 2b, have been solved by numerical analysis. Solutions for different sets of parameters indicate the same frequency limitation due to lead inductance as found by the scattering analysis. In addition, plots of the circuit currents and voltages give a phenomenological insight into the behavior of the circuit. Figure 4a shows the plot of branch current against tunnel diode voltage for the upper and lower halves of the circuit illustrated in Figure 2b, with an input current of 4% of the peak diode current and a load of 40% of the peak diode current at 150 Mc. Although it can be shown that this circuit is unstable for the circuit parameters chosen, the input is large enough to inhibit oscillations. An attempt to load the circuit to 50% of the diode peak current results in oscillations in the circuit, although initially only one of the diodes switches, as shown in Figure 4b. Over 200 solutions of the differential equations indicate that the normal stability criterion as applied to tunnel diode oscillators is a good first approximation for predicting behavior of balanced pair circuits. For high-frequency operation, it has been found that all useful circuits will be classified as unstable, with the consequence that the gain decreases rapidly with increasing frequency.

An extensive static tolerance analysis compared logic systems composed of balanced-pair circuits, using 5-ma peak current-tunnel diodes, with those using 50-ma diodes. Results indicate that 5-ma diodes are better suited for use in large systems. Tunnel-diode volt-ampere characteristics were approximated with straight-line segments. Worst-case conditions were assumed for all circuit tunnel-diode, and power-supply parameters. In addition, the major system problem of undesirable signals originating in other portions of the logic system was considered.

Several balanced-pair circuits using both 5 and 50-ma Ge tunnel diodes were operated in the 150- to 1,200-Mc

[Continued on page 106]

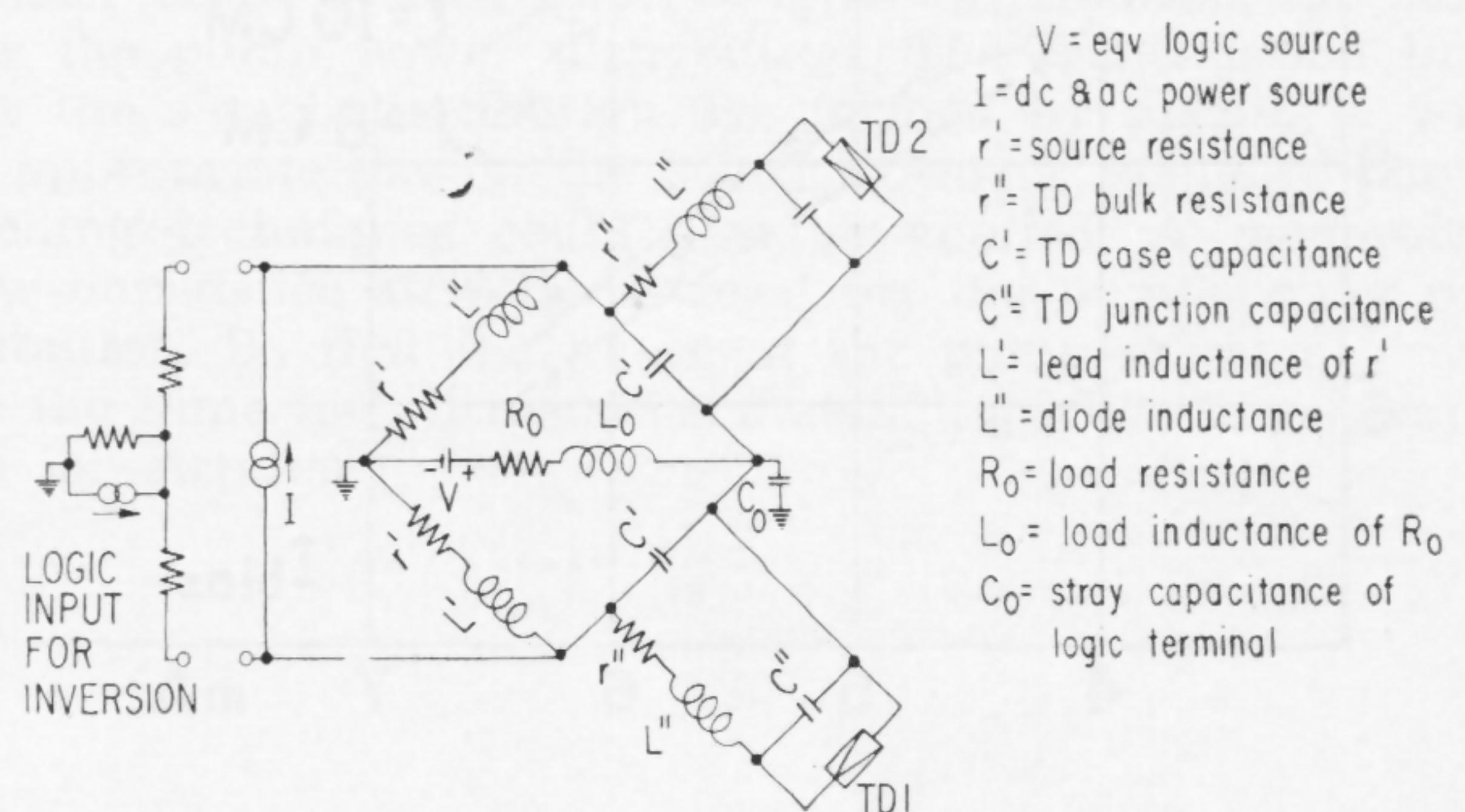


Figure 1—The balanced-pair circuit.

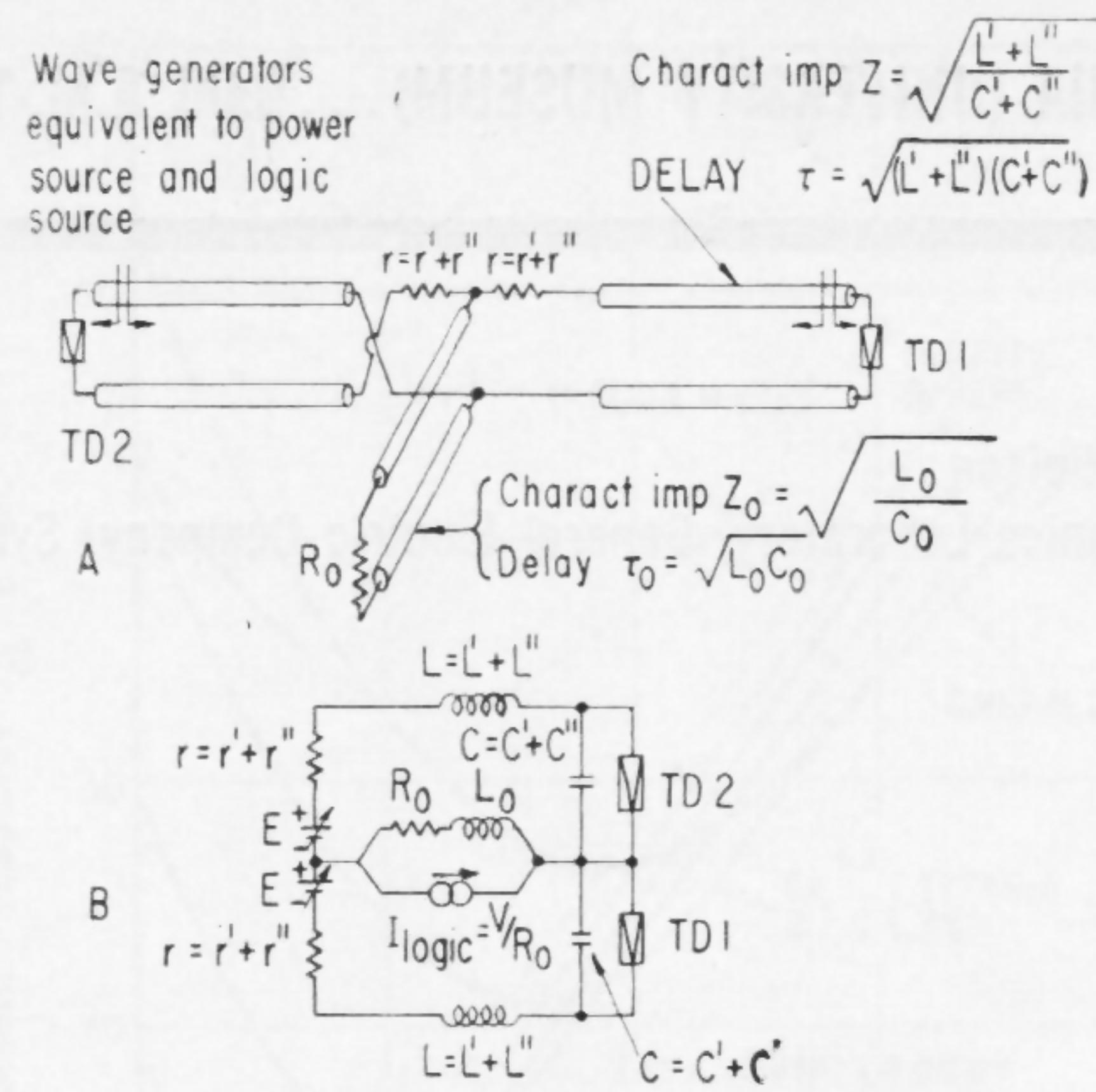


Figure 2—Two simplified balanced-pair circuits.

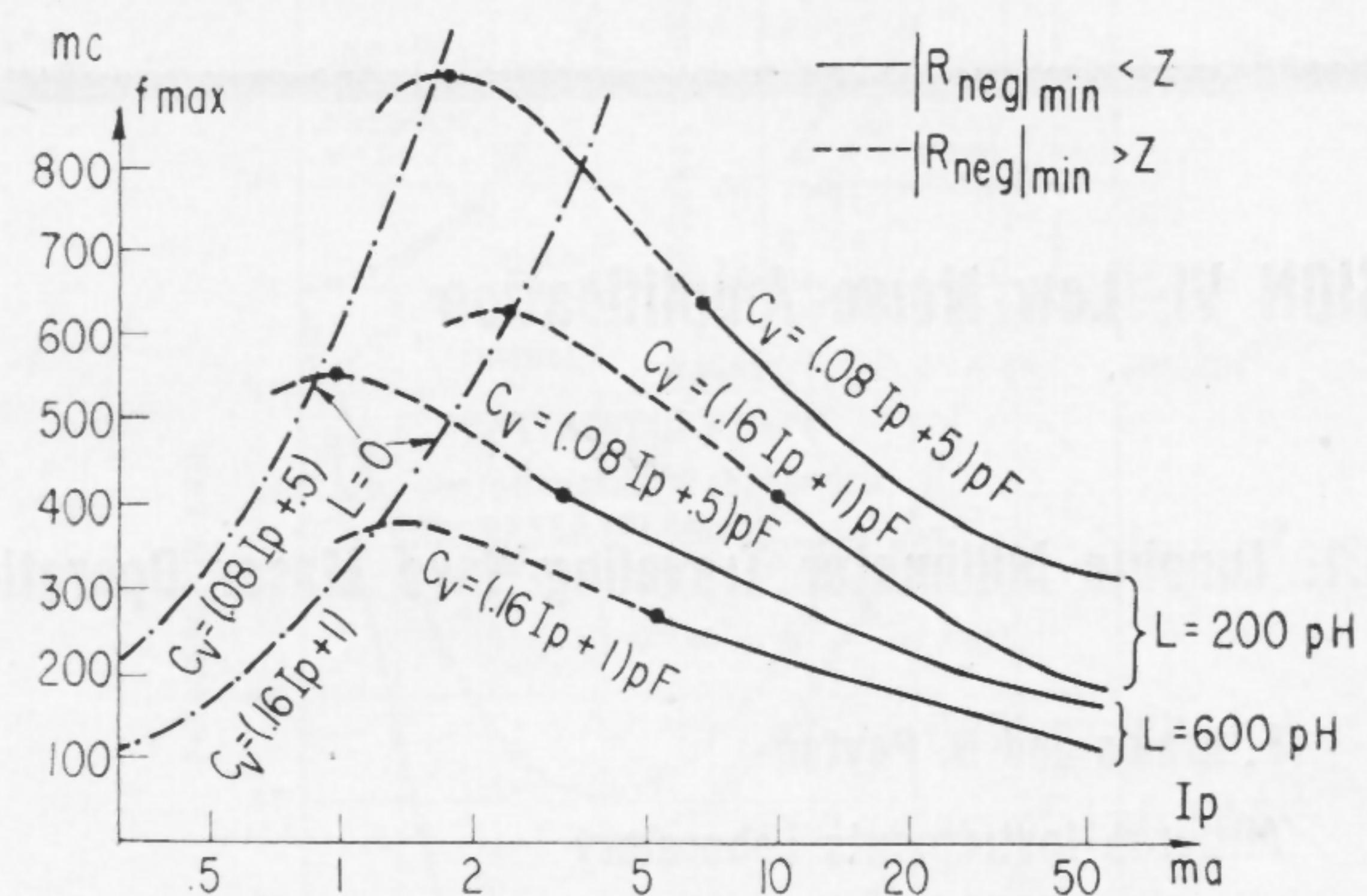


Figure 3—Maximum frequency for reliable locking with a sinusoidal ac source versus peak current.

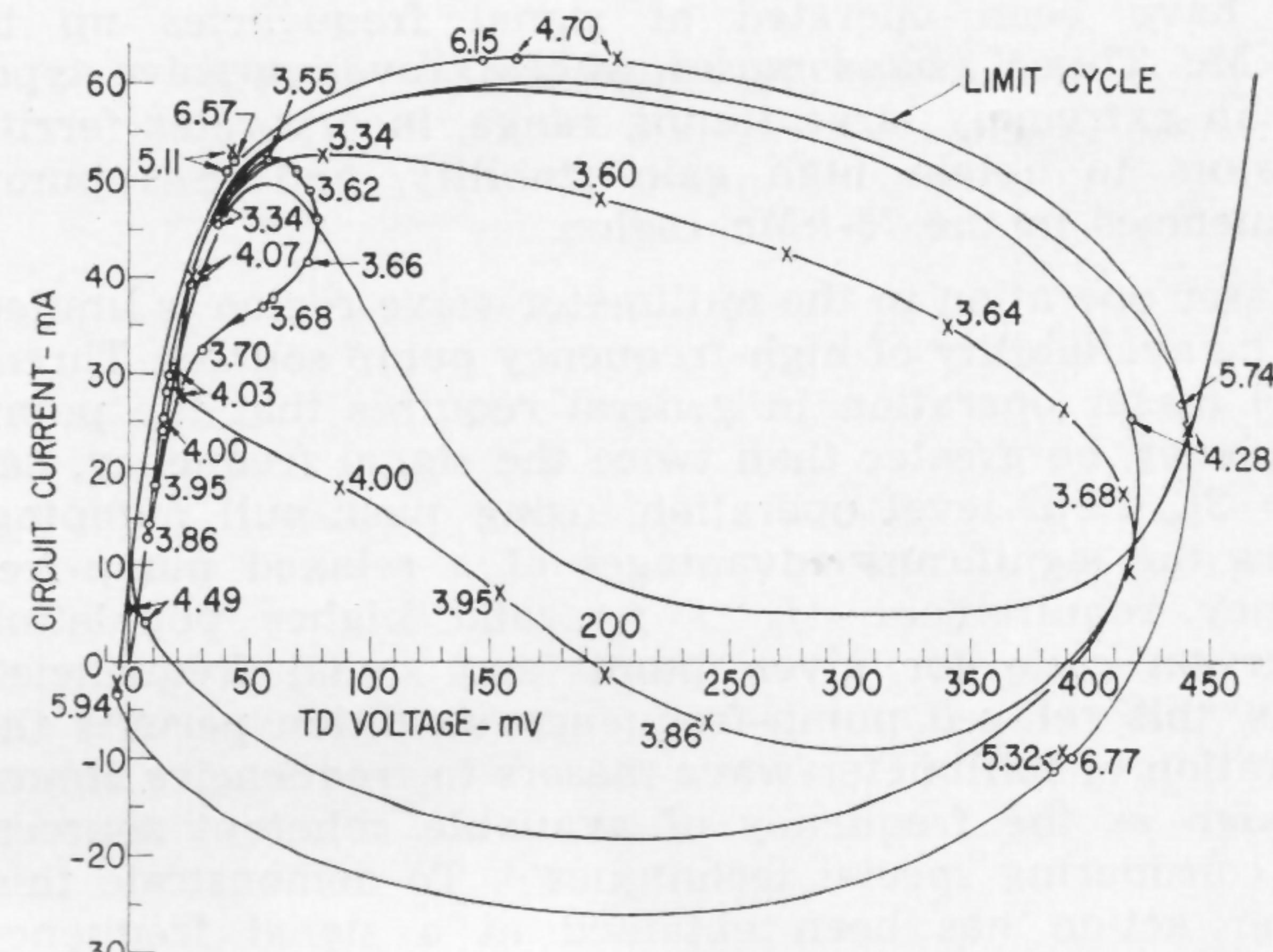
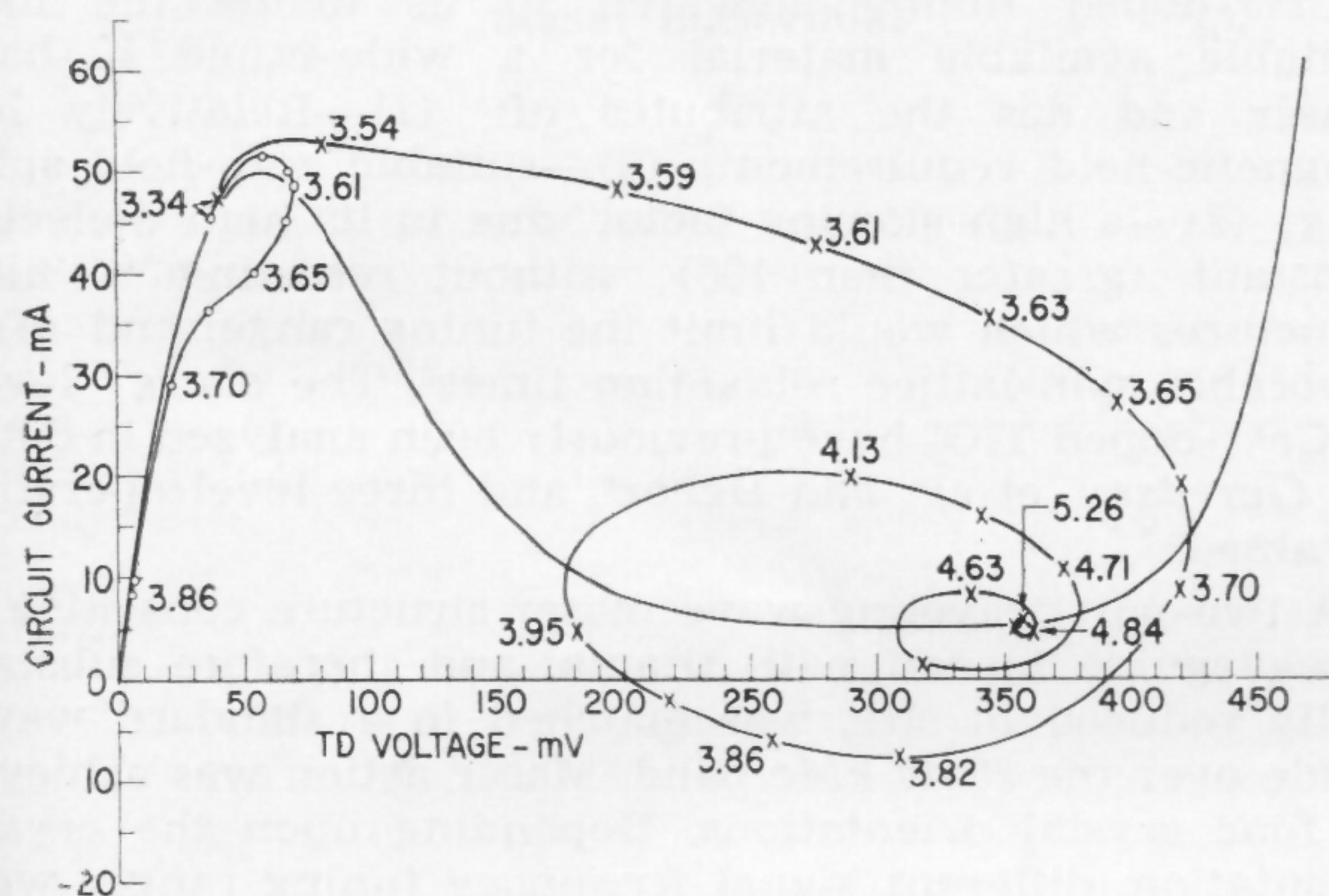


Figure 4—Circuit V-I trajectory of unstable balanced pair at 150 Mc. The trajectory in (a) at left shows plot of branch current against tunnel-diode voltage for upper and lower halves of Figure 2b circuit. Plot in (b) at right shows results of circuit loading causing oscillations.

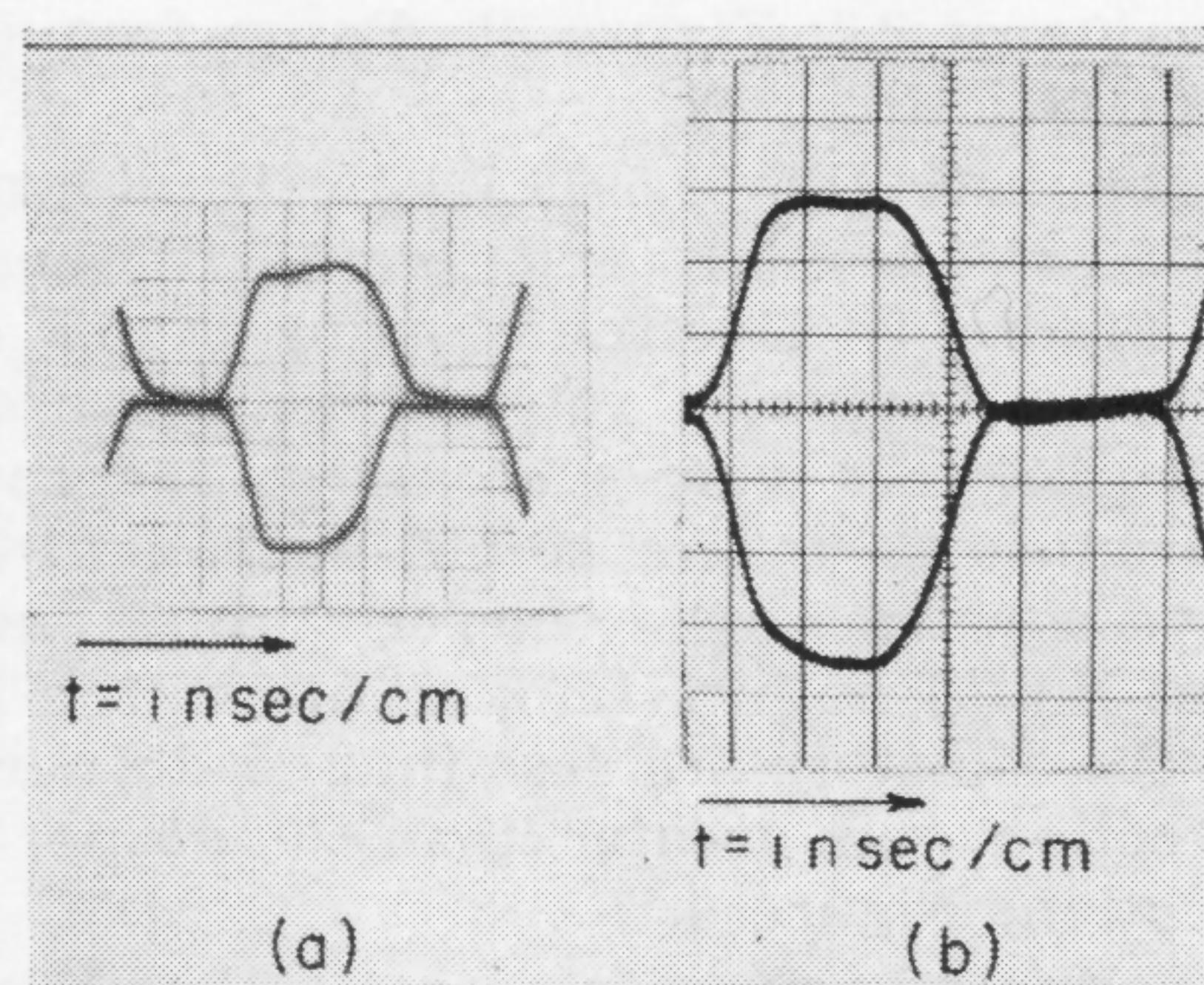


Figure 5—Waveforms of balanced-pair circuits: (a)—50-ma Ge circuit at 150 Mc; (b)—5-ma Ge circuit at 150 Mc.

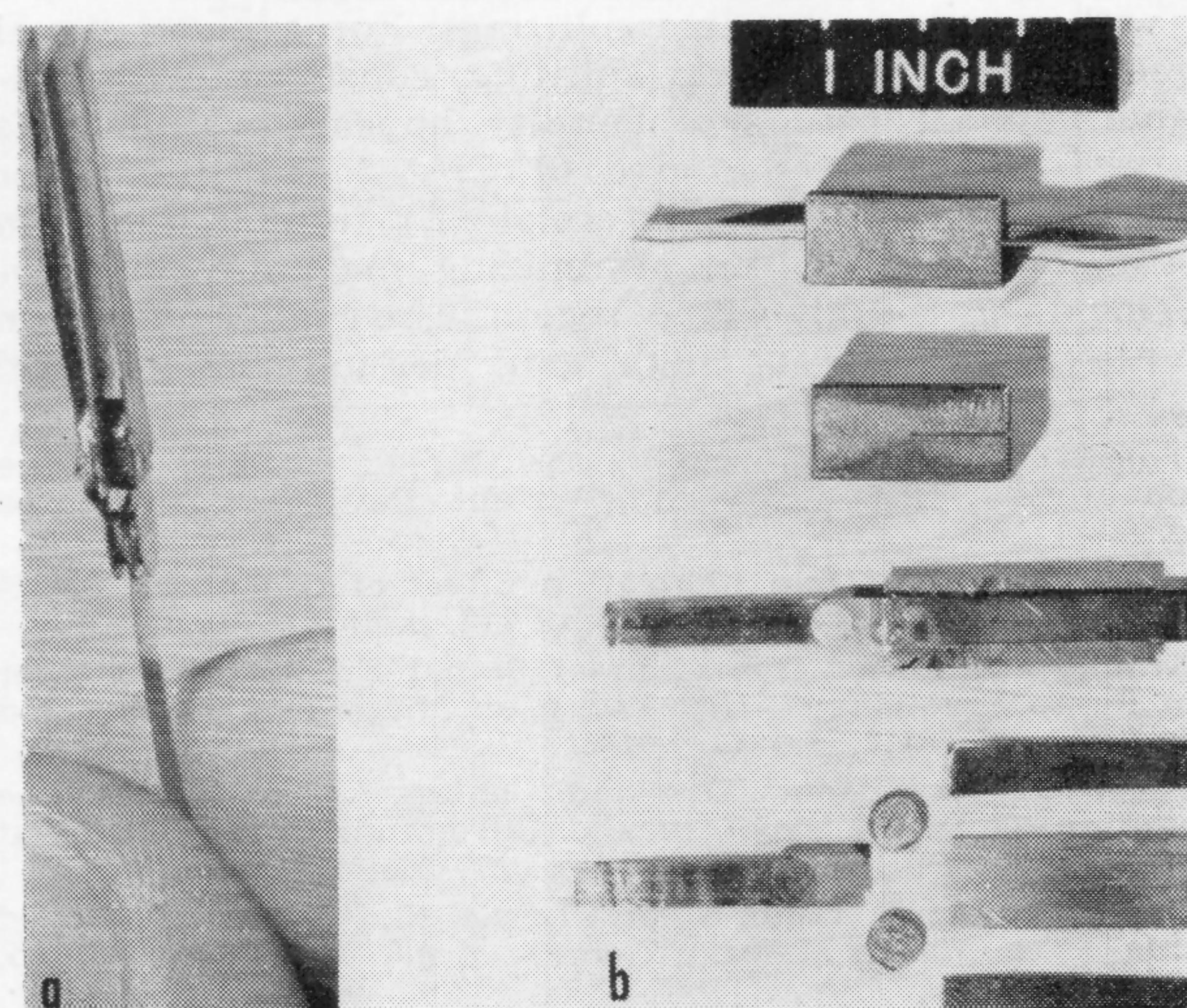


Figure 6—Packaging technique for balanced-pair circuits: (a)—Two tunnel-diode two-resistor assembly; (b)—steps for putting balanced-pair circuit in electro-formed copper shield can.

## SESSION VI: Low Noise Amplification

Chairman: E. G. Nielsen

Electronics Laboratory, General Electric Company, Syracuse, N. Y.

## TM 6.1: Tunable Millimeter Traveling-Wave Maser Operation\*

F. Arams and B. Peyton

Airborne Instruments Laboratory  
Deer Park, L. I., N. Y.

PROTOTYPE SECTIONS of a low-noise solid-state maser amplifier have been operated at signal frequencies up to 40 kMc. This  $K_a$  band maser, of the traveling-wave type, has an extremely large tuning range, incorporates ferrite isolators to obtain high gain stability, and uses pump frequencies in the 75-kMc region.

Maser operation in the millimeter-wave region is limited by the availability of high-frequency pump sources. Three-level maser operation in general requires that the pump frequency be greater than twice the signal frequency, i.e.,  $f_p > 2f_s$ . Four-level operation, using push-pull pumping, offers the significant advantages of a relaxed pump-frequency requirement ( $f_p > f_s$ ), and higher population inversion ratio for given pump and signal frequencies. Thus, this relaxed pump-frequency condition permits the operation of millimeter-wave masers to frequencies almost as high as the frequency of available coherent sources; not considering special techniques<sup>1,2</sup>. To demonstrate this, maser action has been obtained at a signal frequency of 40 kMc, using a pump frequency of only 43 kMc, and an applied magnetic field of 700 oersteds, with push-pull pumped chromium-doped titania as the active maser crystal at 4.2°K.

$Cr^{3+}$ -doped crystals have the advantage of symmetry in their energy levels at certain crystal orientations, permitting push-pull pumping over extended signal frequency ranges. Figure 1 shows signal frequency as a function of applied magnetic field for several  $Cr^{3+}$ -doped maser crystals with varying zero-field-splittings. For a given signal frequency, a low zero-field splitting, consistent with reasonable pump transition probability, appears desirable. As Figure 1 shows, in the case of  $Cr^{3+}$ -doped titania for  $\theta = 90^\circ$ , the presence of the axial ( $E$ ) term in the *Spin Hamiltonian* is useful in minimizing magnetic field requirements in the high-field region. The high-field region has the advantages of high gain per-unit length, and

\* This work was supported by the Bureau of Ships and the Aeronautical Systems Division, Wright Patterson Air Force Base.

<sup>1</sup> Minkowski, J., "Cross Relaxation Effect of Cr and Fe in  $K^3$  (Co, Cr, Fe) (CN)<sup>6</sup>", *Phys. Rev.*, vol 119, p. 1577; 1960.

<sup>2</sup> Arams, F., "Maser Operation at Signal Frequencies Higher Than Pump Frequency", *IRE Trans. on Microwave Theory and Techniques*, p. 68-72; January, 1961.

<sup>3</sup> Pace, J., Sampson, D., and Thorp, J., "Spin-Lattice Relaxation Times in Sapphire and Chromium-Doped Rutile at 34.6 Gc", *Proc. Phys. Soc.*, vol. 77, p. 257-260; 1961.

<sup>4</sup> Gerritsen, H., Harrison, S., and Lewis, H., "Chromium-Doped Titania as a Maser Material", *Jour. Appl. Phys.*, vol. 31, p. 1566-1571; 1960.

<sup>5</sup> Devor, D., "Fine Structure Levels and Transition Probabilities of  $Cr^{3+}$  in  $TiO_2$  (Rutile)", *Research Report 148*, Hughes Research Laboratories; May, 1960.

<sup>6</sup> Gerritsen, H., and Lewis, H., "Operation of a Chromium Doped Titania Maser", *Jour. Appl. Phys.*, vol. 31, p. 608; 1960.

<sup>7</sup> Sabisky, E., and Gerritsen, H., "Traveling-Wave Maser Using Chromium-Doped Rutile", *Proc. IRE*, vol. 49, p. 1329-1330; 1961.

convenient traveling-wave maser operation, since overlap with a ferrimagnetic isolator material is obtainable by adjusting the ferrite demagnetizing factors.

$Cr^{3+}$ -doped titania appeared to us to be the most suitable available material for a wide-range  $K_a$ -band maser and has the attributes of: (1)—Relatively low magnetic-field requirement; (2)—suitable zero-field splitting; (3)—a high slowing factor, due to its high dielectric constant (greater than 100), without resorting to filter structures which would limit the tuning range; and (4)—favorable spin-lattice relaxation times<sup>3</sup>. The energy levels of  $Cr^{3+}$ -doped  $TiO_2$  have previously been analyzed in detail by Gerritsen, et al<sup>4</sup>, and Devor<sup>5</sup>, and three-level operation obtained<sup>6,7</sup>.

A two-port traveling-wave maser structure consisting of a waveguide loaded with titania, and therefore substantially reduced in size, was matched to a standard waveguide over the 26-40 kMc band. Maser action was achieved at four crystal orientations. Depending upon the crystal orientation, different signal frequency tuning ranges were obtained. The experimental data of paramagnetic absorption and maser action is summarized in Figure 2.

Maser action was obtained in the low-magnetic-field region over the entire band from 25-40 kMc with pump frequencies from 43-47.3 kMc and magnetic fields from .7 to 5.2 kiloersteds; Figure 2. The magnetic field was oriented at  $\theta = 45.7^\circ$  in the ac plane of the maser crystal, where the low magnetic complexes of  $Cr^{3+}$  in  $TiO_2$  are aligned, thereby doubling the electronic gain.

Population inversion was also obtained using the above crystal orientation at high magnetic fields where higher gains, due to the higher pump frequency, are available. As shown in Figure 3a, electronic gains averaging 4.4 db-per-cm from 23-27 kMc were obtained at 4.2°K. The electronic gain increased to 10.5 db-per-cm at 1.7°K. The measured population inversion correlated well with the calculated value of 2.2; Figure 3b. Pump frequencies used were from 64-73 kMc.

Maser action over the 33.5-39.5 kMc band was obtained using a  $\theta = 80^\circ$  crystal, and pump frequencies from 62-78 kMc; Figure 2. Electronic gains of 6.5 db-per-cm, and a population inversion ratio of 1.5, were obtained at 1.7°K. Ferrite isolators were successfully incorporated into the twm structure to insure stable operation. The ferrite tuning curve overlaps the maser tuning curve from 33-41 kMc at liquid helium temperatures. The losses contributed by the isolators are less than .5 db-per-cm in the forward direction and greater than 30 db-per-cm in the reverse direction; Figure 4.

Stable traveling-wave maser operation has been obtained over very large tuning ranges in the  $K_a$ -band using  $Cr^{3+}$ -doped titania as the active material. The tuning range can be varied by suitably selecting the crystal orientation and the techniques employed are believed to be also applicable to much higher frequencies. Further work is in progress.

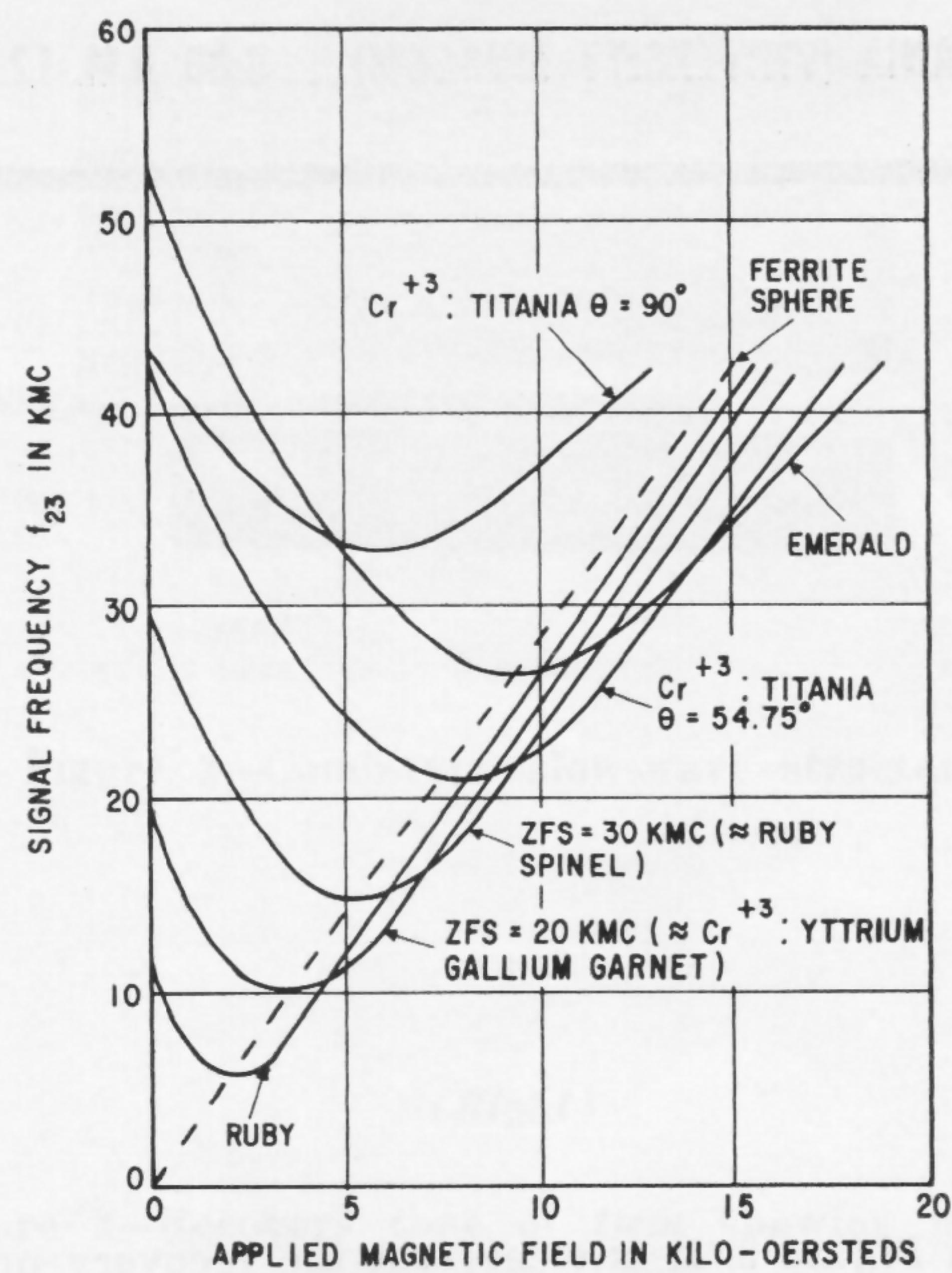


Figure 1—Comparison of various push-pull-pumped maser materials.

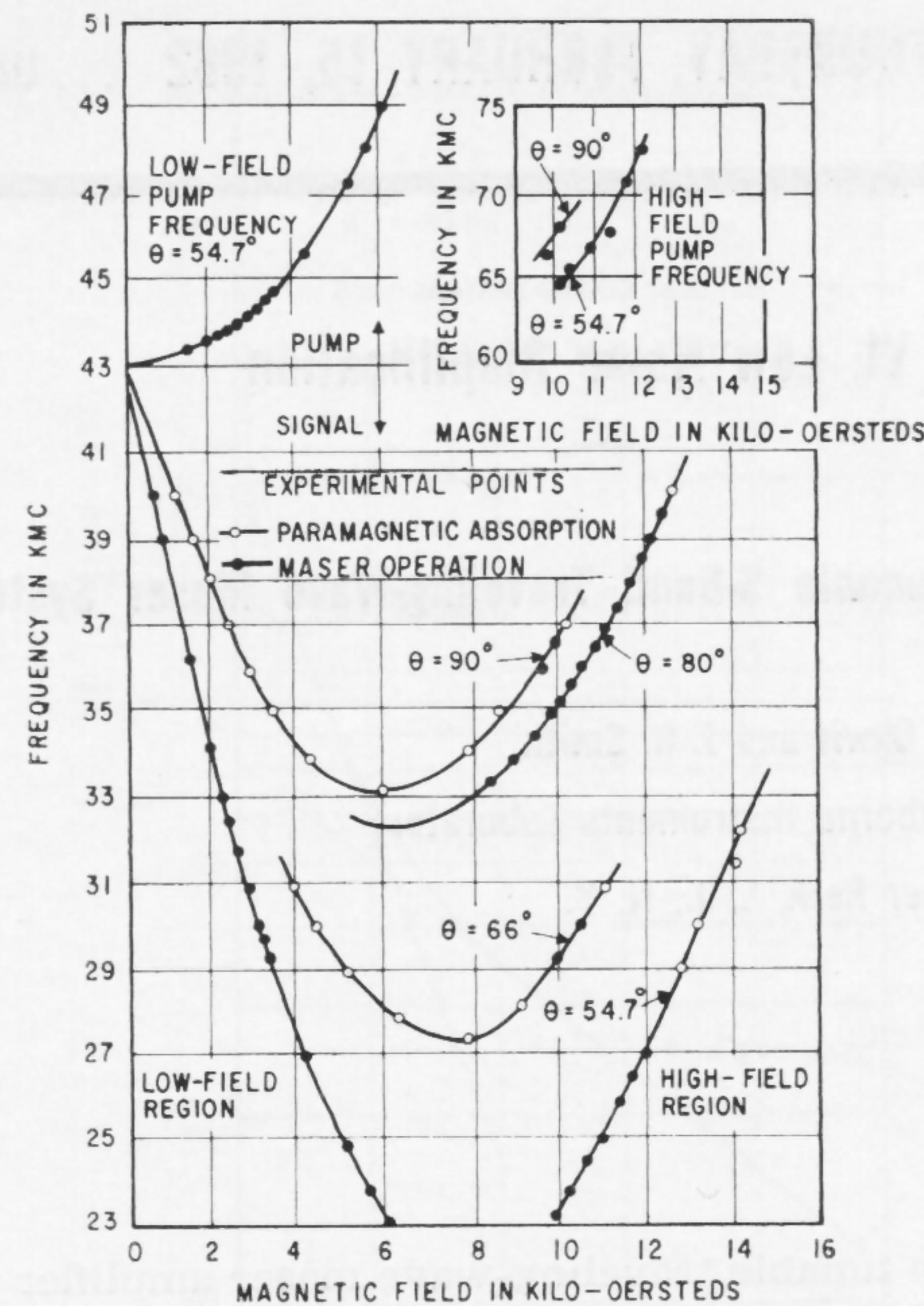


Figure 2—Experimental operating points.

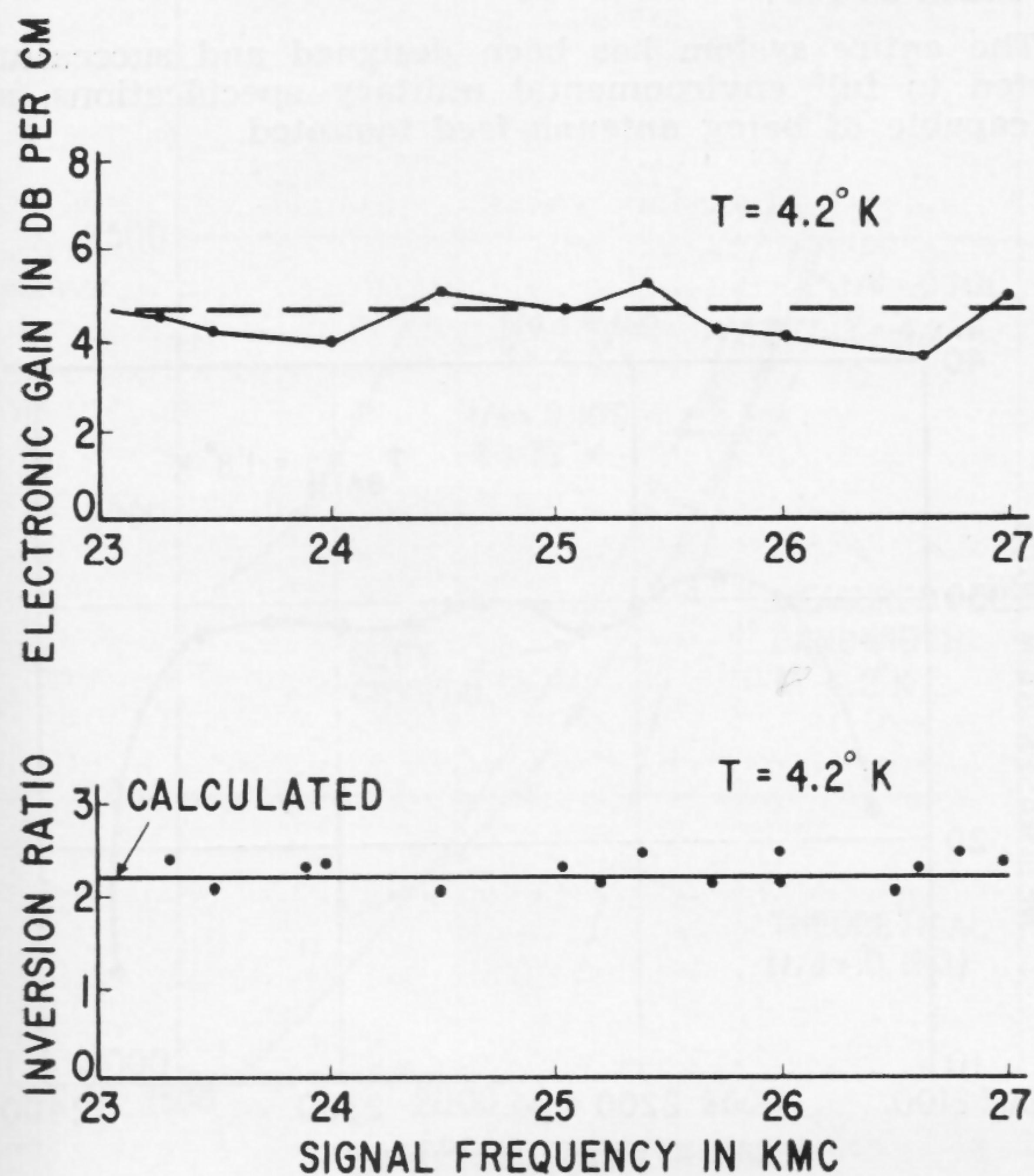


Figure 3—Electronic gain and population inversion ratio versus signal frequency.

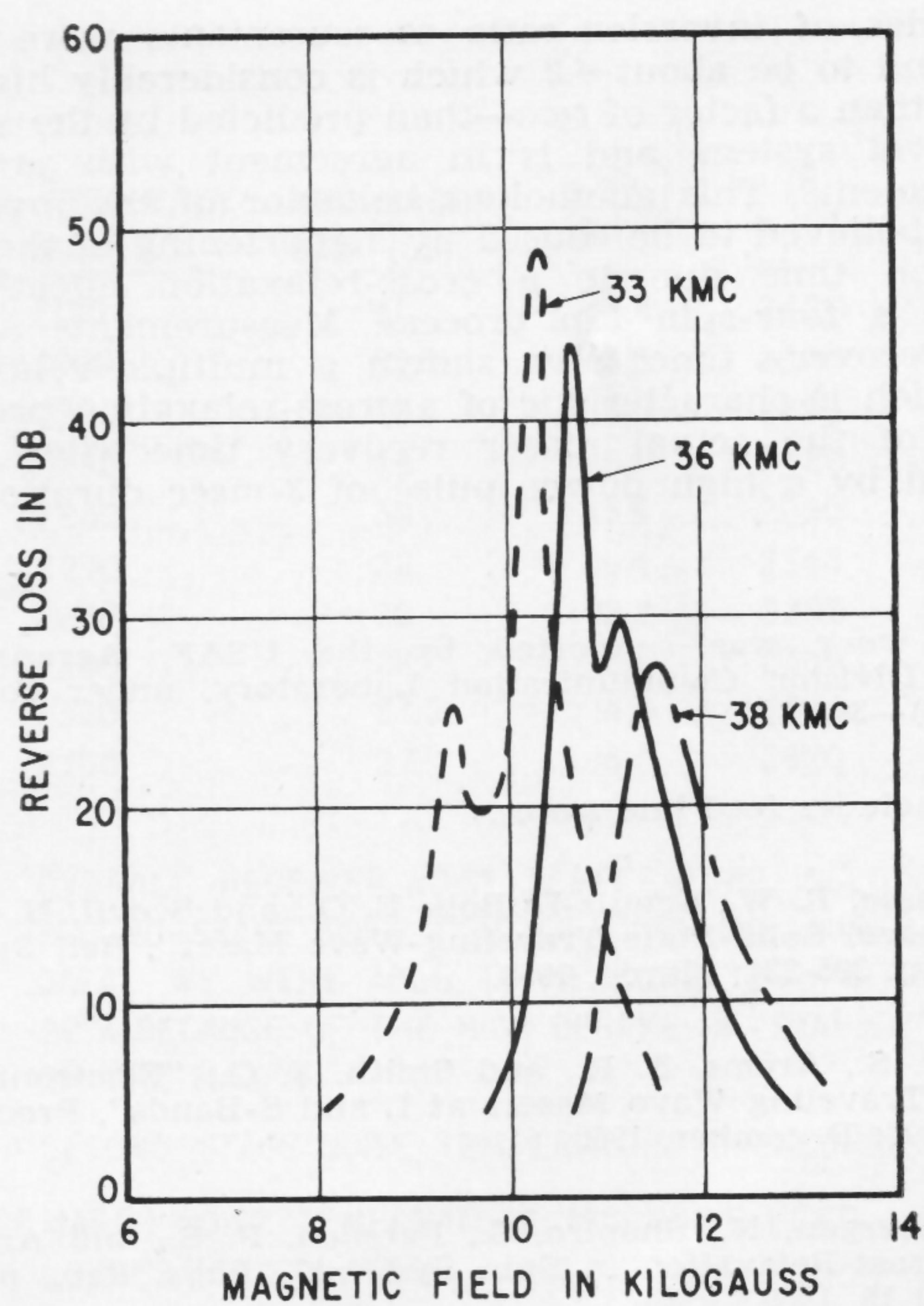


Figure 4—Reverse isolator loss versus applied magnetic field at room temperature.

## SESSION VI: Low Noise Amplification

### TM 6.2: Tunable S-Band Traveling-Wave Maser System\*

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Deer Park, L. I., N. Y.

A PACKAGED tunable traveling-wave maser amplifier system, operating at a bath temperature of  $1.8^{\circ}\text{K}$ , has been designed and developed for telemetry applications. The unit is electronically tunable from 2126 to 2380 Mc by means of a single frequency-calibrated dial. The maser yields nearly constant net gains of 30 db across the tuning range with instantaneous bandwidths of 22 Mc; Figure 1.

The traveling-wave maser (*twm*), utilizes a comb-type slow-wave structure<sup>1</sup> that is loaded on both sides with  $6\frac{1}{2}''$  of *x-ray* oriented ruby; Figure 2. The ruby is located in the structure with its *C-axis* aligned perpendicular to the external magnetic field and parallel to the direction of propagation<sup>2</sup>. The combination of double-sided loading and parallel *C-axis* orientation yields close to the maximum available gain per unit length. This is a result of:

- (1)—Increased filling factor afforded by double-sided loading.
- (2)—Increased magnetic susceptibilities afforded by the parallel *C-axis* alignment.

Measurements have shown that this combination improved the gain per-unit-length by as much as a factor two (twice the db), relative to the conventional single-sided,  $60^{\circ}$  *C-axis* loading;  $60^{\circ}$  relative to the direction of propagation.

A series of inversion-ratio measurements were made and found to be about 4.2 which is considerably higher—greater than a factor of two—than predicted by the simple three-level system, and is in agreement with previous measurements. This anomalous behavior of the inversion ratio is believed to be caused by a shortening of the idler relaxation time due to a cross-relaxation effect<sup>3</sup> that involves a four-spin flip process. Measurements on the maser recovery time have shown a multiple relaxation rate which is characteristic of a cross-relaxation process<sup>4</sup>. A plot of the actual maser recovery time after being saturated by a high power pulse of 3-msec duration ap-

pears in Figure 3. It is clear that the recovery process is described by three relaxation rates, two of which are easily determined to be 90 and 270 msec. The third relaxation time is estimated to be about 5 msec. The time required for the maser to recover to within 3 db of its full 30-db gain is about 50 msec.

Several gain stability measurements were taken on an overall maser if system, and yielded long term peak-to-peak drift of  $\pm .1$  db and short term peak-to-peak stability of  $\pm .05$  db; Figure 4. This high stability was a result of the high degree of isolation (greater than 100 db) afforded by ferrimagnetic disks of YIG that were distributed in the slow-wave structure. The YIG disk dimensions were adjusted so that the external magnetic fields required for ferrimagnetic resonance would be coincident with the fields required for maser operation; Figure 5.

Measurements of the effective maser noise temperature,  $T_m$  \*, using a hot and cold load noise generator in a Y-factor measurement, yielded  $T_m$  as low as  $9.2^{\circ}\text{K}$ . A detailed table of noise measurements taken across the tuning band is shown in Figure 6.

The overall maser system consists of three units: (1)—The *twm* assembly; (2)—remote control power supply; and (3)—vacuum pump. These units can be separated by as much as 100'.

The entire system has been designed and successfully tested to full environmental military specifications, and is capable of being antenna-feed mounted.

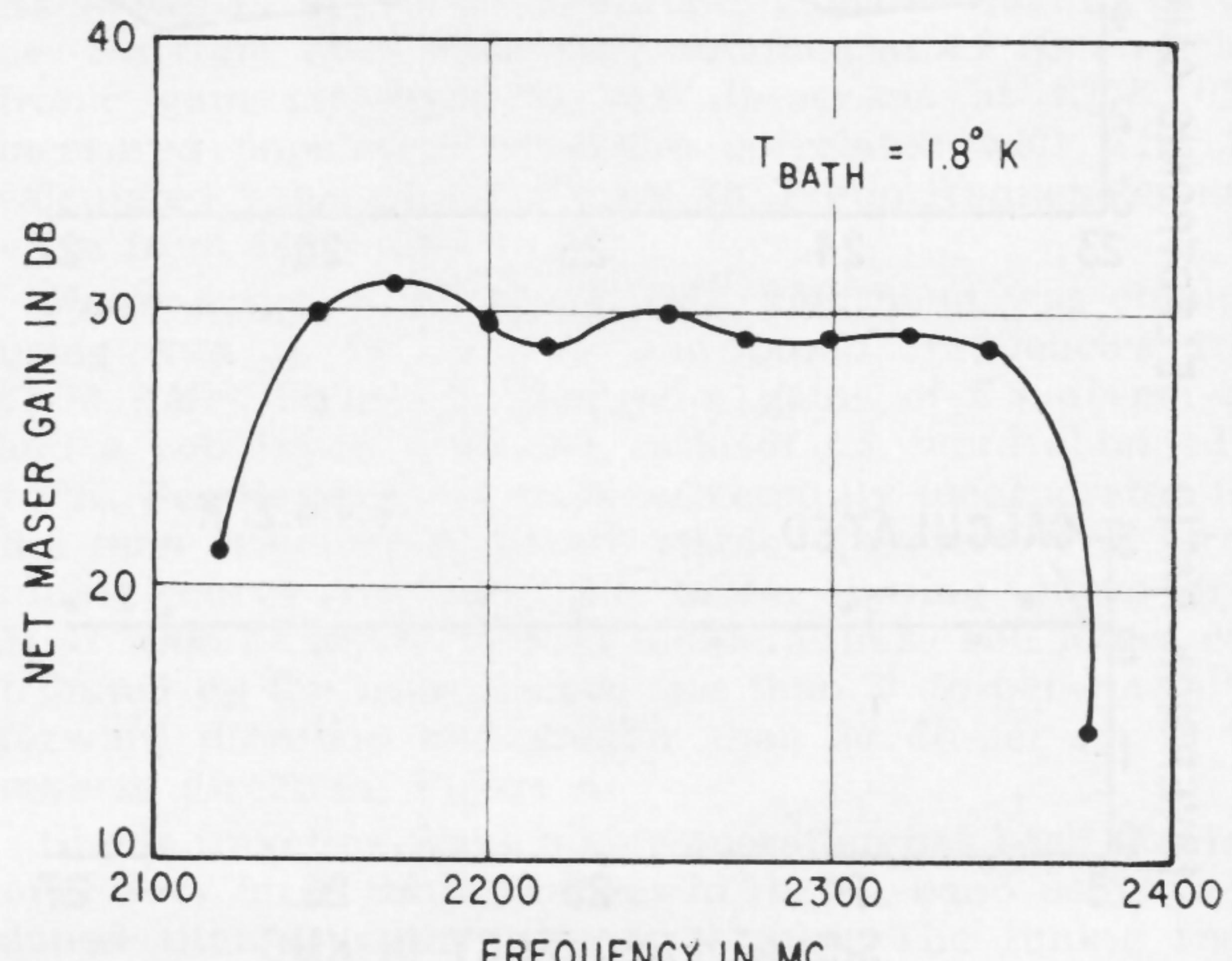


Figure 1—Net maser gain as a function of tuning frequency.

\* This work was supported by the USAF, Aeronautical Systems Division Communication Laboratory, under contract AF33(600)—38862.

\*  $T_m$  includes feed line losses.

<sup>1</sup> DeGrasse, R. W., Schulz-DuBois, E. O., and Scovil, H. E. D., "Three-Level Solid-State Traveling-Wave Maser", *Bell Systems Tech. J.*, p. 305-334; March, 1959.

<sup>2</sup> Okwit, S., Arams, F. R., and Smith, J. G., "Electronically-Tunable Traveling Wave Masers at L and S-Bands", *Proc. IRE*, p. 2205-2206; December, 1960.

<sup>3</sup> Bloembergen, N., Shapiro, S., Pershan, P. S., and Artman, J. O., "Cross-Relaxation in Spin Systems", *Phys. Rev.*, p. 445-457; April 15, 1959.

<sup>4</sup> Chang, W. S. C., "Spin Lattice Relaxation via Harmonic Coupling", in "Quantum Electronics", Columbia University Press, p. 346; 1960.

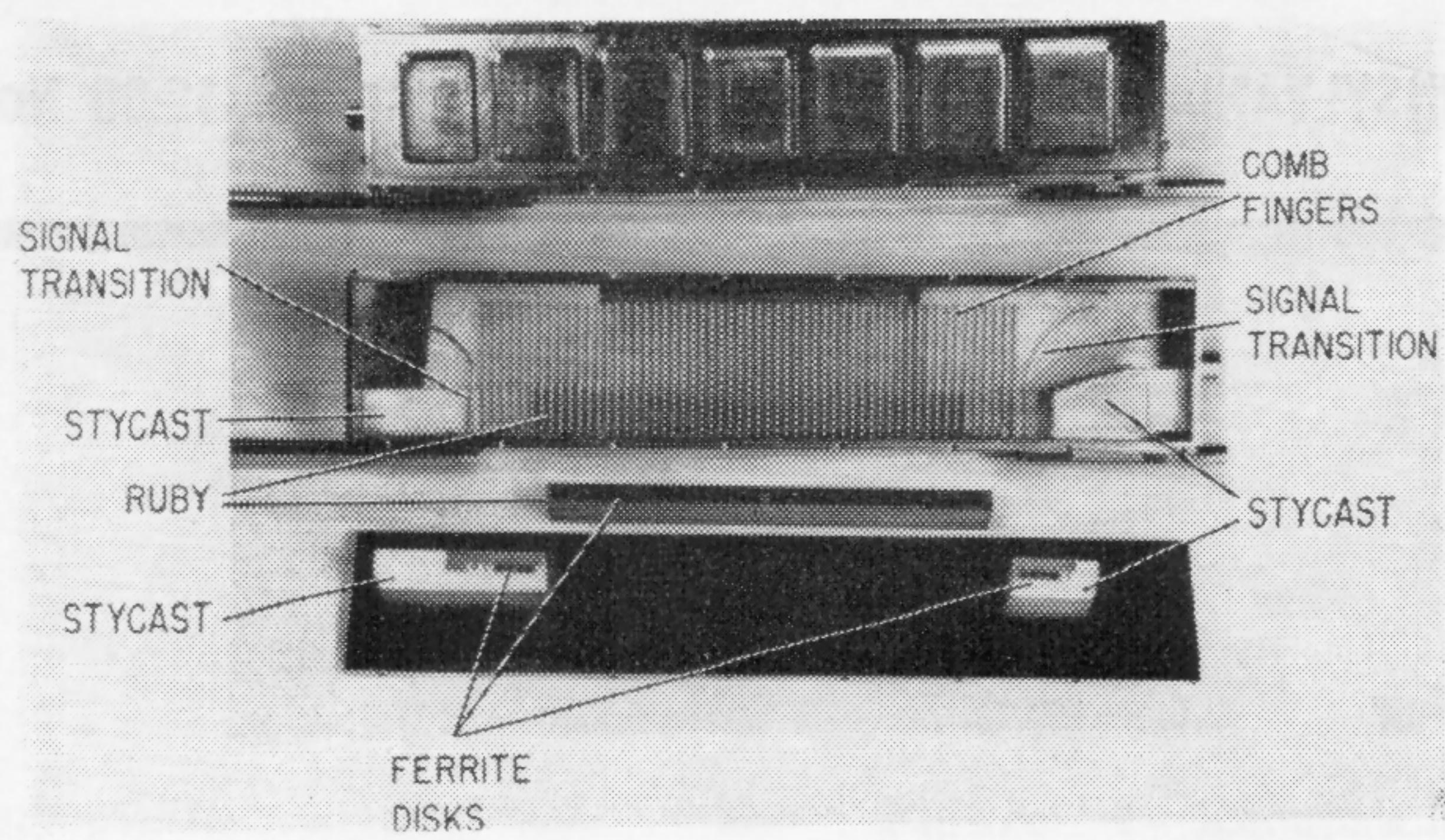


Figure 2—Comb-type slow-wave structure.

(Right)

Figure 3—Recovery time of *twm* showing multiple relaxation times.

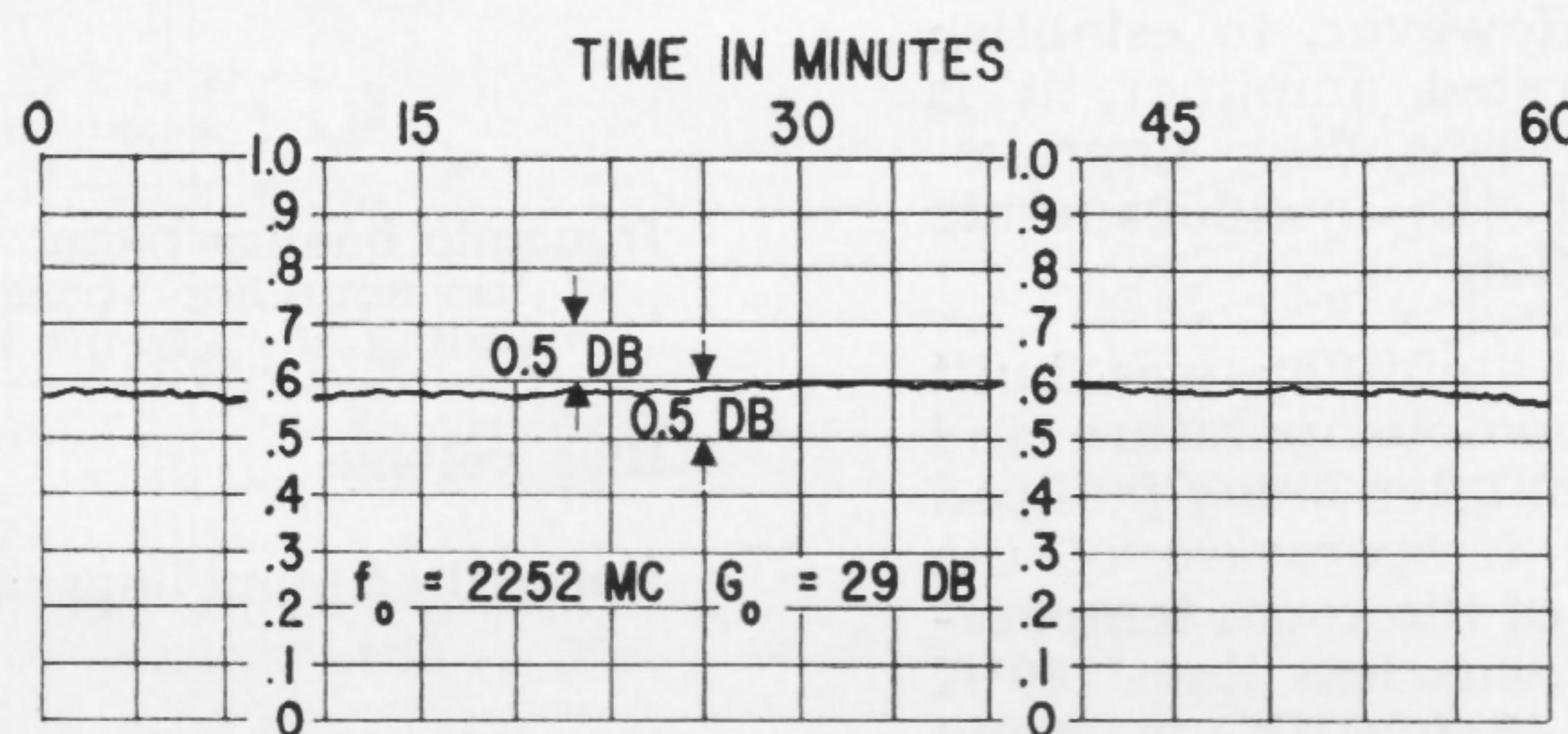
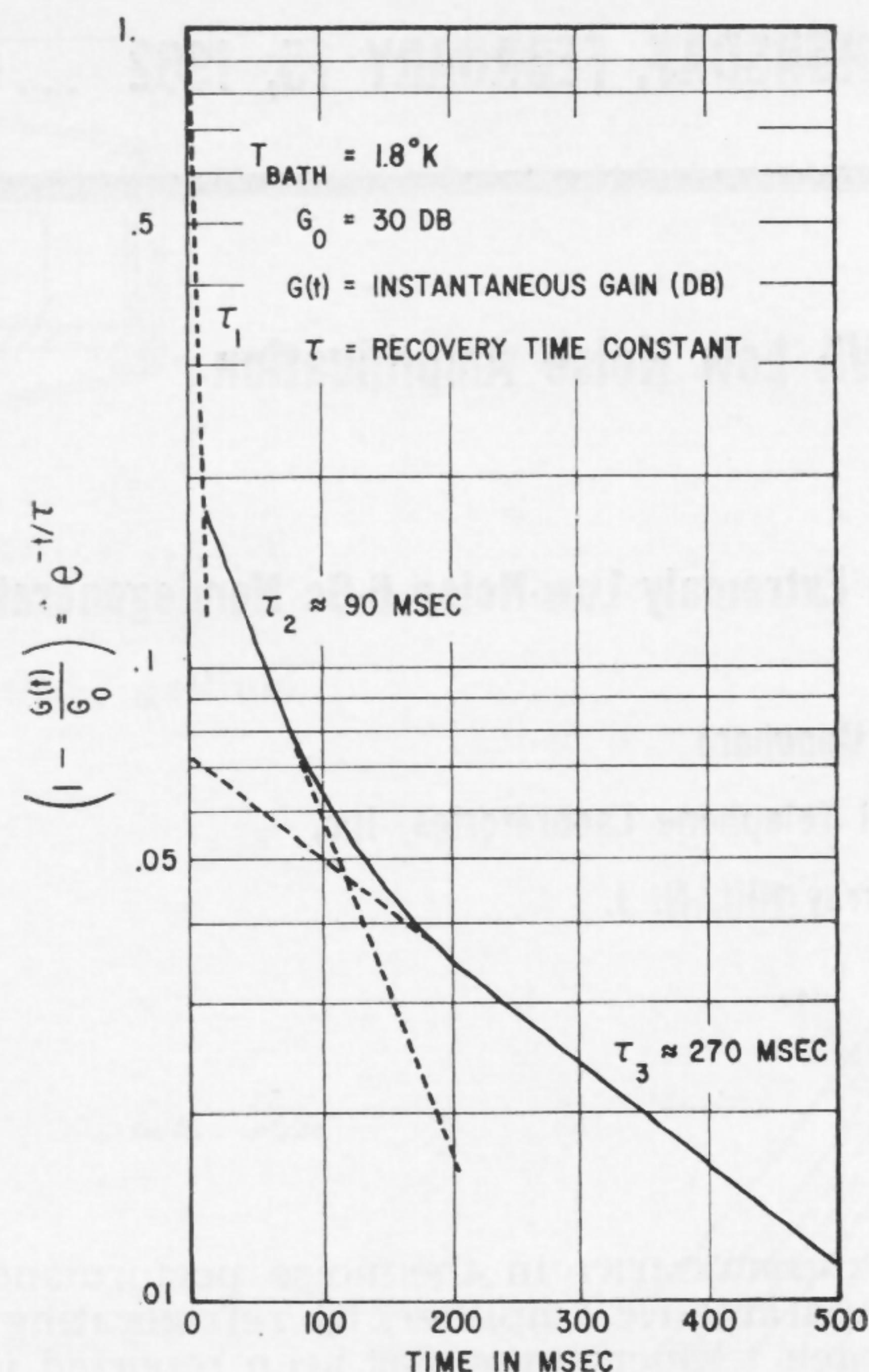


Figure 4—Recorder display of gain stability for a *twm* receiving system.

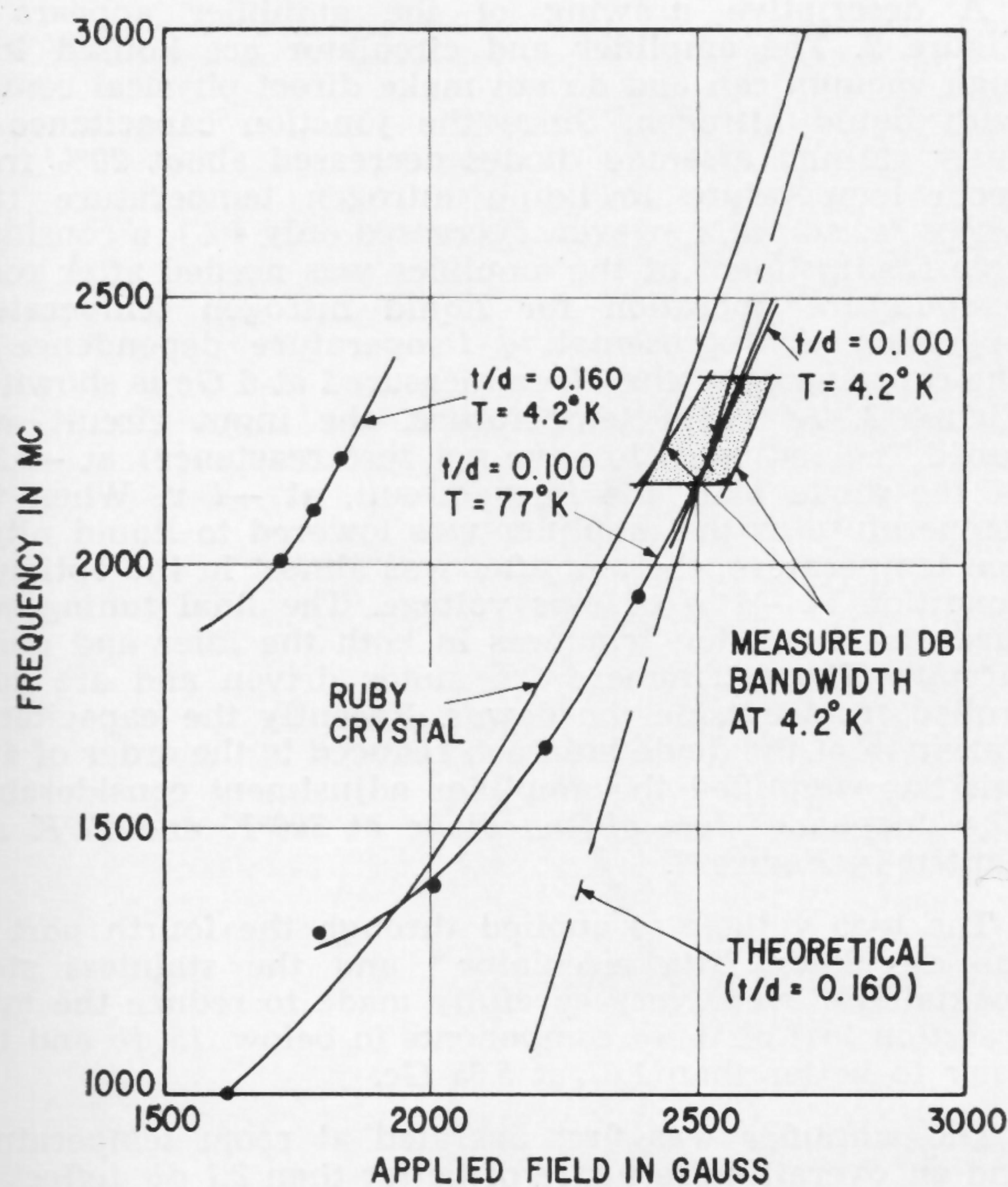


Figure 5—Resonant frequency versus applied magnetic field for ruby crystal and YIG ferrite disks.

SIGNAL FREQUENCY (MC)	NET MASER GAIN (DB)	T <sub>e</sub> (°K)	T <sub>2</sub> (°K)	T <sub>m</sub> (°K)
2170	31	12.4	2420	10.5
2200	29.5	13.5	2345	10.9
2220	28	15.8	2290	12.2
2230	29	15.1	2420	12.0
2250	30	15.5	2050	13.4
2270	28	15.4	2345	11.7
2280	28	12.8	2295	9.2
2300	28	13.6	2350	9.9
2330	27.5	14.3	2350	10.1
2350	27	15.1	2520	10.1

T<sub>e</sub> = OVERALL RECEIVER NOISE TEMPERATURE INCLUDING SECOND-STAGE NOISE CONTRIBUTIONS (MEASURED DATA). WE WERE ABLE TO MEASURE T<sub>e</sub> TO WITHIN  $\pm 2^{\circ}\text{K}$  BECAUSE OF THE HIGH DEGREE OF STABILITY OF THE MASER.

T<sub>2</sub> = SECOND-STAGE NOISE TEMPERATURE (MEASURED DATA).

T<sub>m</sub> = MASER NOISE TEMPERATURE INCLUDING FEED-LINE LOSSES (CALCULATED).

Figure 6—Results of receiver noise temperature measurements.

## SESSION VI: Low Noise Amplification

## TM 6.3: An Extremely Low-Noise 6-Gc Nondegenerate Parametric Amplifier

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Murray Hill, N. J.

A MARKED IMPROVEMENT in the noise performance of the degenerate parametric amplifier, by refrigerating down to liquid nitrogen temperatures, has been reported in several publications<sup>1,2,3,4,5</sup>. This improvement in the noise performance is of great significance for the parametric amplifier, particularly at microwave frequencies where a high quality diode is difficult to obtain. However, to establish the true potentiality of the refrigerated amplifier, it is necessary to demonstrate also a corresponding improvement in the noise performance of the nondegenerate parametric amplifier with refrigeration.

A 6-Gc nondegenerate parametric amplifier was built and operated successfully both at room temperature and at liquid nitrogen temperature, the amplifier being pumped at 23 Gc. The effective input noise temperature of the amplifier, including the insertion loss of the room temperature circulator and the mixer noise, was less than 180°K at room temperature, and was less than 60°K at liquid nitrogen temperature; of this more than 20°K is attributed to the circulator and the mixer.

The varactor diodes used for this experiment were gallium arsenide point-contact diodes, both unsealed<sup>6</sup> and sealed types. The encapsulation of the sealed diode, developed by N. C. Vanderwal<sup>†</sup> is shown in Figure 1. The dynamic quality factor  $\tilde{Q}$  at 6 Gc for average types of these diodes lies in the 6 to 8 range; therefore, the optimum pump frequency for such diodes lies somewhere in the K band<sup>7</sup>, the precise value depending also on the amount of external idler loading; from practical considerations, 23 Gc was chosen for this amplifier. The main features of the amplifier are:

<sup>†</sup> Bell Telephone Labs., Allentown, Pa.

\* Raytheon circulator CCL-4 (room temperature model) and CCL-5 (liquid nitrogen model).

<sup>1</sup> Uenohara, M., and Bakanowski, A. E., "Low Noise Parametric Amplifier Using Germanium P-N Junction Diode at 6 KMC," *Proc. IRE*, p. 2113; December, 1959.

<sup>2</sup> Uenohara, M., and Sharpless, W. M., "An Extremely Low-Noise 6-KMC Parametric Amplifier Using Gallium Arsenide Point Contact Diodes," *Proc. IRE*, p. 2114; December, 1959.

<sup>3</sup> Forster, J. H., and Uenohara, M., "Diffused Silicon Mesa Diodes for Use in Refrigerated Parametric Amplifiers," *Third Interim Rept. Microwave Solid-State Devices*, Contract DA36-039 SC-85325; to be published in *Proc. IRE*.

<sup>4</sup> Knechtli, R. C., and Weglein, R. D., "Low Noise Parametric Amplifier," *Proc. IRE*, p. 584-585; April, 1959.

<sup>5</sup> Stelzried, C. T., "A Cooled, Negative Conductance, Degen- erate Parametric Amplifier," *Microwave Journal*, p. 79-84; July, 1961.

<sup>6</sup> Sharpless, W. M., "Gallium-Arsenide Point-Contact Diodes," *IRE Trans. on MTT*, p. 6-10; January, 1961.

<sup>7</sup> Uenohara, M., and Seidel, H., "961-Mc Lower-Sideband Up- Converter for Satellite-Tracking Radar," *BSTJ*, p. 1183-1205; July, 1961.

Input and output frequency	5.85 Gc
Pump frequency and power	23 Gc, 5 mw
Varactor diode	Gallium arsenide point-contact diode $C_o = .42 \text{ pf}$ at 300°K, includes about .07 pf of package capacitance
Dynamic quality factor $\tilde{Q}$ of the amplifier at 5.85 Gc, including the circuit loss	7 at 300°K, and about 15 to 20% higher at 77°K
Bias voltage	-1 v
Normalized input impedance $R_s/R_o$	1/8.5 at 300°K and 1/10.5 at 77°K
Normalized idler impedance $R_s/R_L$	1
Gain	20 db
Estimated noise temperature; amplifier alone	150°K at 300°K and 38°K at 77°K

A descriptive drawing of the amplifier appears in Figure 2. The amplifier and circulator are housed in a high vacuum can and do not make direct physical contact with liquid nitrogen. Since the junction capacitance of early gallium arsenide diodes decreased about 20% from room temperature to liquid nitrogen temperature (the series resistance, however, decreased only 4%), a considerable readjustment of the amplifier was needed after room temperature operation for liquid nitrogen temperature operation. A representative temperature dependence of the capacitance of the diode measured at 6 Gc is shown in Figure 3. At room temperature, the input circuit was tuned (i.e., adjusted to have net zero reactance) at -2.3 v of the diode bias; the idler circuit, at -4 v. When the temperature of the amplifier was lowered to liquid nitrogen temperature, the amplifier was almost in the optimum condition at -1 v of bias voltage. The final tuning was made by the teflon trimmers in both the idler and pump circuits. These trimmers are motor driven and are controlled from outside the dewar. Recently the capacitance variation of the diode has been reduced to the order of 4%; this has simplified the amplifier adjustment considerably. The impedance loci of the diode at 300°K and 77°K are plotted in Figure 4.

The bias voltage is applied through the fourth port of the circulator. The circulator\* and the stainless steel coaxial line were very carefully made to reduce the total insertion loss of these components to below .15 db and the vswr to better than 1.07 at 5.85 Gc.

The amplifier was first operated at room temperature and an overall noise figure of better than 2.1 db (effective input noise temperature of 180°K) was measured with 20 db of gain and 30-Mc bandwidth. Since the insertion loss of the input circuit was about .15 db and the single

[Continued on page 106]

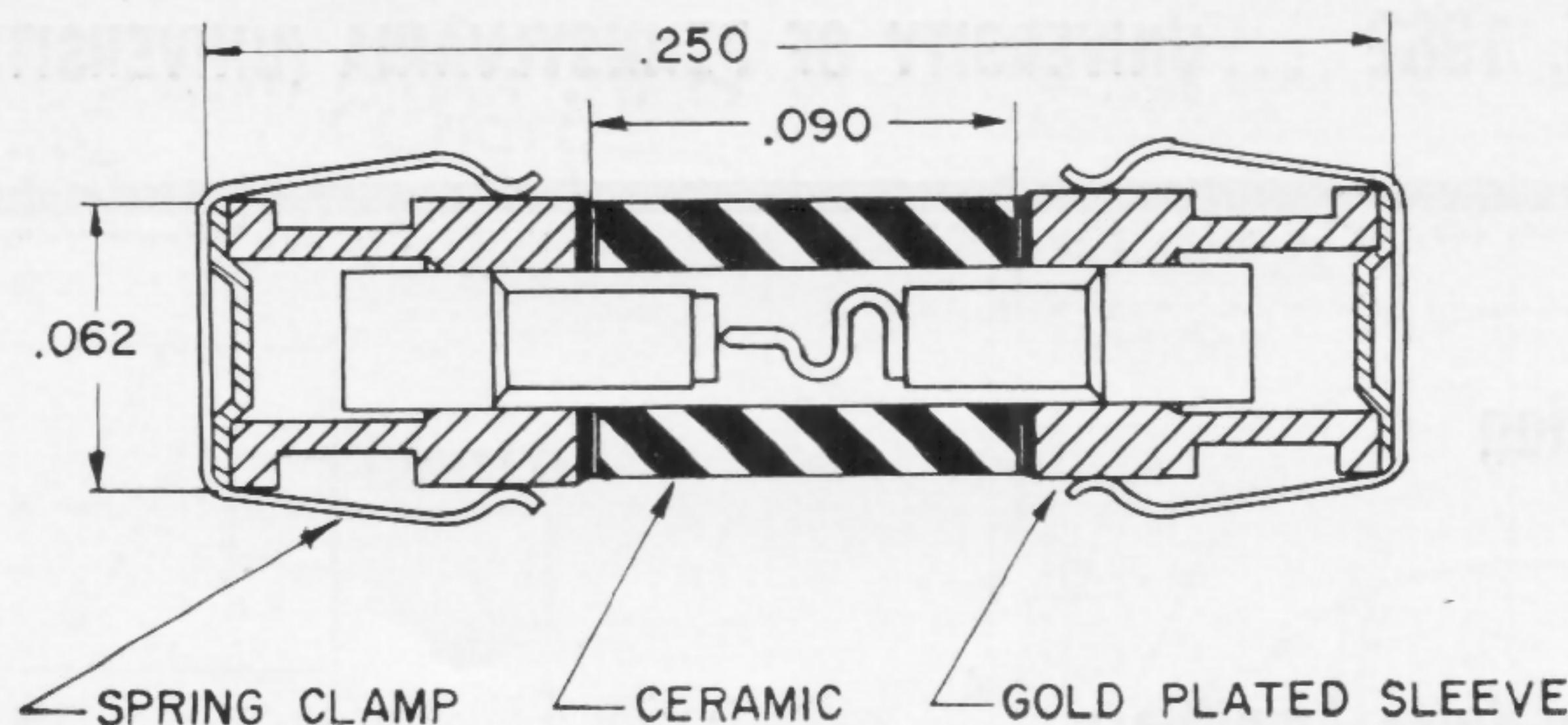


Figure 1—Encapsulation of the sealed gallium arsenide diode.

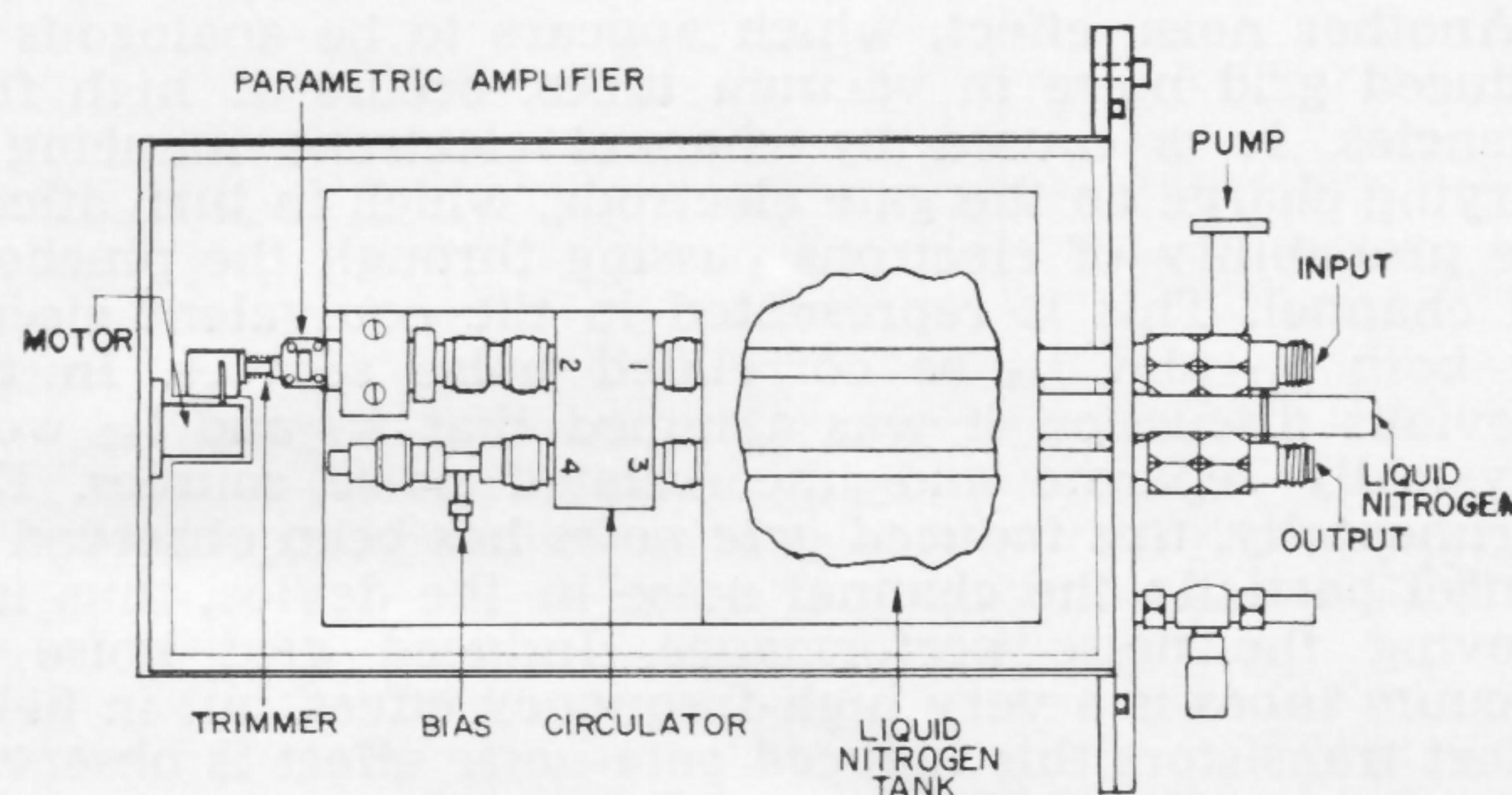


Figure 2—Refrigerated 6-Gc one-port parametric amplifier. Liquid nitrogen is stored in two tanks to which the amplifier and the circulator are fastened. The amplifier does not make physical contact with liquid nitrogen.

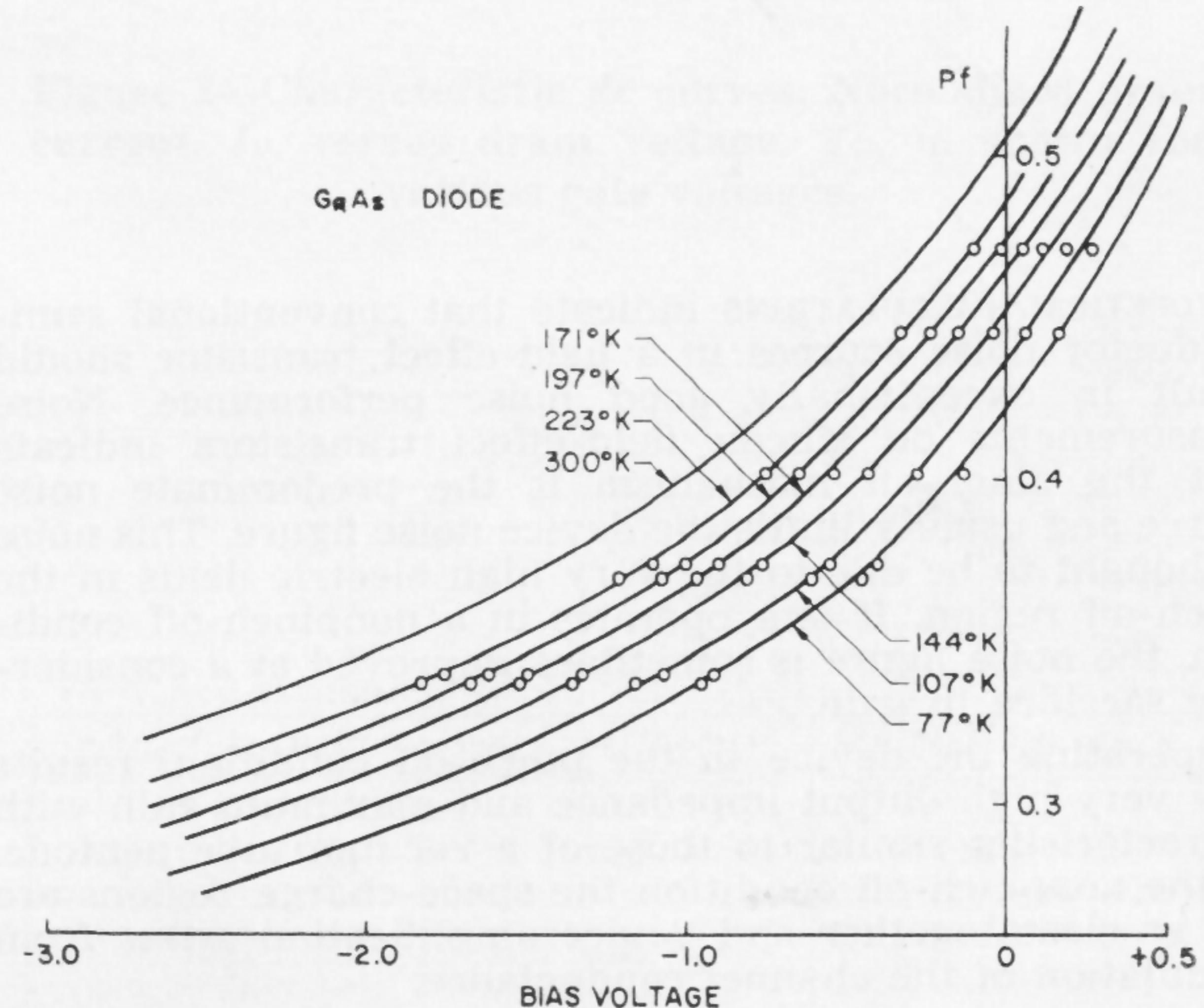


Figure 3—Representative temperature dependence of the capacitance of the gallium arsenide diode (including about .07 pf of package capacitance). Junction capacitance decreased about 20% from 300°K to 77°K. Recently this change has been only 4%.

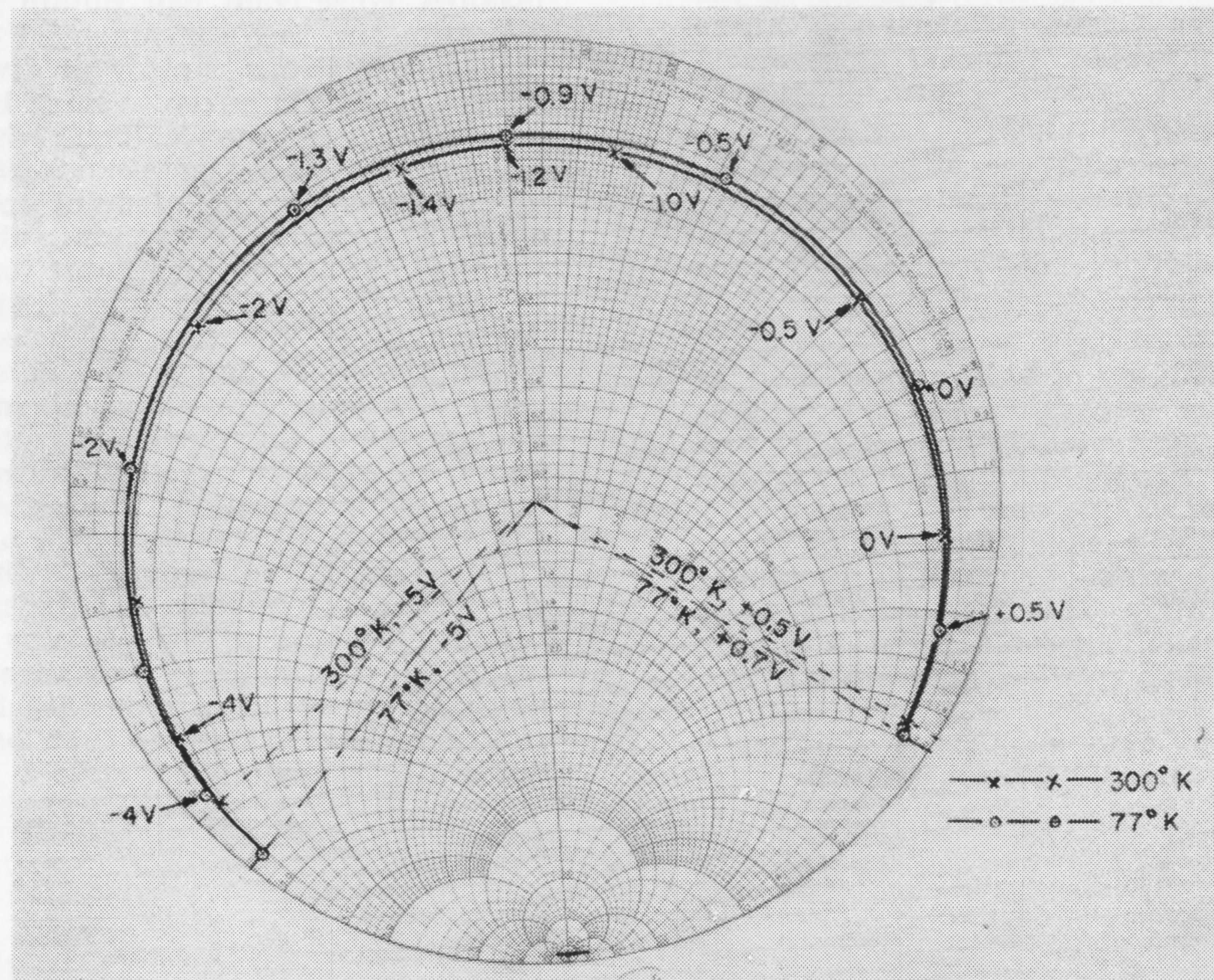


Figure 4—Impedance loci of the refined diode at 300°K and 77°K (measured at 5.85 Gc). Circles represent the impedance at 77°K; and crosses at 300°K. Dynamic quality factor is 7.8 at 300°K and is 9.3 at 77°K.

## SESSION VI: Low Noise Amplification

### TM 6.4: Field-Effect Transistors as Low-Noise Amplifiers

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Palo Alto, Calif.

THEORETICAL CALCULATIONS indicate that conventional semiconductor noise sources in a field-effect transistor should result in exceptionally good noise performance. Noise measurements on silicon field-effect transistors indicate that the pinch-off mechanism is the predominate noise source and usually limits the device noise figure. This noise is thought to be due to the very high electric fields in the pinch-off region. If one operates in a nonpinch-off condition, the noise figure is sometimes improved at a considerable sacrifice in gain.

Operating the device in the pinch-off condition<sup>1</sup> results in a very high output impedance and maximum gain with characteristics similar to those of a vacuum tube pentode. In the nonpinch-off condition the space-charge regions are not as close together and device amplification arises from modulation of the channel conductance.

The gate-drain capacitance,  $C_{gd}$ , is analogous to the *Miller* effect capacitance on the vacuum tubes, and thus it increases the effective input capacitance. If one is concerned about obtaining the highest input impedance possible, the load impedance should be kept low to decrease the *Miller* effect. From a noise point of view the *Miller* effect is not important as it does not change either the noise figure of the device, or the optimum noise impedance value as long as  $g_m \gg \omega C_{gd}$ .

The noise sources are positioned in the equivalent circuit so that  $i_{n1}$  physically represents the noise generated in the gate to source junction and  $i_{n2}$ , the noise in the source to drain channel. The circuit properties of these noise sources can be determined by external noise measurements using the equivalent circuit characteristics to separate one noise source from another.

The noise generator  $i_{n1}$  represents the noise caused by leakage currents in the reversed biased gate-source junction. This type of noise has a characteristic  $1/f$  slope and is very low and usually negligible on good planar type devices, with low leakage currents. High drain or gate voltages tend to increase this noise.

There are several different types of noise represented by the equivalent channel noise generator  $i_{n2}$ . At low frequencies there is  $1/f$  noise generated in the channel and on good devices this represents the only  $1/f$  noise source. Above the  $1/f$  noise frequencies one observes a frequency independent noise which has a magnitude equal to or often less than full shot noise when operating in the pinch-off region of transistor operation. This *reduced shot noise* is independent of drain voltage and for a given device,  $m$  remains constant over a wide variation of drain current,

$I_D$ . In various devices  $m$  has been observed to vary from 1 to 20.

Another noise effect, which appears to be analogous to induced grid noise in vacuum tubes, occurs at high frequencies. It is caused by channel electrons inducing a varying charge on the gate electrode, which in turn affects the probability of electrons passing through the pinched-off channel. This is represented in the equivalent circuit by both  $i_{n1}$  and  $i_{n2}$  as correlated noise sources. In the previous discussion it was assumed that  $i_{n1}$  and  $i_{n2}$  were physically separate and uncorrelated noise sources. Experimentally, this *induced gate noise* has been observed to cancel partially the channel noise in the device, thus improving the noise performance. Induced grid noise in vacuum tubes is a very high-frequency effect, but in field-effect transistors this *induced gate-noise* effect is observed at as low as 5 to 20 kc. As the frequency is increased this effect increases very rapidly and should be considered in a representation of the noise.

For lower frequencies, where this gate-modulation effect does not occur, the important noise sources are the  $i_{n2}$  channel  $1/f$  noise and *reduced shot noise*. Then one can characterize the noise of the device with an input noise resistance,  $R_n$ , as is done in vacuum tubes. For frequencies in the  $1/f$  noise range,  $R_n$  is a function of frequency. The optimum source conductance,  $G_s$ , is spelled out in Figure 5.

Sometimes, when the device used has high channel or leakage noise, one can obtain the best noise figure by operating in the non-pinchoff region. Since the device power gain drops rapidly at drain voltages below pinchoff voltage, a compromise must be made between gain and best noise performance. The *reduced shot noise*, avalanche noise, and induced gate-noise effect previously discussed, do not appear in this mode of operation and the remaining channel noise is very low, although it is still above thermal noise. The bias point for best noise figure appear to vary greatly from one device to another. On some devices these low bias voltages do not improve significantly the noise figure. The noise data plotted was measured well into the pinchoff region of operation (drain voltage triple the pinchoff voltage). This type of operation is often more practical, although perhaps not the best for noise optimization. The data shows a noise figure at one-megohm source resistance of less than 2 db from 120 cps to 150 kc, and around .3 db over most of the range. At the high-frequency end the noise could be reduced by tuning out the 7-pf device, plus wiring capacitance or by using a lower source resistance. At low frequencies the noise factor could be considerably improved by using a source resistance greater than one megohm, since for this device  $i_{n1}$  is negligible.

<sup>1</sup> Dacey, G. C., and Ross, I. M., "The Field-Effect Transistor," *Bell System Tech. Journal*, p. 1149-1189; November, 1955.

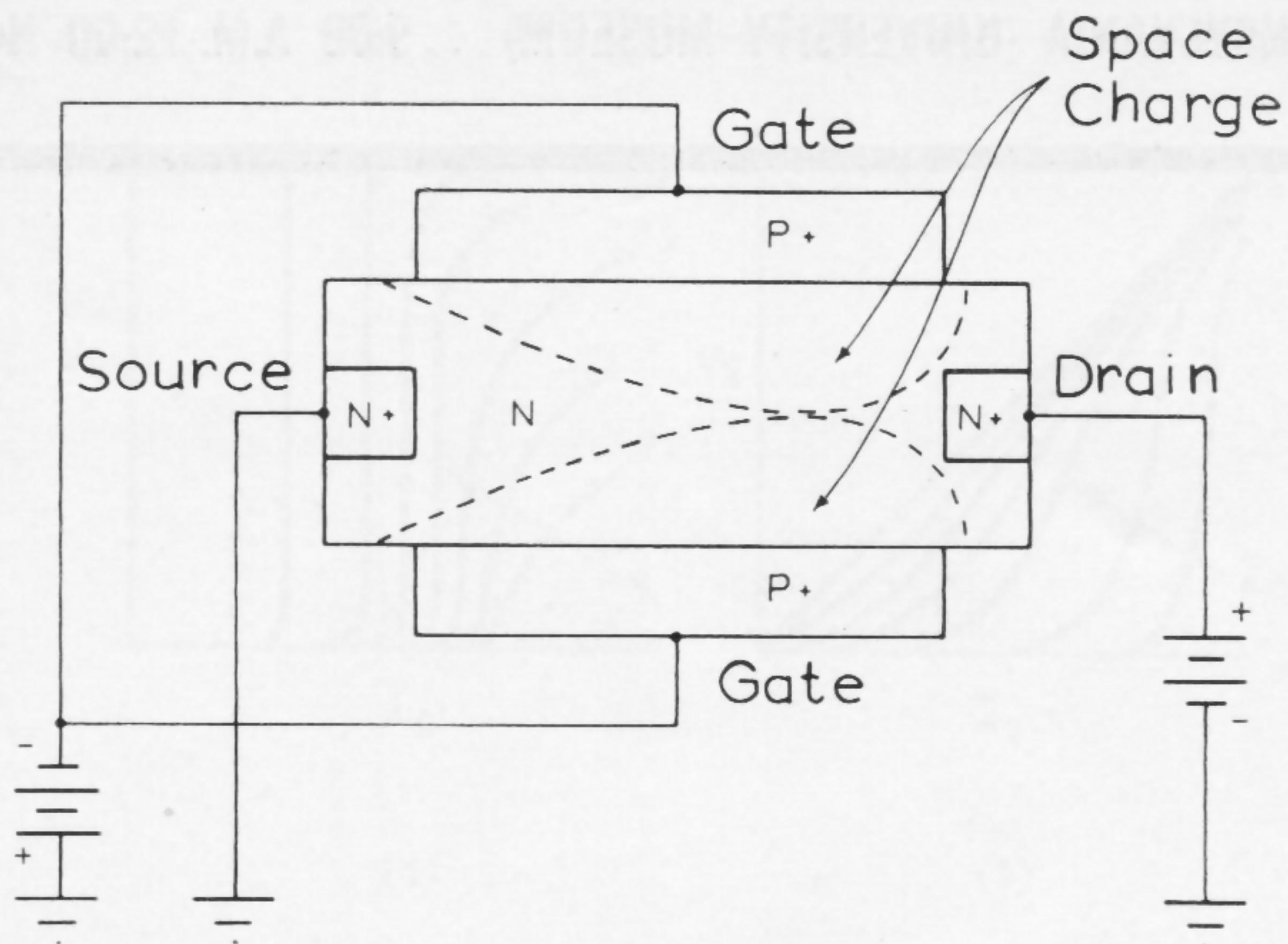


Figure 1—Field-effect transistor in pinch-off mode of operation

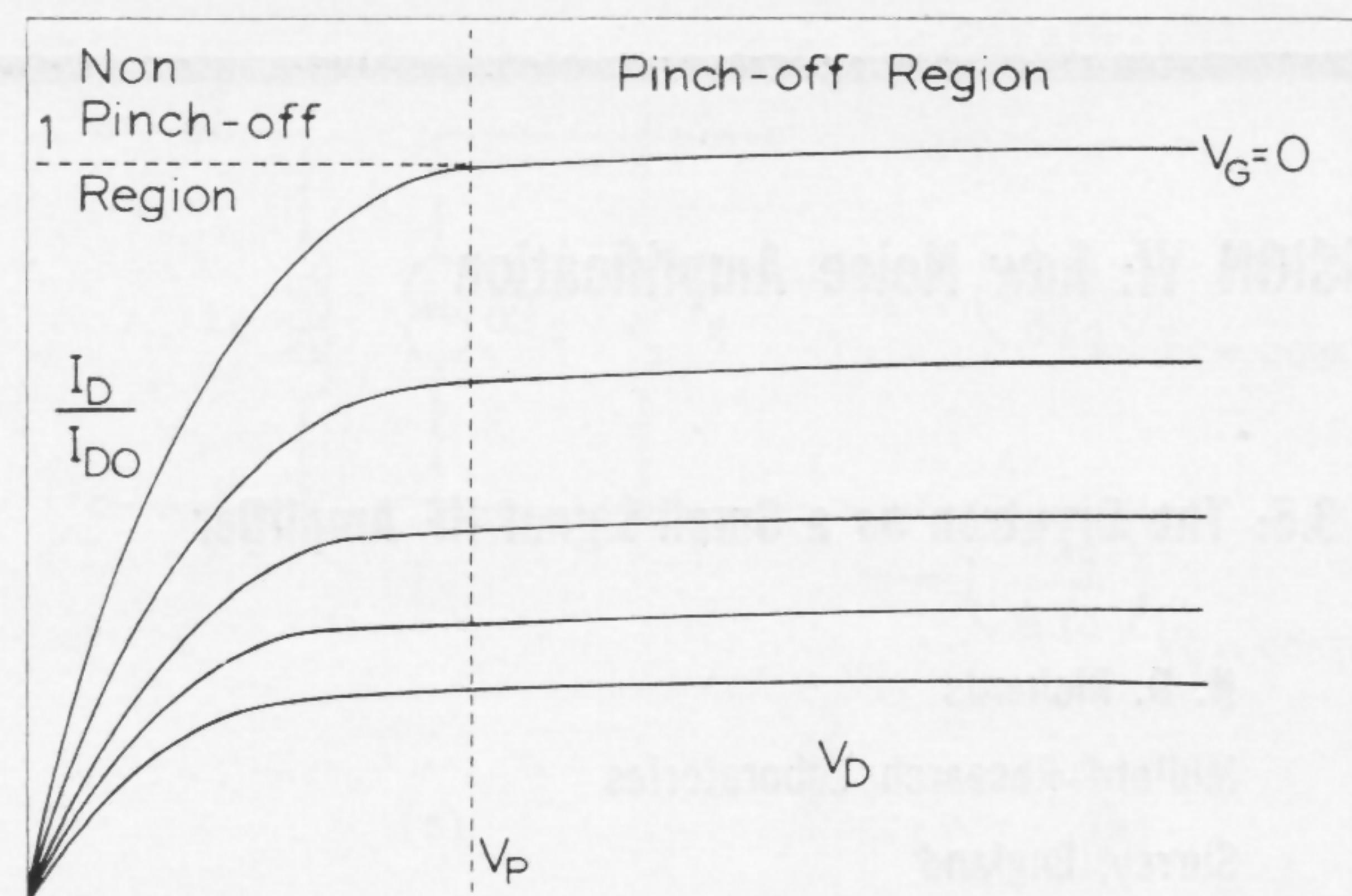


Figure 2—Characteristic dc curves. Normalized drain current,  $I_D$ , versus drain voltage,  $V_D$ , is shown for various gate voltages.

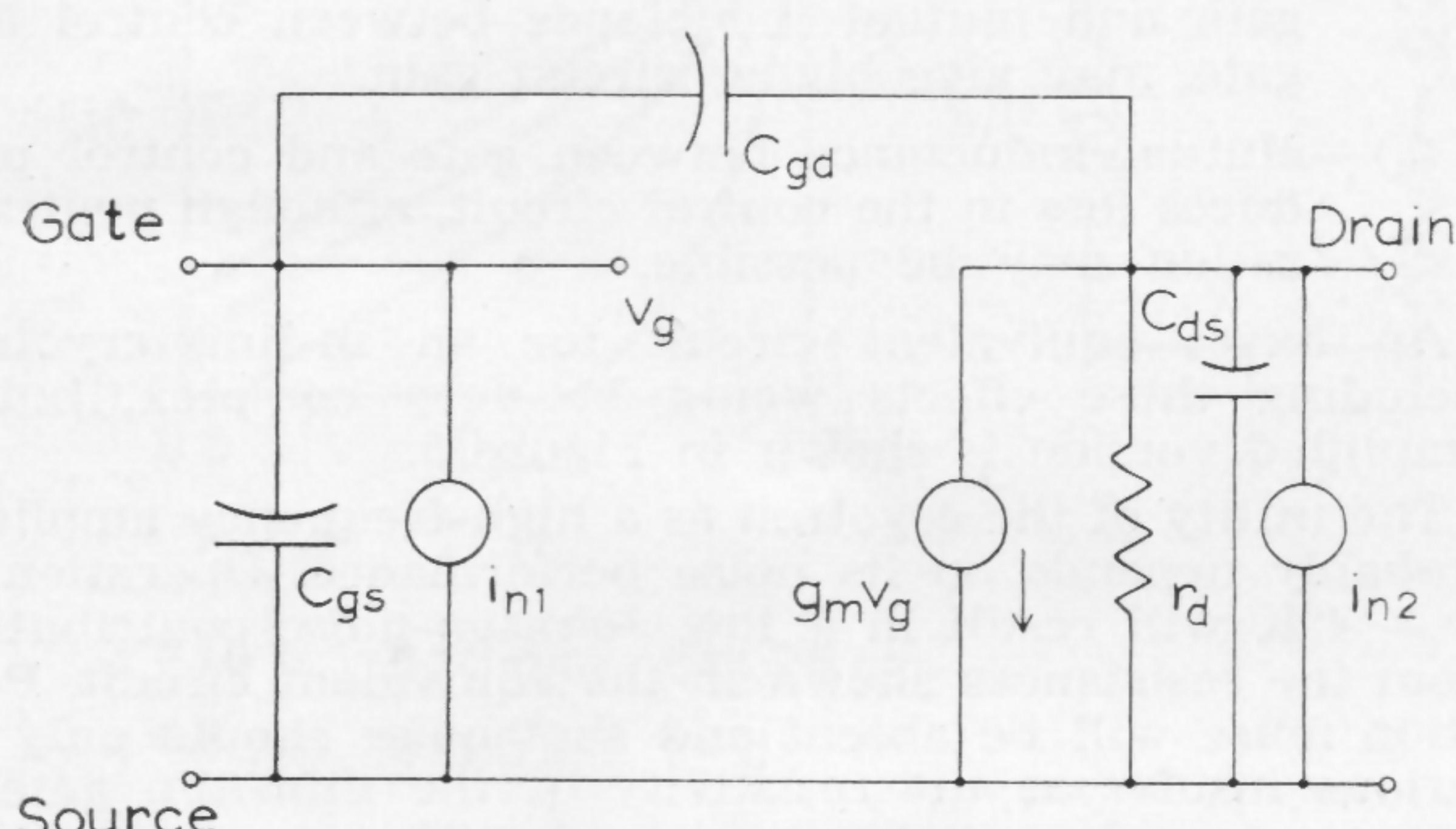


Figure 3—Small signal equivalent circuit with equivalent noise sources.

CIRCUIT ELEMENT	PINCH-OFF REGION	NON-PINCH-OFF REGION
$C_g = C_{gs} + C_{gd}$	4 pf	5 pf
$C_{gs}$	2 pf	—
$C_{gd}$	2 pf	—
$g_m$	200 - 300 $\mu$ hos	60 $\mu$ hos
$r_d$	0.2 - 1 m $\Omega$	4 k $\Omega$

Figure 4—Typical equivalent circuit element values for developmental device.

$$\text{Reduced Shot Noise: } \overline{i_{n2}^2} = \frac{2e I_d \Delta f}{m}$$

$$\text{Noise Resistance: } R_n = \frac{\overline{i_{n2}^2}}{4KT \Delta f g_m^2}$$

$$\text{Optimum } G_S: \quad G_0 = \sqrt{\frac{\overline{i_{n1}^2}}{\overline{i_{n2}^2}} g_m^2 + \omega^2 C_g^2}$$

$$\text{Optimum Noise Figure: } F_0 = 1 + 2R_n G_0$$

$$\text{Noise Figure with } i_{n1} \approx 0: \quad F = 1 + R_n \left( G_S + \frac{\omega^2 C_g^2}{G_S} \right)$$

Figure 5—Noise formulas. These formulas do not include the induced gate-noise effect.

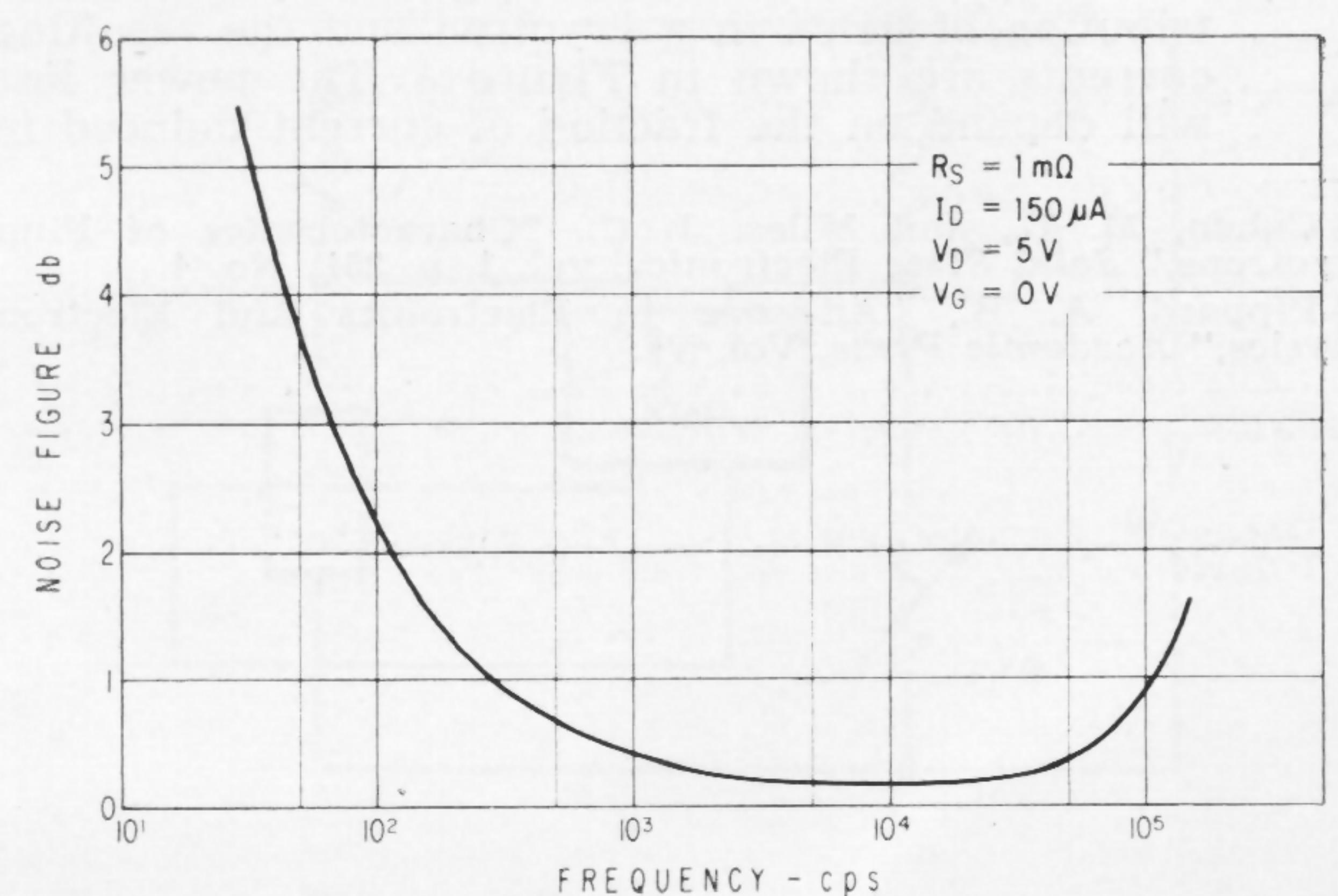


Figure 6—Noise figure versus frequency on a developmental device.

## SESSION VI: Low Noise Amplification

## TM 6.5: The Cryotron as a Small-Signal HF Amplifier

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Mullard Research Laboratories  
Surrey, England

THE USE OF THIN-FILM cryotrons as computer-switching elements, using the large-signal non-linear properties of the device, is well established. Its use as a small signal linear amplifier has received less attention, although a typical set of *dc* characteristics (Figure 1) are the approximate duals of tube characteristics.

The cryotron may be approximately specified as a switching element by three parameters: Large signal current gain  $G$ , gate normal resistance  $R_g$ , and control inductance  $L_c$ . The behavior of a cryotron as a small signal amplifier may be specified approximately by three similar parameters:  $r_g$ ,  $\alpha$  and  $L_c$ ; Figure 2b. Optimum biasing results in the small signal parameters  $\alpha$  and  $r_g$  showing significant improvement over the related large signal parameters  $G$  and  $R_g$ .

At frequencies which are not too high, the cross-film cryotron may be represented by the equivalent circuit of Figure 2a. A cascaded amplifier composed of identical stages would have a bandwidth  $B = R_g/2\pi L_c$  (neglecting  $L_g$ ). For crossed-film cryotrons having given insulator and conductor thicknesses, the product  $BG^2$  is a constant<sup>1</sup> which may be of the order of 200 Mc. Foreseeable improvements in materials and techniques should increase this product by at least an order of magnitude and, as  $r_g$  and  $\alpha$  will generally be greater than  $R_g$  and  $G$ ,  $B\alpha^2$  products of several kMc may be anticipated.

The simple equivalent circuit of Figure 2a would predict an infinite power gain. This is not to be expected in practice and so possible sources of control circuit loss—outlined below—should be considered:

- (1)—Irreversibility of magnetic field induced transitions results in hysteresis loss, which is a function of signal amplitude and frequency.
- (2)—Superconductors have a finite resistivity at high frequencies; Figure 3<sup>2</sup>. This effect becomes significant above 1 kMc.
- (3)—High-frequency currents in the control will induce eddy currents in the resistive gate. A possible distribution of fields in a cryotron and the resulting currents are shown in Figure 4. The power loss will depend on the fraction of current induced in

the gate and the gate high-frequency resistivity.

- (4)—Matching and coupling networks introduce loss. Crossed-film cryotrons have impedances of the order of  $10^{-3}$  ohms, which must be matched to impedances of the order of 50 ohms in practical applications. In-line cryotrons have higher impedances and so, despite their fractional current gain and mutual inductance between control and gate, may give higher circuit gain.
- (5)—Mutual inductance between gate and control produces loss in the control circuit, although neutralization may be possible.

An exact equivalent circuit for an in-line cryotron including these effects would be very complex, but a simplified version is shown in Figure 5.

The utility of the cryotron as a high-frequency amplifier probably depends on its noise performance. Operation at  $3^\circ - 4^\circ$ K will result in a low *Johnson*-noise contribution from the resistances shown in the equivalent circuit. Partition noise will be absent and shot noise should only be serious insofar as the resistivity of the thin-film gate is due to tunneling between islands. The most probable source of noise is noise due to irreversible changes connected with the nucleation and movement of normal domains in the gate. This will result in noise similar to *Barkhausen* noise in ferromagnetics; i.e., it will be frequency dependent and a non-linear function of signal amplitude. It is hoped that cryotrons may be constructed in which the superconducting—normal domain walls may move quasi-reversibly, and thus not result in a serious source of noise.

The correct biasing of the cryotron is important. For experimental purposes it is convenient to define the gate current by means of an external voltage source and a resistor. The control current may be varied by an external servo amplifier to maintain the gate bias voltage constant; Figure 6. The gate power dissipation must be restricted so as to prevent thermal switching. For convenience, external coaxial matching elements have been used, although eventually it is envisaged that these may be made superconducting.

Due to the signal-amplitude dependence of the noise sources it is necessary to use methods of noise measurement that measure actual signal-to-noise ratios, i.e., involving the use of a *cw* signal source.

<sup>1</sup> Cohen, M. L., and Miles, J. C., "Characteristics of Film Cryotrons," *Solid State Electronics*, vol. 1, p. 351; No. 4.

<sup>2</sup> Pippard, A. B., "Advance in Electronics and Electron Physics," *Academic Press*, Vol. VI.

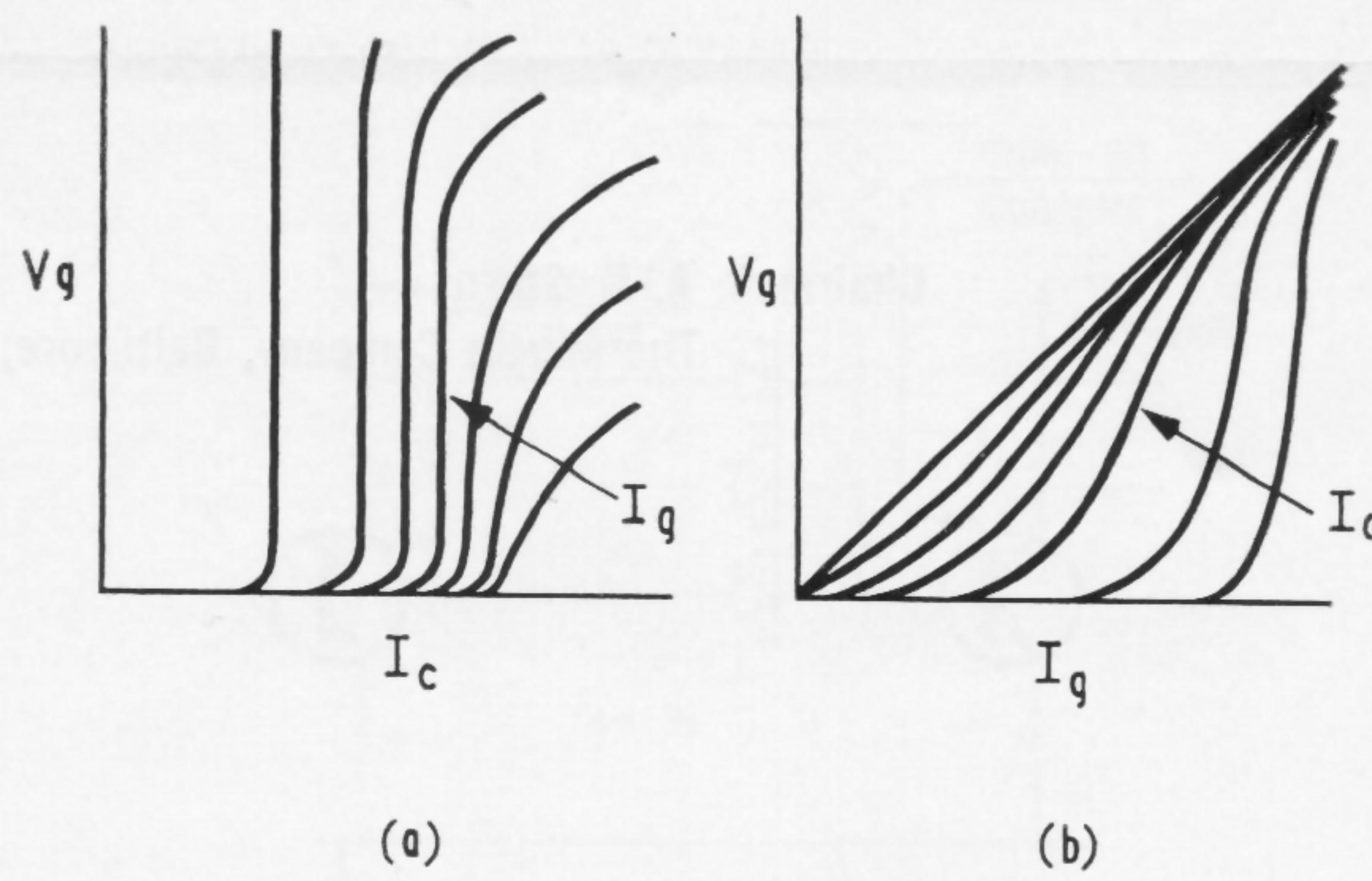


Figure 1—Cryotron *dc* characteristics are duals of thermionic valve characteristics: (a)—Mutual (or quenching) characteristics; (b)—gate characteristics.

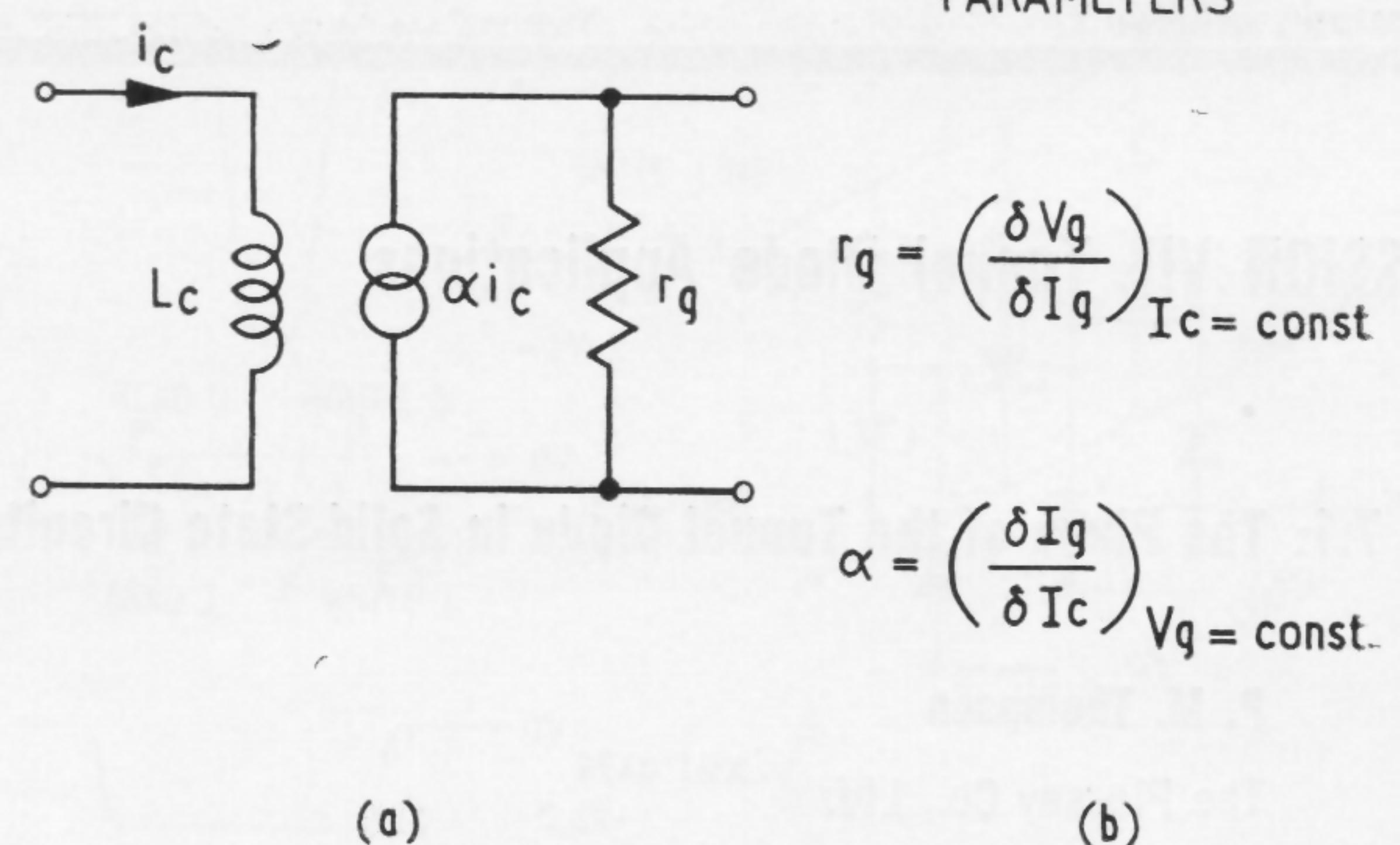


Figure 2—(a)—Low-frequency equivalent circuit of crossed-film cryotron; (b)—parameters  $\alpha$  and  $r_g$  are related to large signal parameters but may be higher in value.

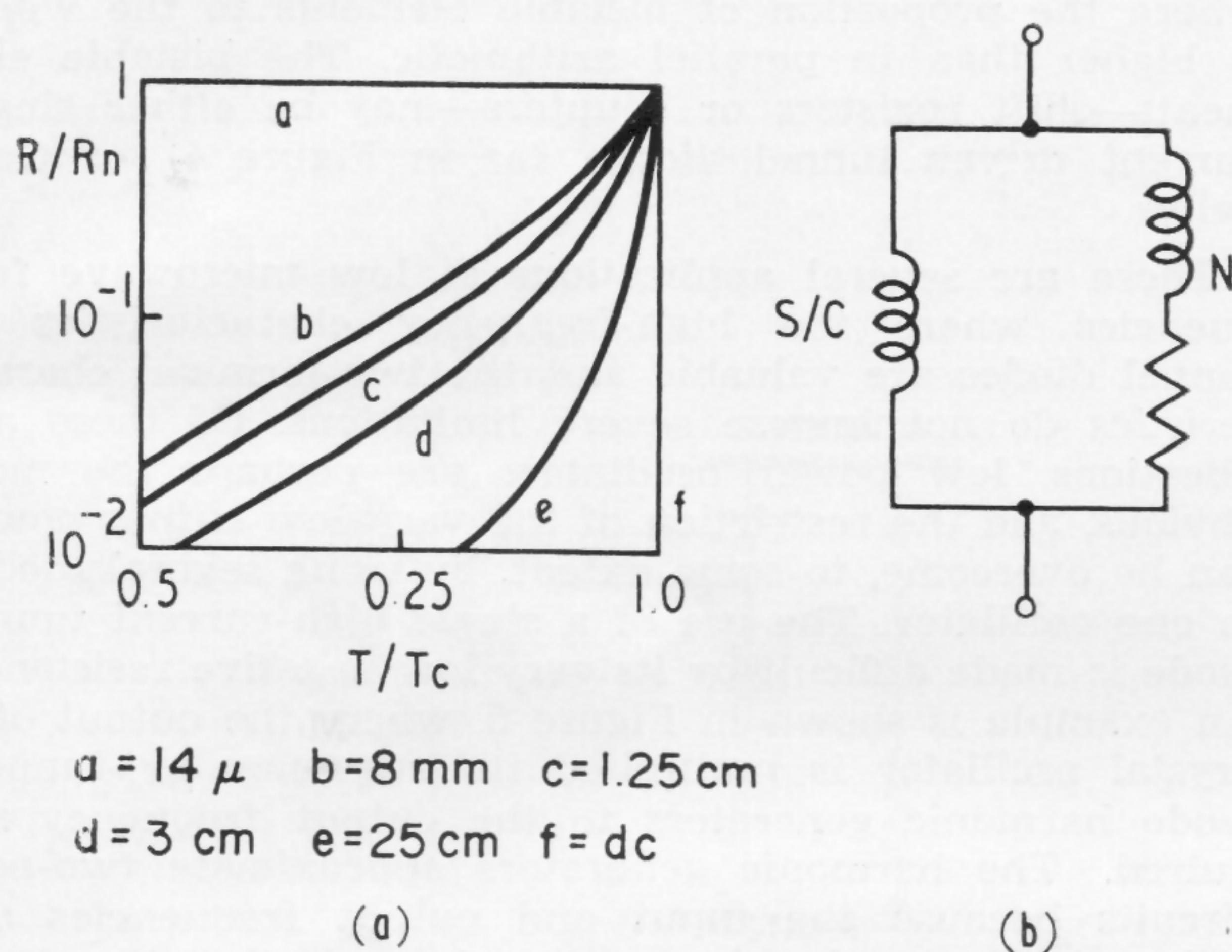


Figure 3—At high frequencies superconductors show resistance, as noted in (a). Superconducting electrons no longer short the normal electrons as shown in (b) where we have an approximate equivalent circuit.

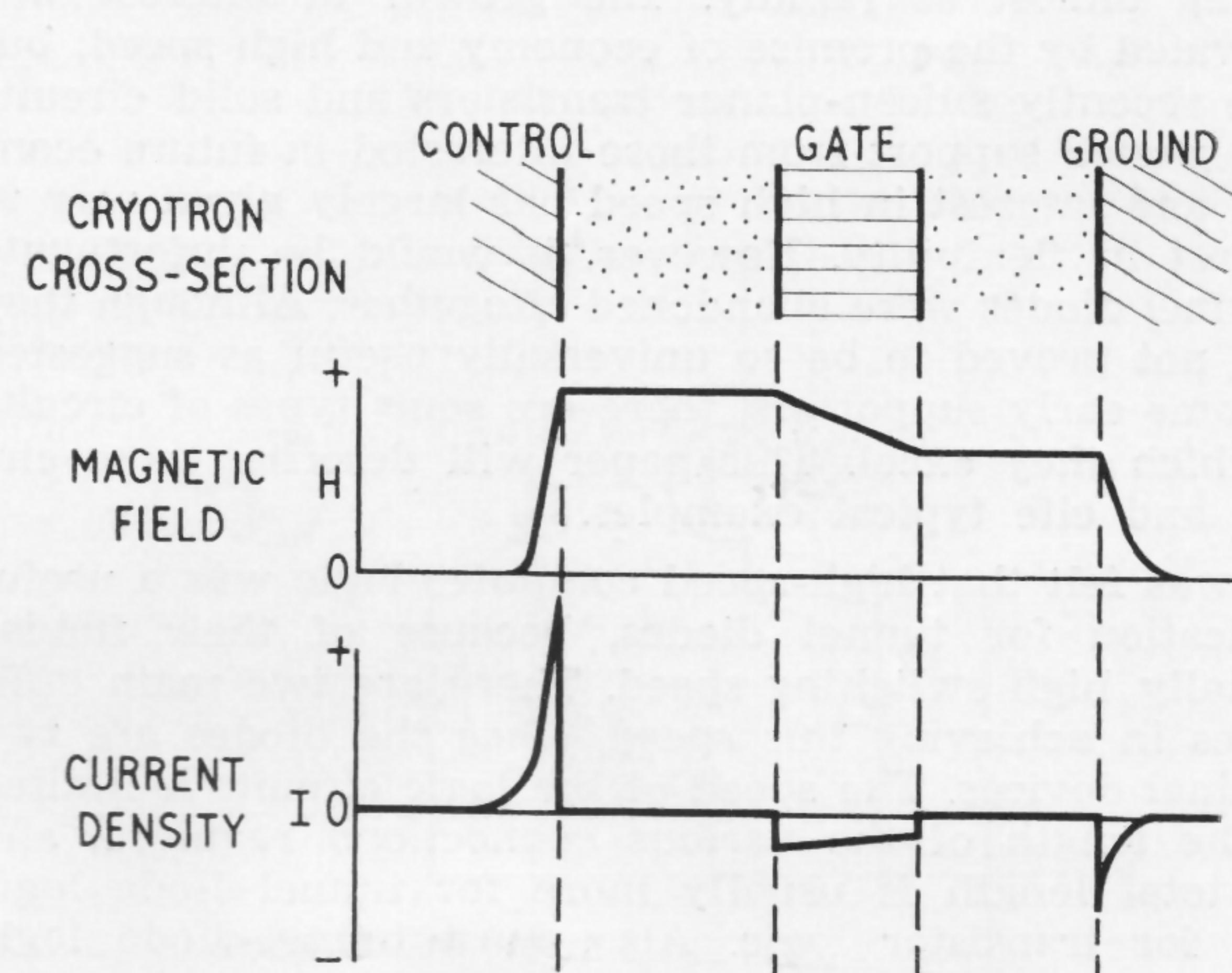


Figure 4—High-frequency control current induces image currents in gate and ground plane. Current in gate gives power loss which depends on gate thickness and resistivity.

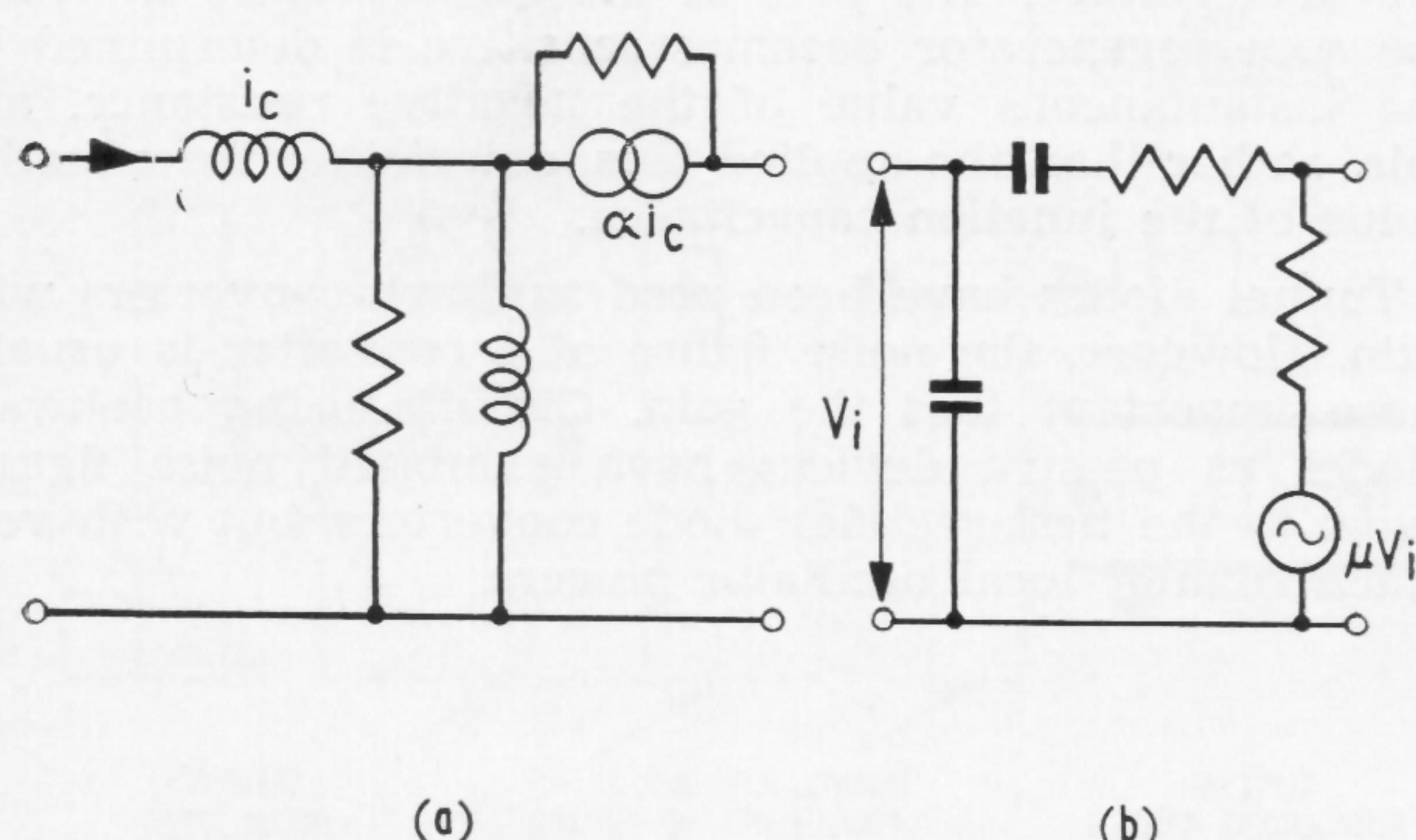


Figure 5—(a)—Simplified high-frequency equivalent of in-line cryotron; (b)—dual of this circuit showing similarity to tube or transistor.

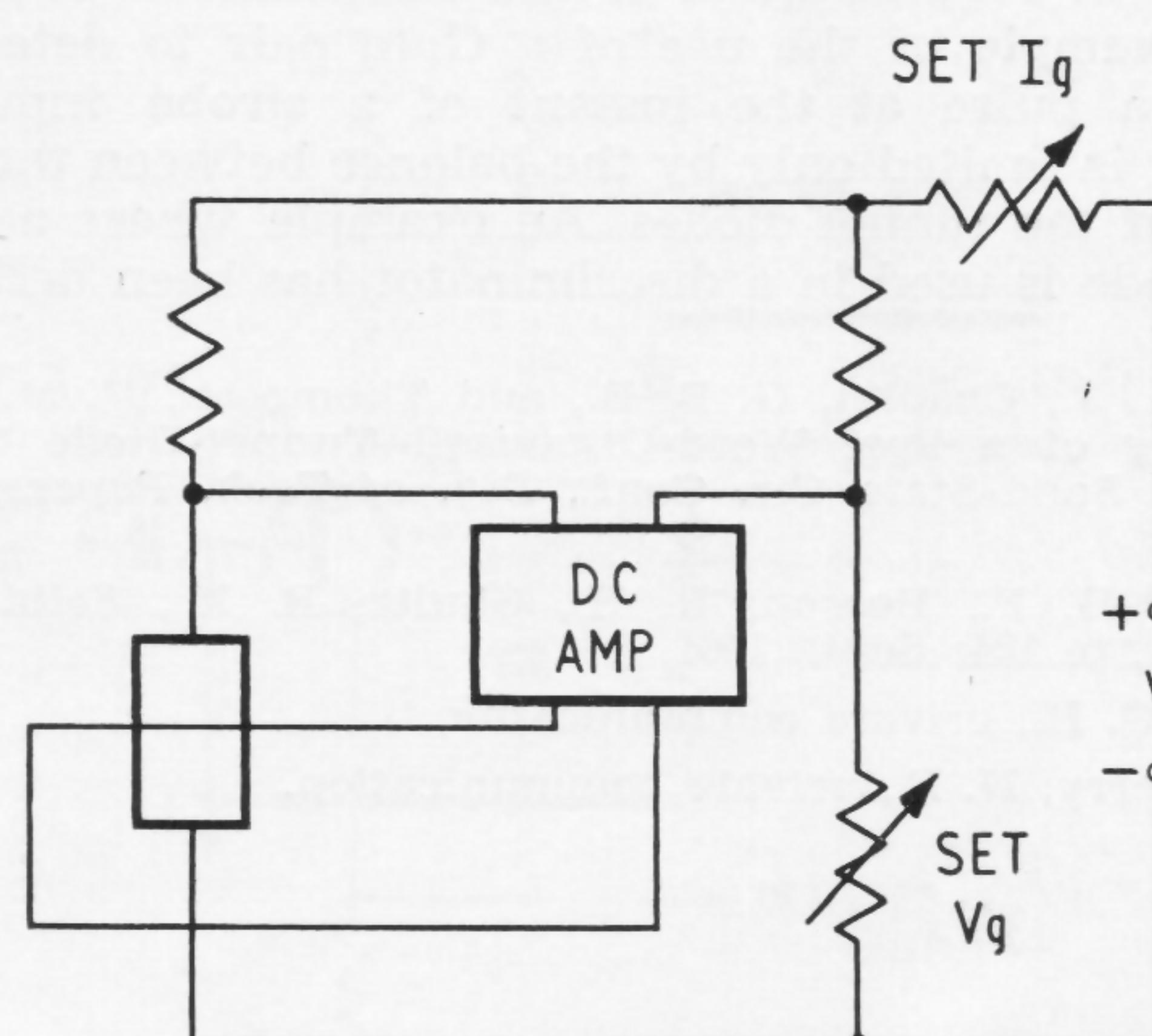


Figure 6—Bias stabilization circuit. Gate current is defined by resistor. Gate voltage is maintained constant by means of *dc* amplifier supplying control current.

## SESSION VII: Tunnel Diode Applications

Chairman: A. P. Stern

The Martin Company, Baltimore, Md.

### TA 7.1: The Place of the Tunnel Diode in Solid-State Circuits

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IN THE PAST THREE YEARS interest in tunnel diodes as circuit elements has grown rapidly, and now it appears to be waning almost as rapidly. The growth in interest was motivated by the promise of economy and high speed; but more recently silicon-planar transistors and solid circuits have gained support from those interested in future economy, and interest in high speed has largely given way to interest in flexibility. However, it would be unfortunate if tunnel diodes were abandoned altogether. Although they have not proved to be so universally useful as suggested by some early supporters, there are some types of circuits in which they excel. This paper will describe these circuits and cite typical examples.

It was felt that high-speed computer logic was a useful application for tunnel diodes, because of their fundamentally high switching speed. There are two main difficulties in achieving this speed, since the diodes are two terminal devices. The speed of the logic circuits is limited by the length of the various connections required, and this total length is usually more for tunnel-diode logic than for transistor logic. Also, most tunnel-diode logic systems suggested to date require multiphase clock waveforms which limit the speed of circuit operation. A more promising application is in transistor backward diode logic, which employs tunnel diodes with very low peak tunnel currents. The example shown in Figure 1 is suitable as a system of either high-speed logic or very low-current logic, and it may possibly prove suitable for silicon solid circuits.

Other computer applications are the fast store \* (Figure 2) and several specialized circuits, two examples of which are shown in Figures 3 and 4. The discriminator of Figure 4 is an example of the use of a *Goto* pair to detect the sense of a pulse at the instant of a strobe input. Its sensitivity is limited only by the balance between the peak currents of the tunnel diodes. An example where a single tunnel diode is used in a discriminator has been described

earlier \*. The incorporation of tunnel diodes into transistor circuits is particularly useful in serial arithmetic where the proportion of bistable elements to the whole is higher than in parallel arithmetic. The bistable elements—shift registers or counters—may be either single current driven tunnel diodes (as in Figure 4) or *Goto* pairs.

There are several applications at low microwave frequencies where the high-frequency characteristics of tunnel diodes are valuable and the two-terminal characteristics do not impose severe limitations. Of these applications, low power oscillators are perhaps the most obvious, and the restriction of the very low output power can be overcome, to some extent, by using several diodes in one oscillator. The use of a single high-current tunnel diode is made difficult by its very low negative resistance. An example is shown in Figure 5, where the output of a crystal oscillator is multiplied in frequency by tunnel-diode harmonic generators to the output frequency required. The harmonic generators approximate two-port circuits because the input and output frequencies are different. The mode of operation is such that the diode is driven in and out of its negative resistance region at the input frequency. At each cycle, there is a burst of oscillations in the output circuit, and, as the output waveform is repeated once per input cycle, it contains only harmonics of the input frequency.

The application of tunnel diodes as amplifiers is limited by their two-terminal characteristics, by the fact that their noise figure is higher than in parametric amplifiers, and by their small linear dynamic range. However, even with these limitations, they are very suitable for superregenerative amplifiers and detectors, a significant advantage being that the tuned frequency is not sensitive to the bias voltage. The part of the quench cycle in which the superregenerator becomes sensitive is determined by the instantaneous value of the negative resistance, and this, rather than the applied bias, determines the effective value of the junction capacitance.

Tunnel diodes have been used as down-converters with gain. However, the noise figure of a converter is usually more important than the gain. Circuits using backward diodes as passive devices have exhibited noise figures equal to the best rectifier diode converters, but with very much smaller local oscillator powers.

\* Cole, A. J., Chaplin, G. B. B., and Thompson, P. M., "The Engineering of a Fast Word-Organized Tunnel-Diode Store", 1962 Inter. Solid-State Cir. Conf., *Dig. of Tech. Papers*; Feb., 1962.

<sup>1</sup> Allison, D. F., Beeson, R. H., Shultz, R. M., *Solid State Electronics*, p. 134; Sept., 1961.

<sup>2</sup> Perry, G. H., private communication.

<sup>3</sup> Broadberry, N. E., private communication.

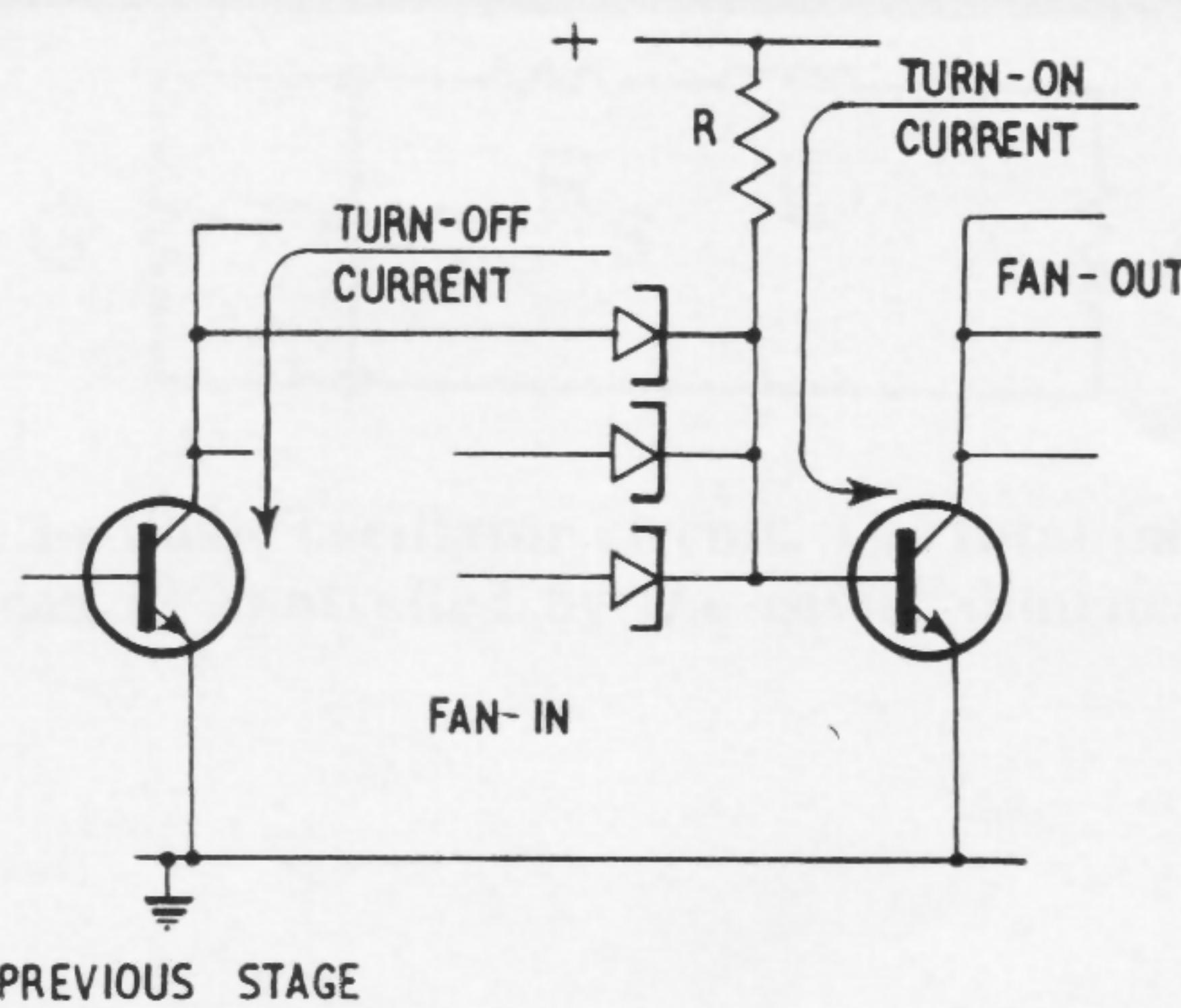


Figure 1—Transistor backward diode logic. Turn-on current controlled by  $R$ . Turn-off is fast because impedance of backward diode and saturated previous stage is low<sup>1</sup>.

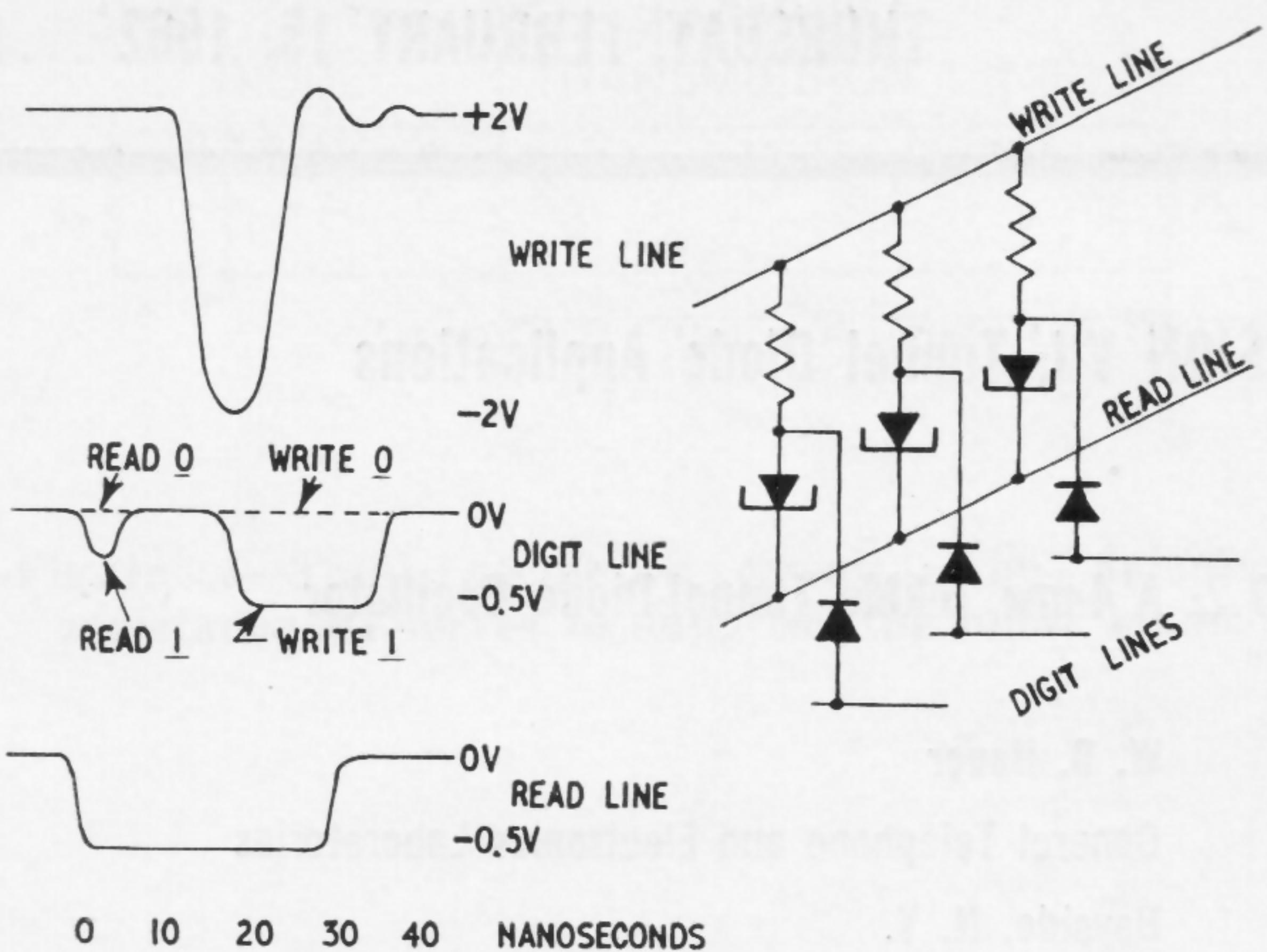


Figure 2—Three storage elements in one word of a tunnel diode computer store, shown with waveforms\*.

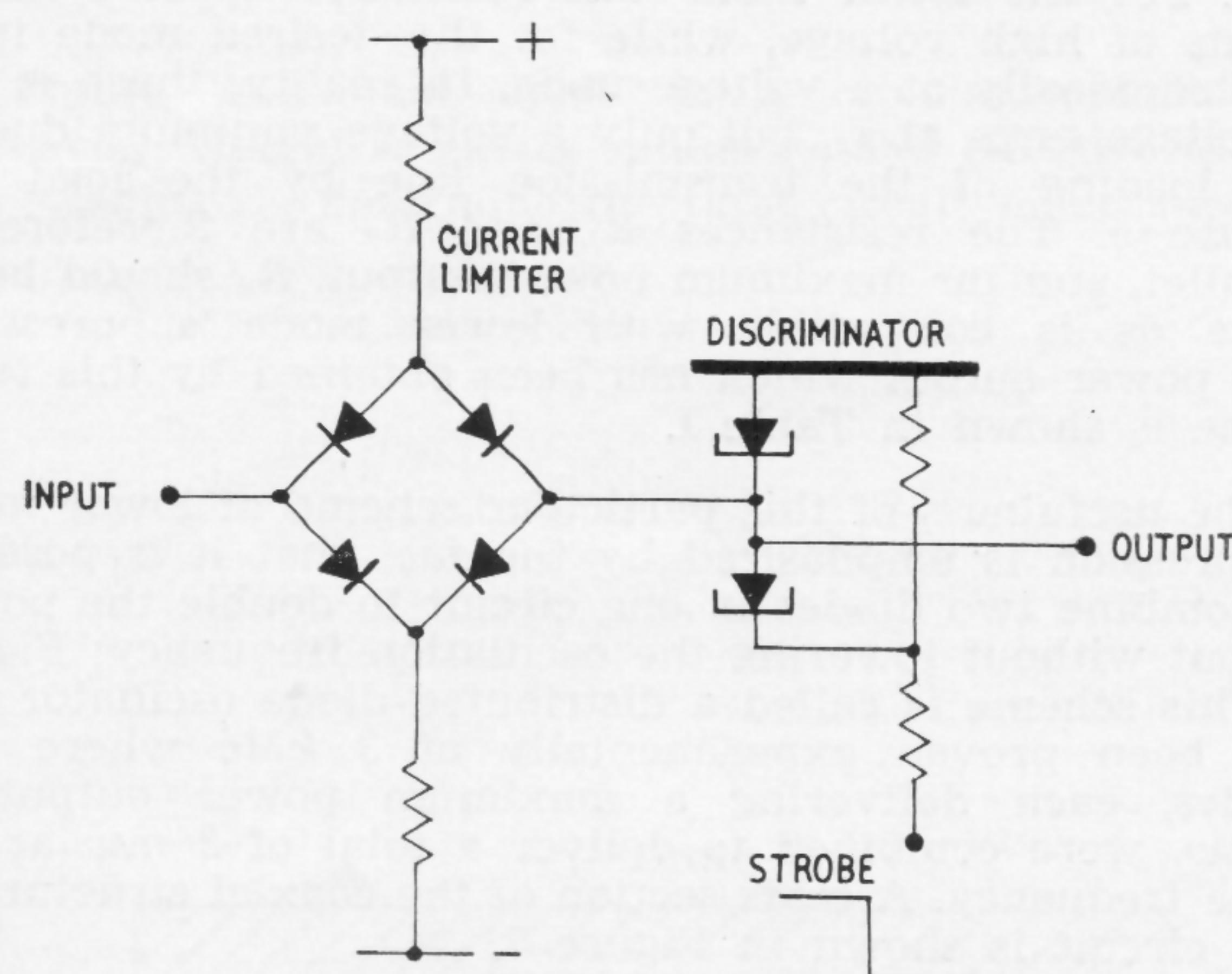


Figure 3—Goto pair discriminator used to detect the sense of a read signal from a core store at a time defined by strobe<sup>2</sup>.

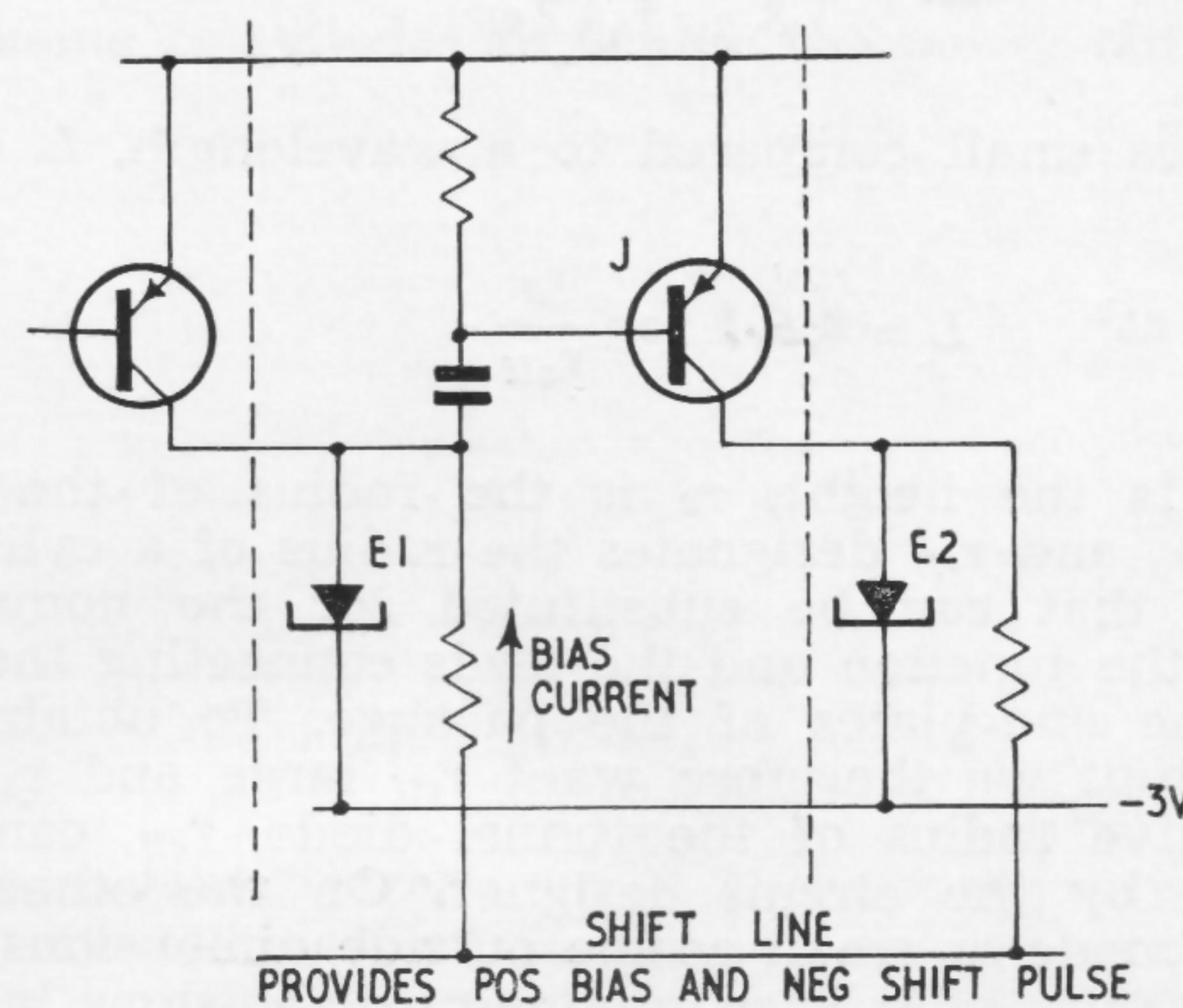


Figure 4—A 10-nsec shift register. Shift pulse switches  $E1$  from high to low voltage state. The resultant pulse is delayed and inverted by  $J$ , and switches  $E2$  high.

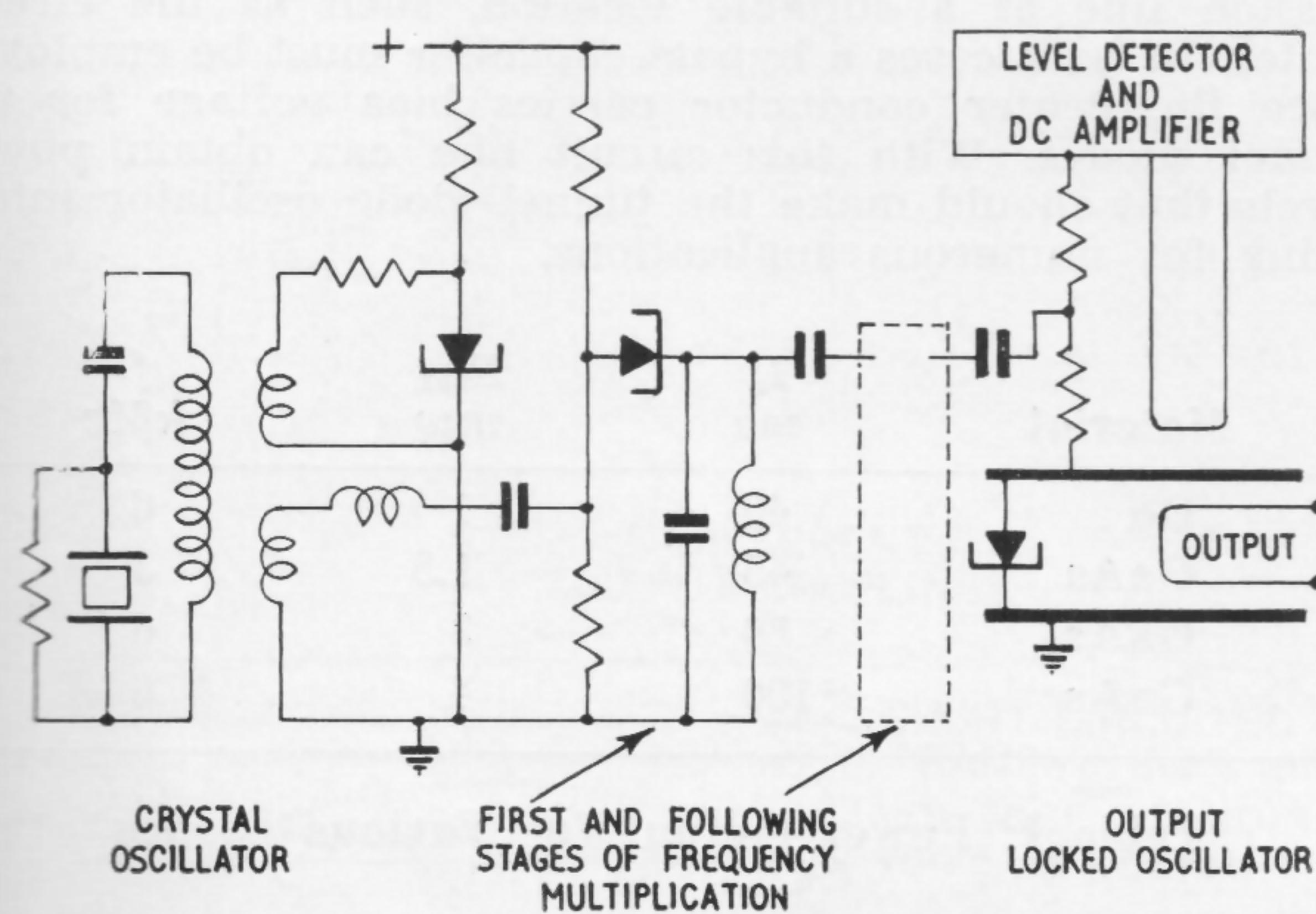


Figure 5—Simplified circuit of microwave low-power source: Tunnel-diode crystal oscillator, harmonic generators with gain, and multiple tunnel-diode locked oscillator<sup>3</sup>.

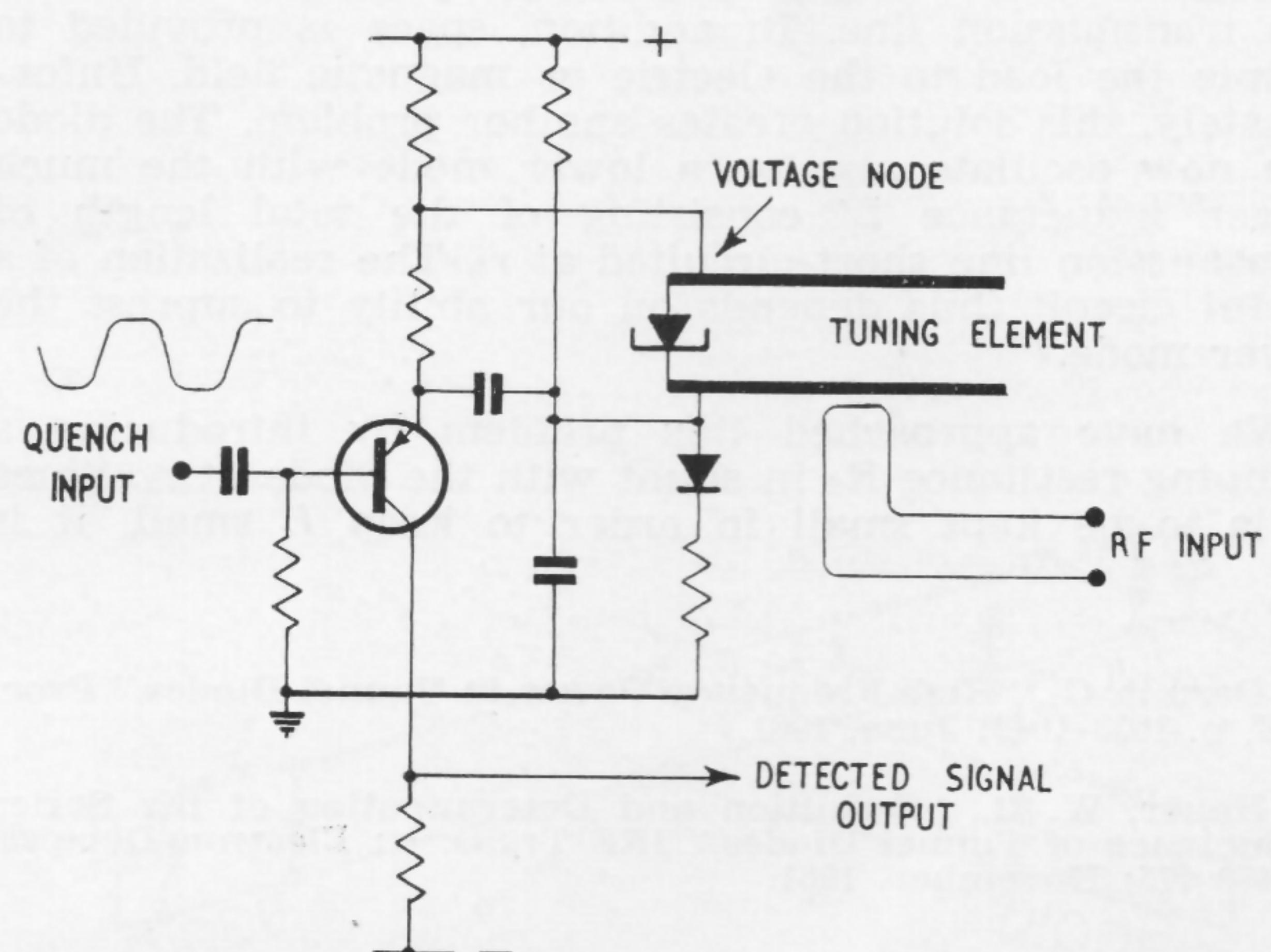


Figure 6—A superregenerative amplifier-detector. Tunnel diode provides variable negative conductance. Transistor provides bias voltage, and functions as common base amplifier for output<sup>3</sup>.

## SESSION VII: Tunnel Diode Applications

## TA 7.2: A 4-mw, 6-kMc Tunnel-Diode Oscillator

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IT HAS BEEN SHOWN in the literature<sup>1</sup> that the power output from tunnel-diode oscillators, under certain assumptions, is inversely proportional to the series inductance  $L$  of the oscillator circuit (Figure 1):

$$P_{out} = \frac{(\Delta V)^2}{8} \frac{1}{L} \left( \frac{1}{2\omega} - CR_s \right) \quad (1)$$

For cavities small compared to a wavelength,  $L$  can be

$$\text{expressed as}^2 \quad L = 4.6 h \log \frac{r_2}{r_{eff}} \quad (2)$$

where  $h$  is the height,  $r_2$  is the radius of the cavity (Figure 2), and  $r_{eff}$  designates the radius of a cylindrical conductor that can be substituted for the nonuniform radius of the junction and the leads connecting the junction to the end-plates of the package. To obtain large power output we therefore want  $r_{eff}$  large and  $r_2$  small. The effective radius of the tunnel diode,  $r_{eff}$ , cannot be influenced by the circuit designer. On the other hand,  $r_2$  can be made as small as the outside dimensions of the diode. A cavity with such minimum dimensions is shown in Figure 3. The major disadvantages of this arrangement are, first, the frequency of oscillation is completely determined by the diode parameters, particularly the junction capacitance; and second, it is very difficult to couple the load to the cavity by means of a probe or loop, due to the small dimensions involved. These shortcomings can be resolved by increasing the electrical length of the cavity radius by  $\lambda/2$ ; Figure 4. Instead of a physical short circuit, a voltage node is then located at  $r_2$ . The frequency of oscillation can now be controlled by the dimensions of the transmission line. In addition, space is provided to couple the load to the electric or magnetic field. Unfortunately, this solution creates another problem. The diode can now oscillate also on a lower mode with the much larger inductance  $L'$  consisting of the total length of transmission line short-circuited at  $r_2$ . The realization of a useful circuit thus depends on our ability to suppress the lower mode.

We have approached this problem by introducing a damping resistance  $R_d$  in shunt with the diode at  $r_2$ . Since  $r_2$  is to be kept small in order to keep  $L$  small, it is

required that  $R_d$  be introduced into the circuit at as small a radius as possible. This problem can be attacked by applying a resistive coating to the ceramic spacer of the diode that connects to the upper and lower diode terminals. For the lower mode this resistance appears across points of high voltage, while for the desired mode it is, located ideally at a voltage node. In reality, there is not a voltage node at  $r_2$ , but only a voltage minimum due to the loading of the transmission line by the load  $R_L$ ; Figure 5. The resistances  $R_L$  and  $R_d$  are therefore in parallel, and for maximum power output,  $R_d$  should be as large as is compatible with lower mode suppression. The power output which has been obtained by this technique is shown in Table I.

The usefulness of this particular scheme of lower mode suppression is emphasized by the fact that it is possible to combine two diodes in one circuit to double the power output without lowering the oscillation frequency; Figure 6. This scheme is called a distributed-diode oscillator and has been proven experimentally at 3 kMc where two diodes, each delivering a maximum power output of 1 mw, were combined to deliver a total of 2 mw at the same frequency. A cross section of the coaxial structure of this circuit is shown in Figure 7.

The principle outlined is not restricted to the combination of only two diodes. A suitable circuit arrangement for three or more diodes is indicated in Figure 8. If the diodes are perfectly matched, the available power output increases proportionally to the number of diodes used. In practice, the mismatch of diode characteristics limits their useful number. Mechanical tunability can be obtained with a tuning stub; for example, with a movable short located at the end of one of the transmission lines approximately  $\lambda/4$  from the circuit center. Voltage tuning is achieved by placing a varactor diode across the transmission line at a suitable location, such as the circuit center. In both cases a bypass capacitor must be employed since the center conductor carries bias voltage for the tunnel diodes. With this circuit one can obtain power levels that should make the tunnel-diode oscillator interesting for numerous applications.

Material	$I_p$ ma	$P_{out}$ mw	$f$ kMc
Ge	40	1	6
GaAs	45	1.5	3
GaAs	80	3	6
GaAs	100	4	6

Table I: Power Output for Various Diodes

<sup>1</sup> Dermit, G., "High Frequency Power in Tunnel Diodes," *Proc. IRE*, p. 1033-1042; June, 1961.

<sup>2</sup> Hauer, W. B., "Definition and Determination of the Series Inductance of Tunnel Diodes," *IRE Trans. on Electron Devices*, p. 470-475; November, 1961.

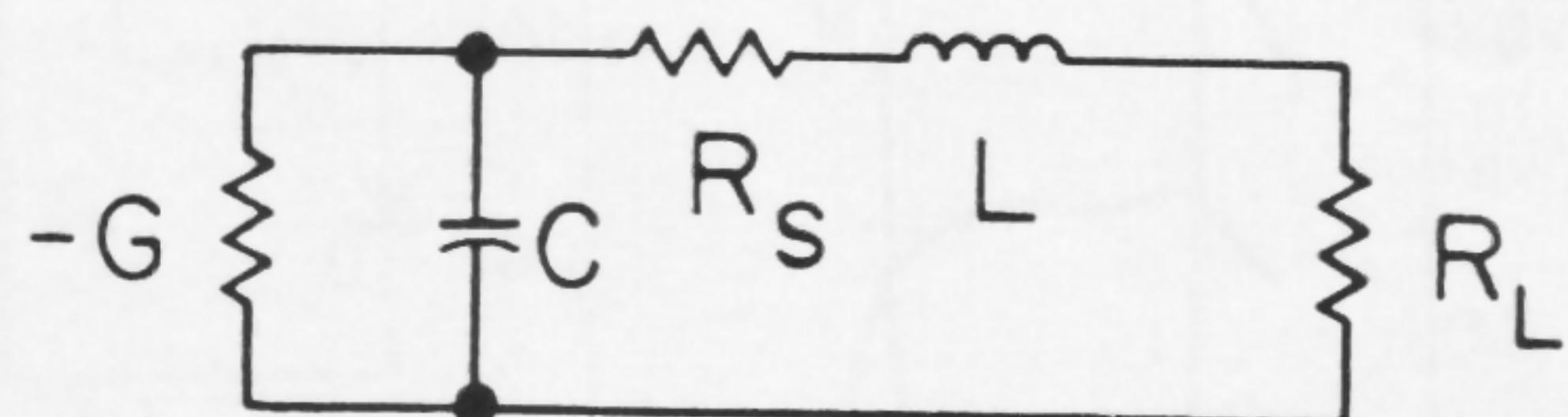


Figure 1—Basic oscillator circuit. The total inductance  $L$  can be controlled by the cavity dimensions.

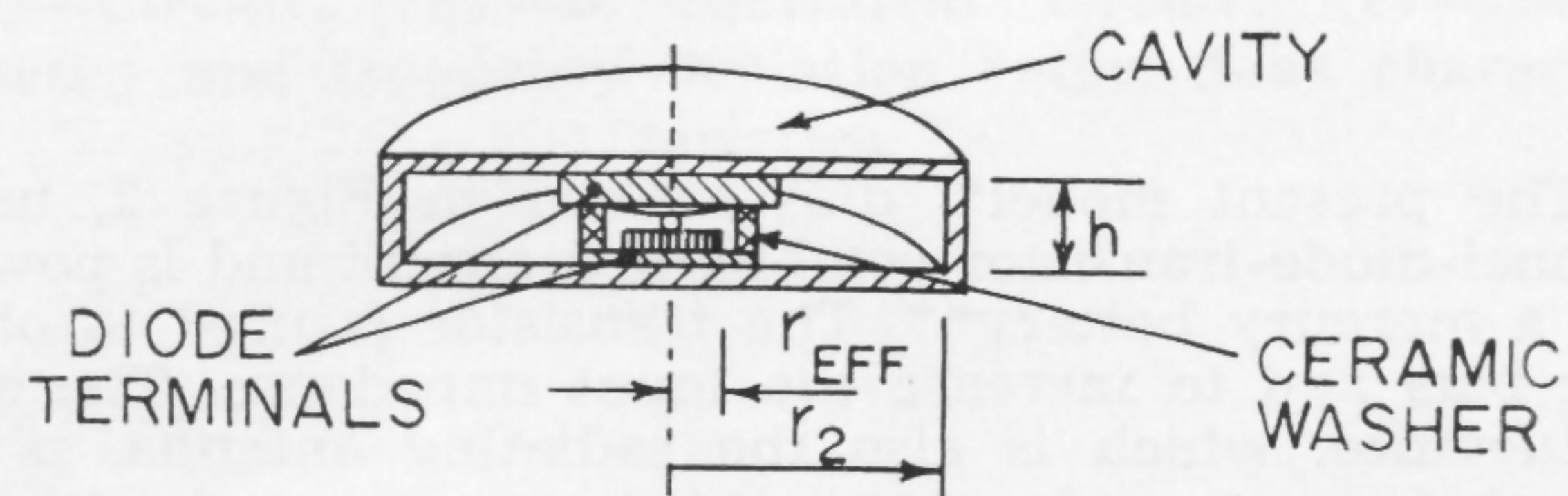


Figure 2—Tunnel diode in a circular cylindrical cavity. Height  $h$ , cavity radius  $r_2$ , and effective diode radius  $r_{eff}$  determine the total circuit inductance.

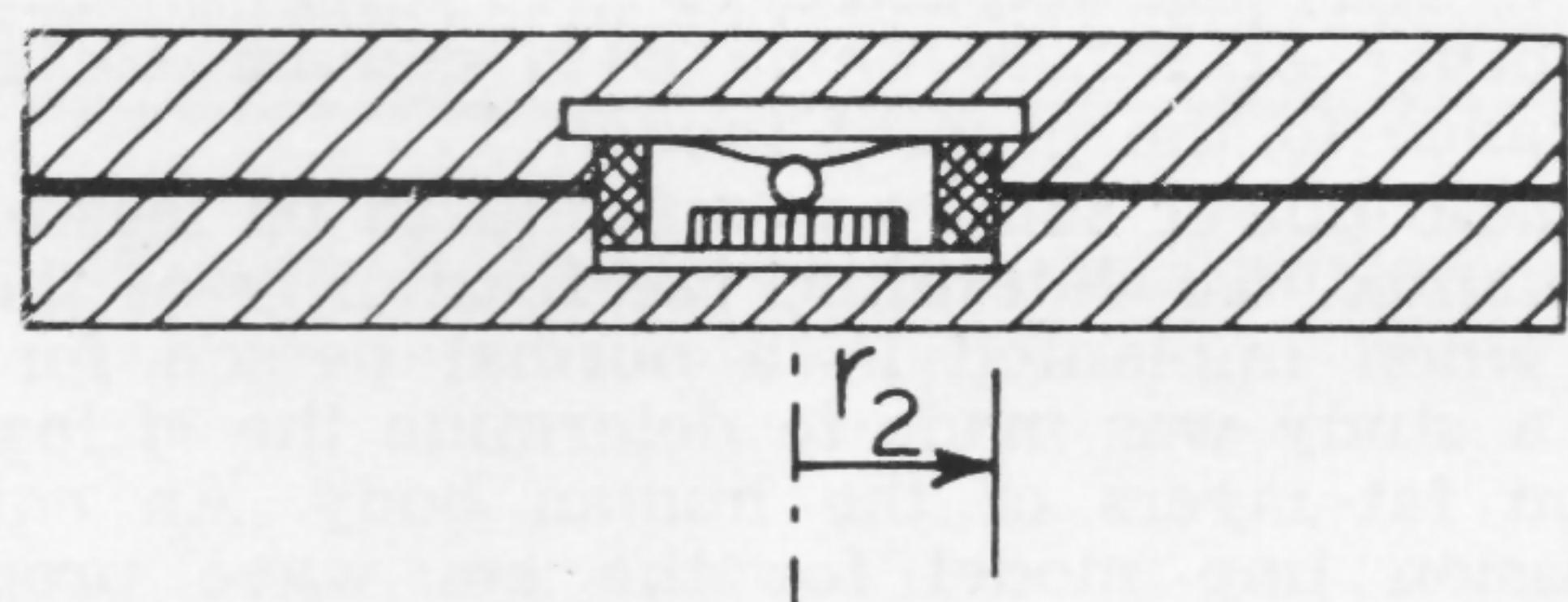


Figure 3—Minimum cavity produces lowest inductance possible, but does not allow for tuning or output coupling.

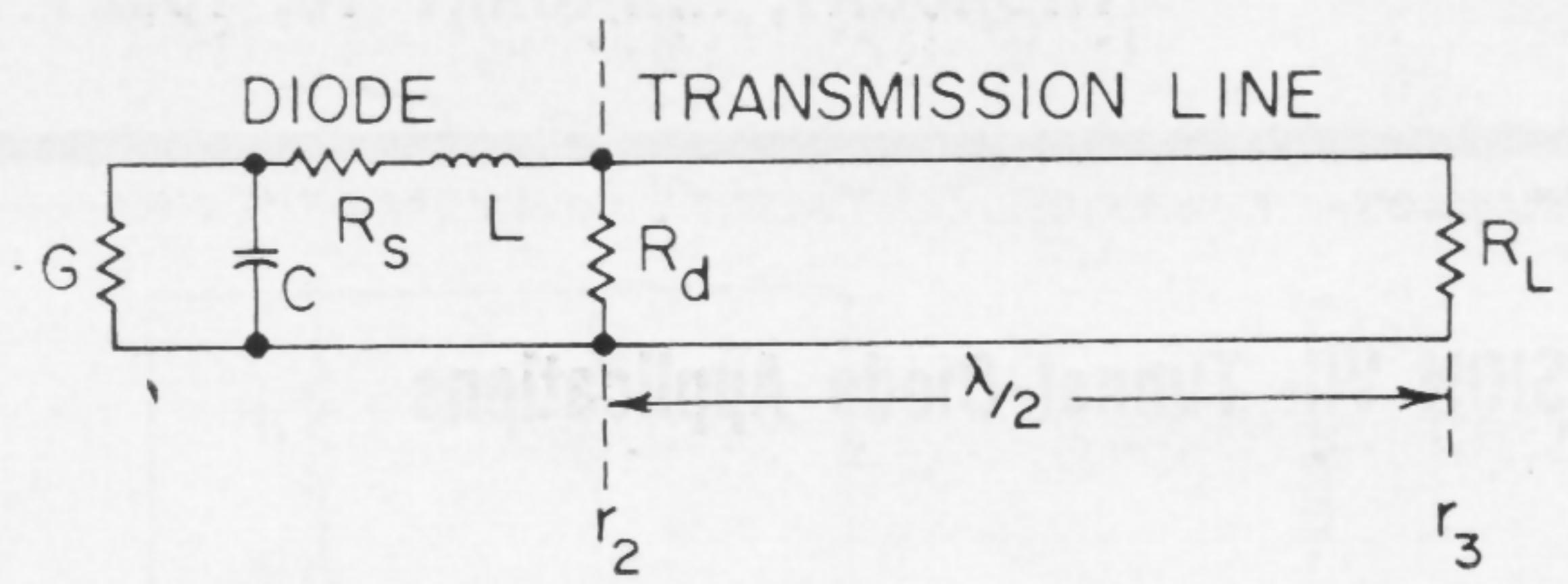


Figure 5—Total oscillator circuit. The damping resistance  $R_d$  serves to suppress the lower mode.

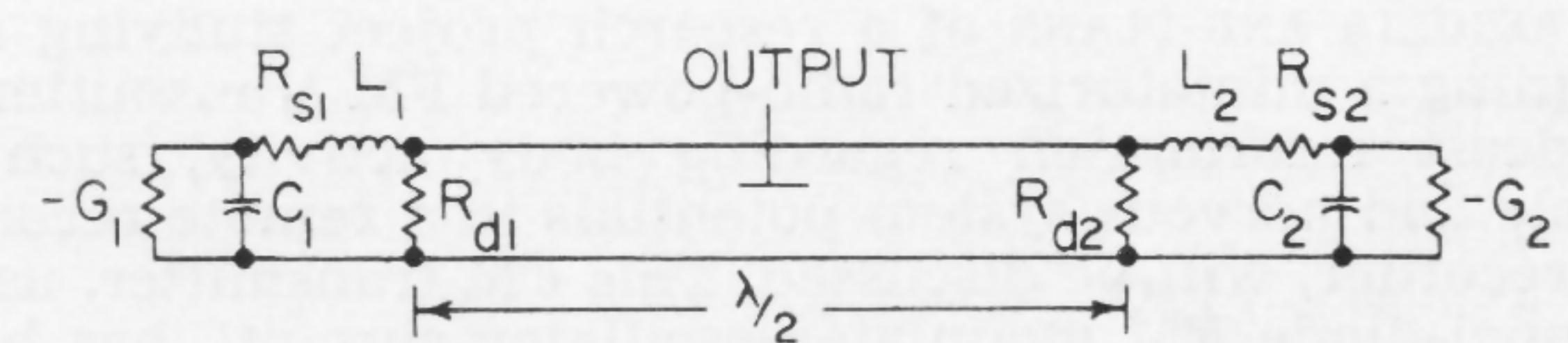


Figure 6—Schematic of distributed-diode oscillator using two diodes to double the power output.

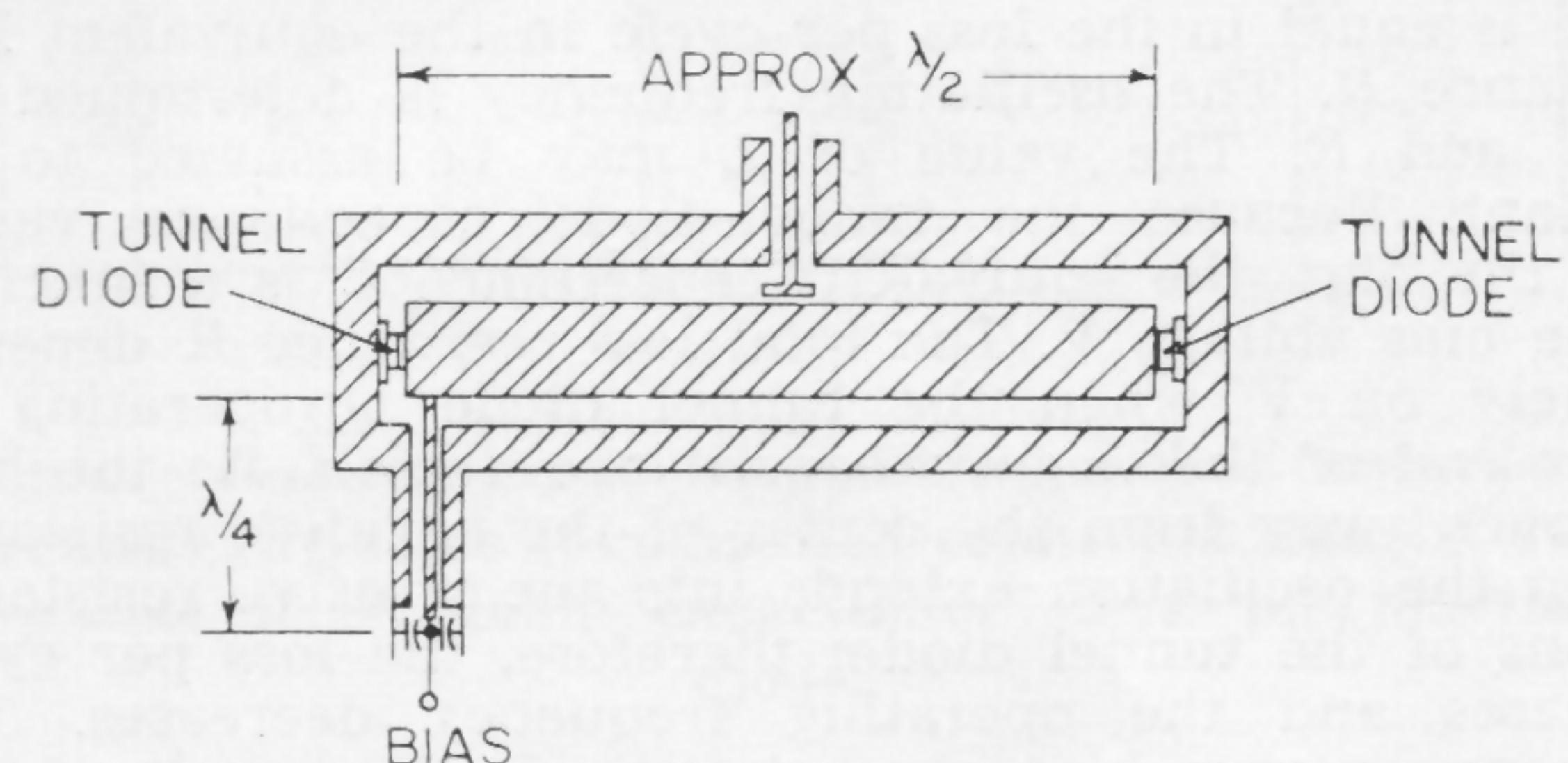


Figure 7—Cross-section of coaxial design of power doubling circuit.

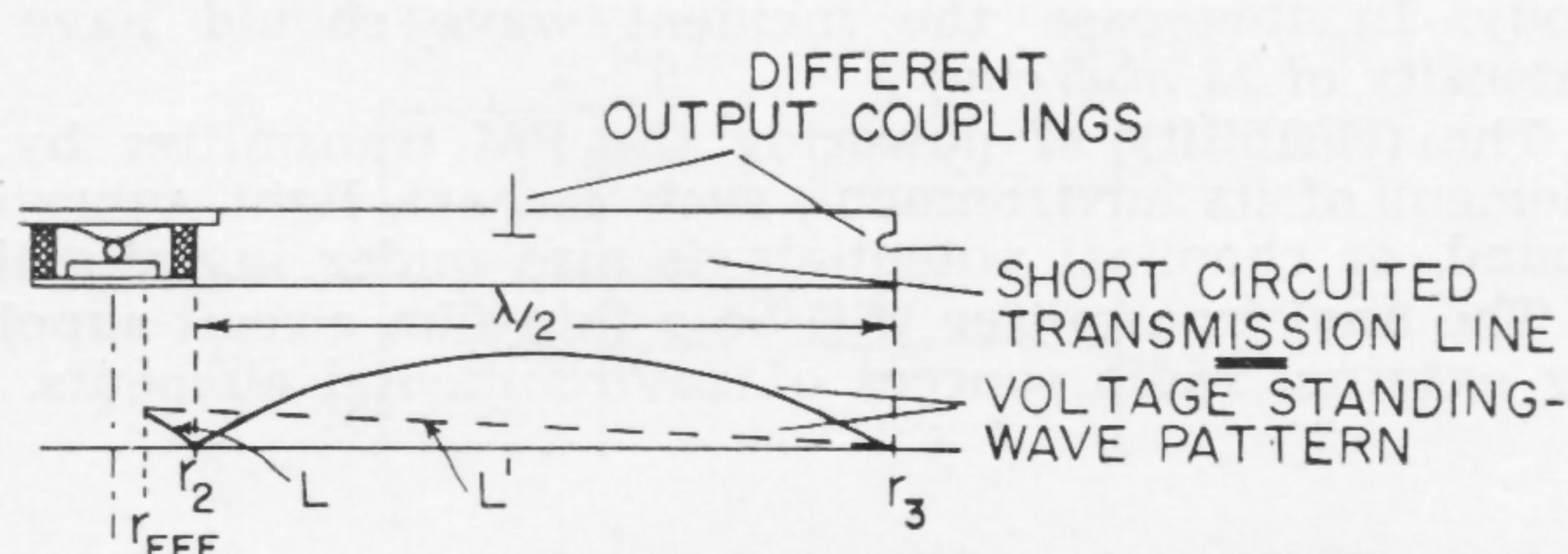


Figure 4—Standing-wave patterns for minimum cavity extended by  $\lambda/2$ . The lower mode with inductance  $L'$  is undesired.

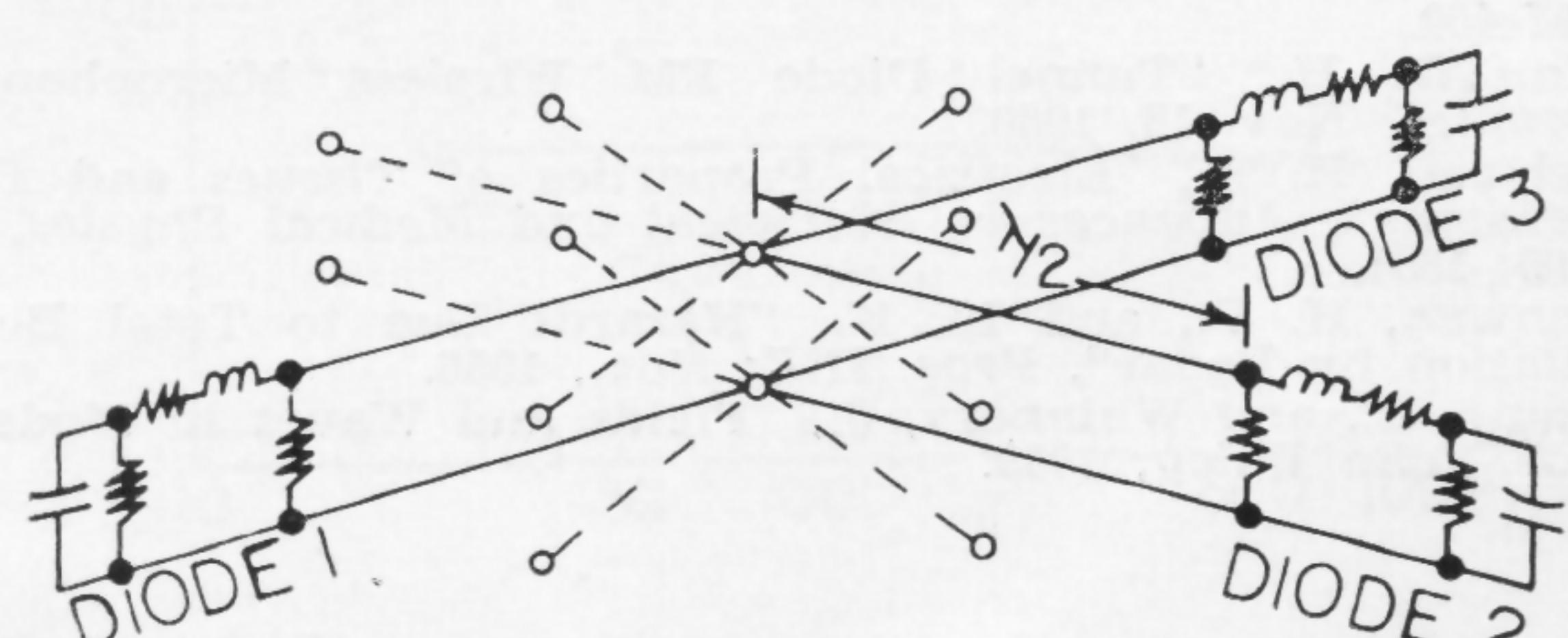


Figure 8—Distributed-diode oscillator for three or more diodes.

## SESSION VII: Tunnel Diode Applications

TA 7.3: A Tunnel-Diode FM Transmitter for Medical Research and Laboratory Telemetering<sup>‡</sup>

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Cleveland, O.

THE RESULTS AND PLANS of a research project studying and designing a miniaturized radio-powered FM transmitter to broadcast information regarding body activity, such as muscle and nervous system potentials to a remote receiver and recorder, will be discussed. This FM transmitter, using a tunnel-diode FM modulator-oscillator circuit<sup>1</sup>, has been found to eliminate the noise and disturbances presently created by the wire transmission techniques used in medical research and laboratory telemetering work.

The requirements of such a unit are: (1)—Small size and light weight; (2)—high sensitivity, low noise, and wide dynamic range; (3)—dc response and wide frequency range; (4)—high reliability and long life; and (5)—short broadcasting range.

The fundamental circuit of the tunnel-diode oscillator-modulator is shown in Figure 1a, where  $R'$  represents the radiation resistance and other rf losses in the circuit; the ac equivalent circuit of the oscillator is shown in Figure 1b. In the steady state the energy supplied per cycle by the negative resistance ( $-R_d$ ) of the tunnel diode is equal to the loss per cycle in the equivalent loss resistance  $R$ . The oscillating frequency is determined by  $L$ ,  $C$  and  $R$ . The value of  $L$  may be assumed to be constant. Because the tunnel-diode capacitance varies with the bias, the equivalent capacitance  $C$  is a function of the bias voltage  $V$ . The total loss resistance  $R$  depends strongly on  $V$  when the tunnel diode is operating at either end of the negative resistance region. As the bias  $V$  moves away from the center of the negative resistance region the oscillation extends into the positive resistance regions of the tunnel diode; therefore, the loss per cycle increases and the operating frequency decreases. The frequency versus bias characteristic is the result of the combined effect of  $R$  and  $C$ . It varies over a considerable range depending on the tunnel diode used in the oscillator. A set of typical characteristics is shown in c of Figure 1.

A frequency deviation,  $\left(\frac{df}{dV}\right)$ , from 50 to 200 kc/mv was

observed in the low bias region. This circuit provides a very sensitive means of generating FM radio waves and it satisfies the five requirements previously mentioned.

<sup>‡</sup> Research supported by a grant from the Office of Vocational Rehabilitation and the Engineering Design Center of Case Institute of Technology. The encouragement from the supporting organizations is acknowledged.

\* Model K-1.

\*\* M-400.

<sup>1</sup> Ko, W. H., "Tunnel Diode FM Wireless Microphone", *Electronics*; Nov. 18, 1960.

<sup>2</sup> Schwan, H. P., "Electrical Properties of Tissues and Cell Suspensions", *Advances in Biological and Medical Physics*, p. 147-209; 1957.

<sup>3</sup> Schwan, H. P., and Li, K., "Hazards Due to Total Body Irradiation by Radar", *Proc. IRE*; Nov., 1956.

<sup>4</sup> Ramo, S., and Whinnery, J., "Fields and Waves in Modern Radio", *John Wiley*; 1953.

The present model\*, diagrammed in Figure 2, uses a tunnel-diode-transistor combination circuit and is powered by a mercury battery\*\*. The transistor is used to obtain the bias and to increase the input impedance. The spiral inductance, which is also the radiating antenna, is constructed on one side of a printed circuit board with wire 3 mils in width. The other circuit elements are mounted on the reverse side of the board. The specifications and performance, measured in a shielded room, are:

Size:  $\frac{1}{2}'' \times \frac{1}{2}'' \times \frac{3}{8}''$ , including battery.

Weight: .1 ounce, including battery.

Current Drain: 1.2 ma.

Battery Life: 50 hours.

Power input: 1.6 mw.

Input Sensitivity: 5  $\mu$ v for 20-db signal-to-noise ratio at receiver output; receiver was 12' away from the transmitter.

Equivalent Noise of the System: 5  $\mu$ v at the input.

Dynamic Range of Input:  $2 \times 10^3$  (1  $\mu$ v to 2 mv).

Frequency Response: Flat from .01 cps to greater than 5 kc.

Input Impedance: 6,000 ohms.

Range: 5  $\mu$ v rf at 15'; with 4' electrode leads in air.

To increase the input impedance, several circuits are under investigation; two of these circuits are shown in Figure 4. They are expected to give an input impedance of the order of 100,000 ohms with comparable size and performance to the present model.

The radio power supply was found to be feasible when not implanted. To determine the feasibility of the power supply when implanted in a normal person for a long period, a study was made to determine the rf loss in the skin and fat layers of the human body. An equivalent transmission line model for the em wave propagating through body tissue layers, as shown in Figure 5, was used for the calculation. From the published data of conductivity and dielectric constant of body tissue at different frequencies<sup>2,3</sup>, the ratio of the power available at the fat muscle interface ( $P_{+3}$ ) to the power incident on the skin tissue ( $P$ ), as well as the ratio of the power absorbed by the skin and fat layers ( $P_L$ ) to the available power ( $P_{+3}$ ) can be calculated<sup>4</sup> as illustrated in Figure 6. If the power required is to be supplied by an external radio wave at 240 Mc or lower frequencies, the loss in the tissues will be equal to or less than the power available. Assuming the pickup efficiency to be 33% and the pickup antenna effective area to be  $1 \text{ cm}^2$ , the maximum loss in the tissues will be about  $4.7 \text{ mw/cm}^2$ , which is less than half of the safe limit of radio absorption of the human body. In this case the incident wave should have an intensity of  $15 \text{ mw/cm}^2$ .

The feasibility of powering the FM transmitter by an element of its environment, such as heat, light, vibration, sound, or chemical potentials, is also under investigation.

The final transmitter will be a thin-film circuit supplied by external radio sources of environmental elements.

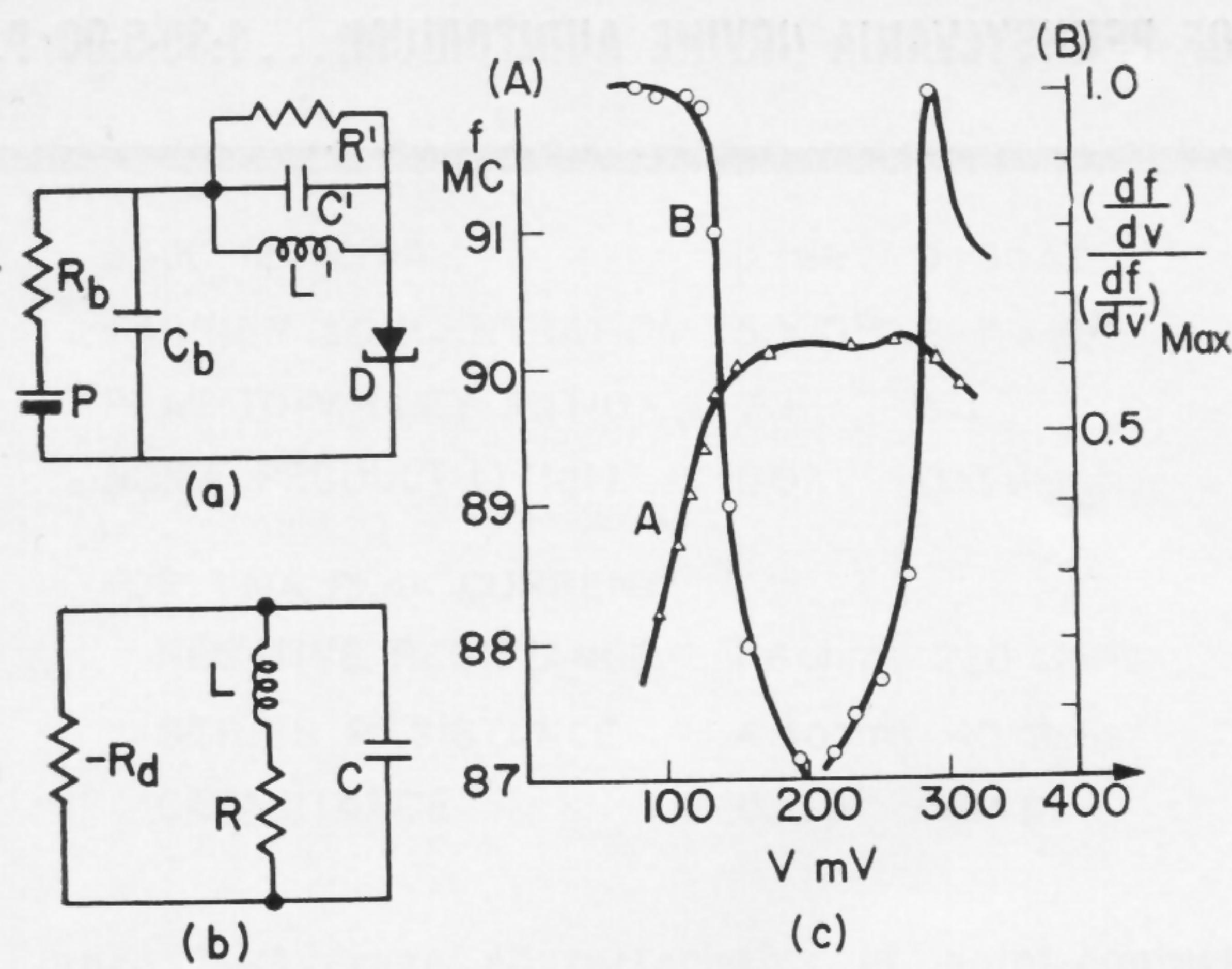


Figure 1—Tunnel-diode FM oscillator-modulator: (a)—Circuit; (b)—ac equivalent circuit; (c)—frequency and frequency deviation versus bias characteristics.

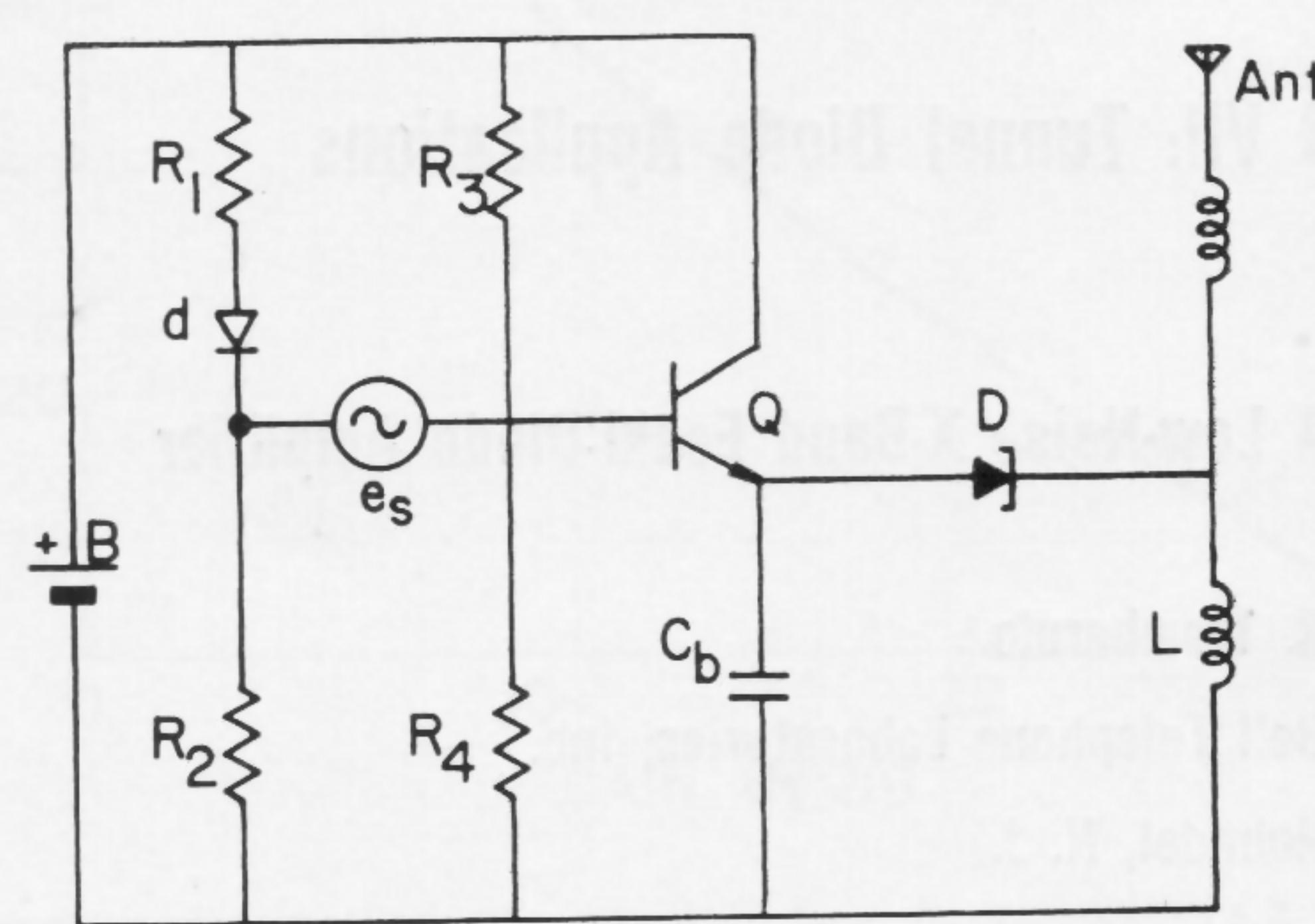


Figure 2—Circuit diagram of FM transmitter.

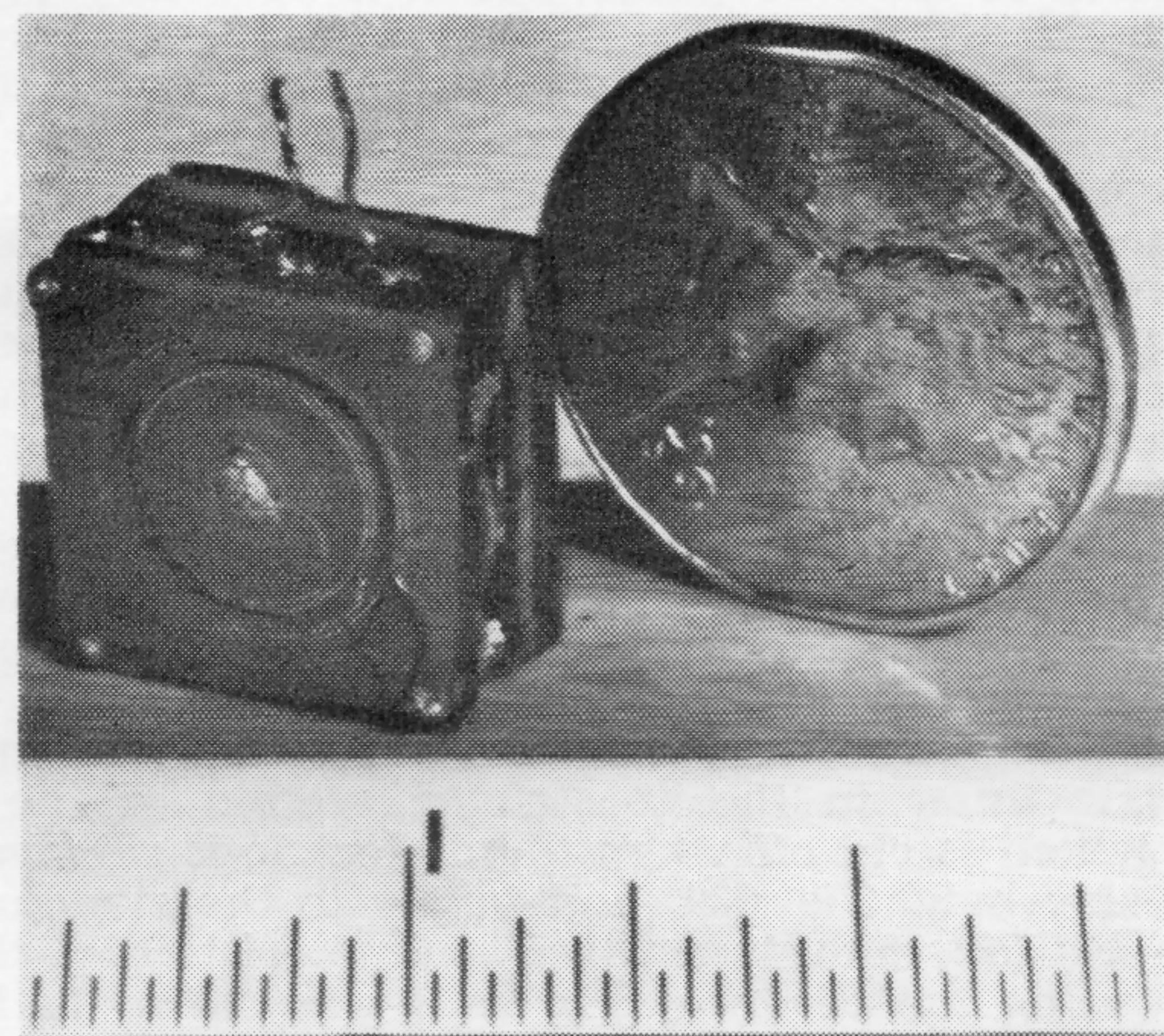


Figure 3—Photo of the transmitter.

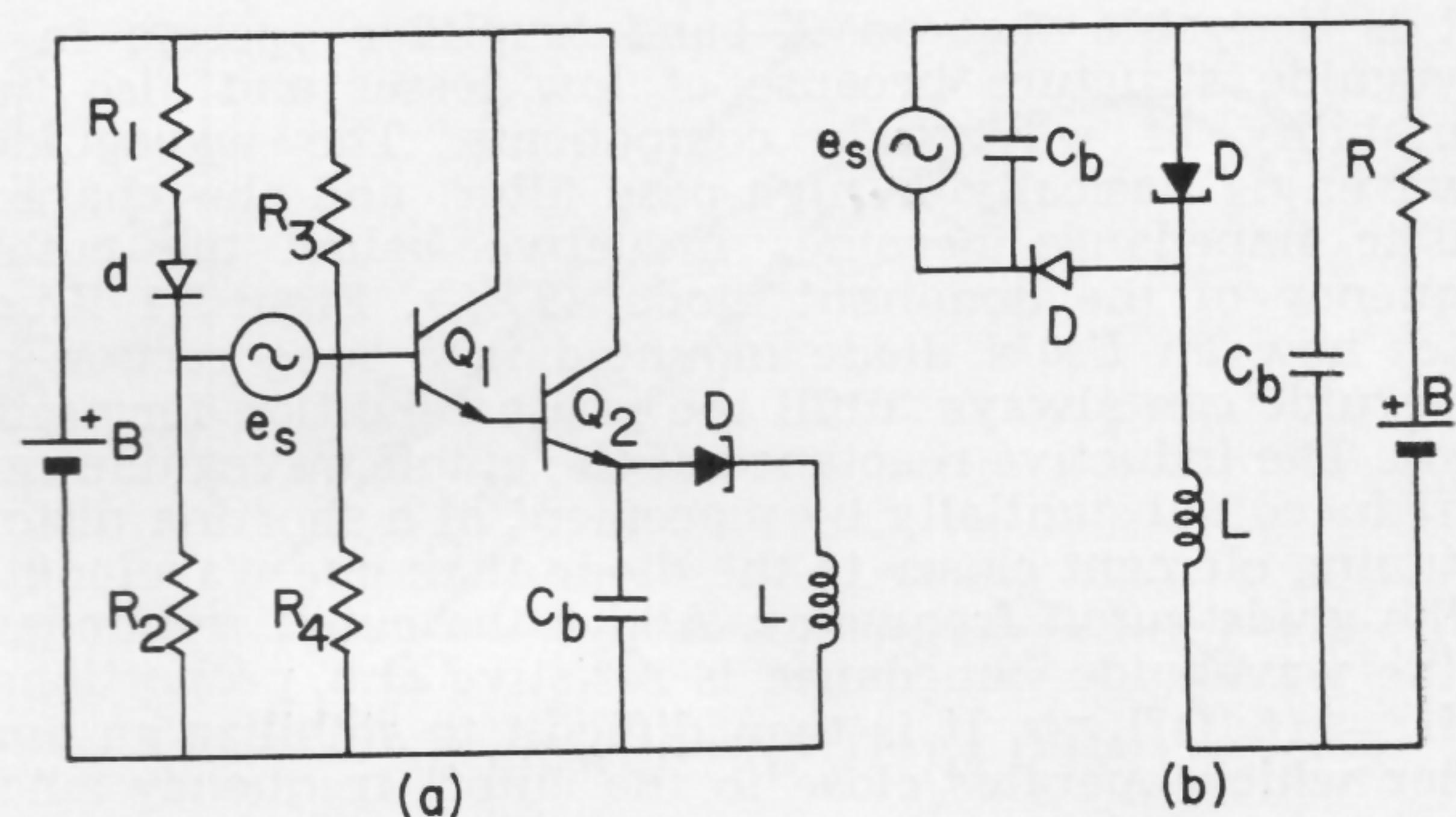


Figure 4—High-input impedance FM transmitter circuits: (a)—Use of compound-connected transistors; (b)—use of variable capacitance of a pn junction diode.

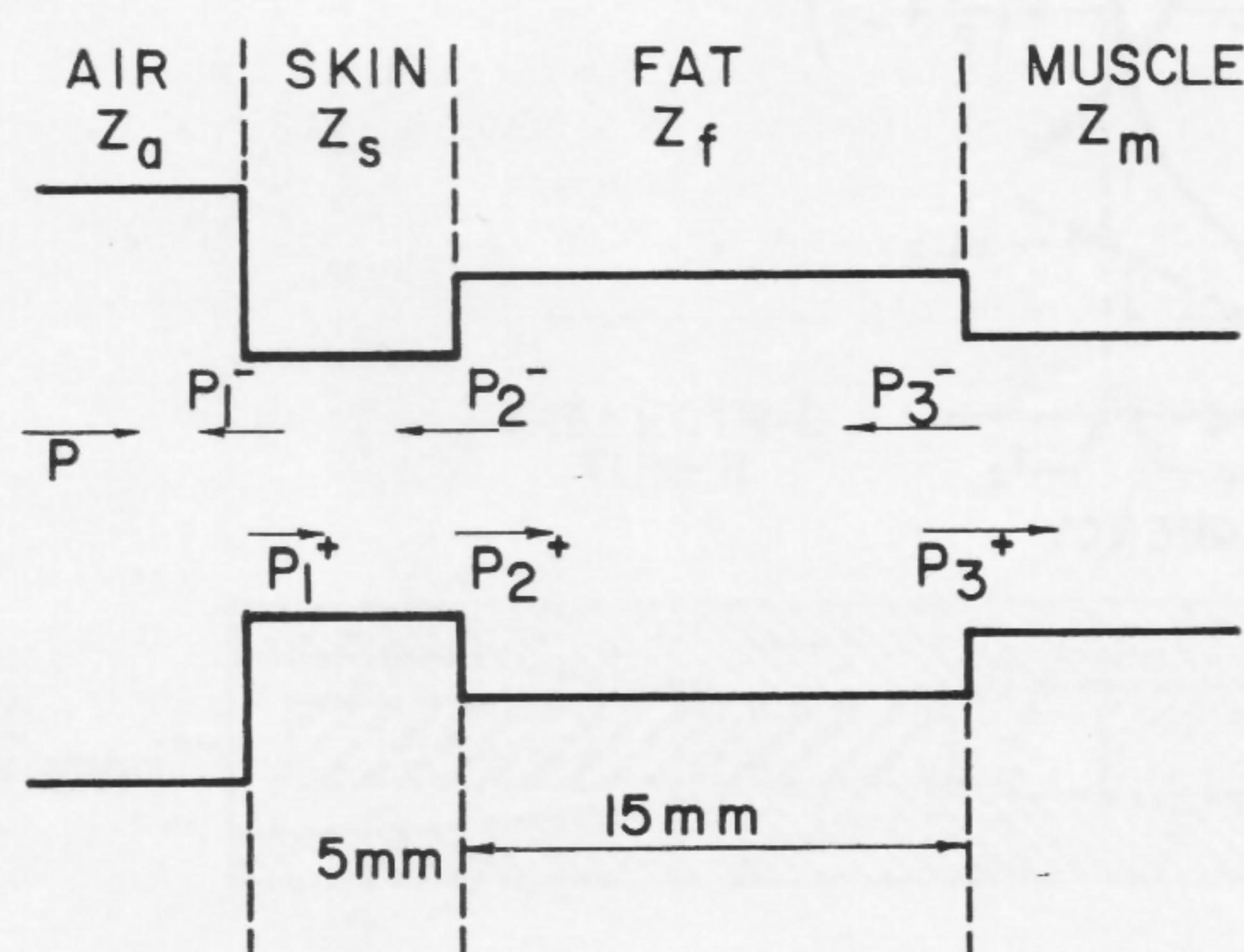


Figure 5—Transmission line model of body skin and fat layers.

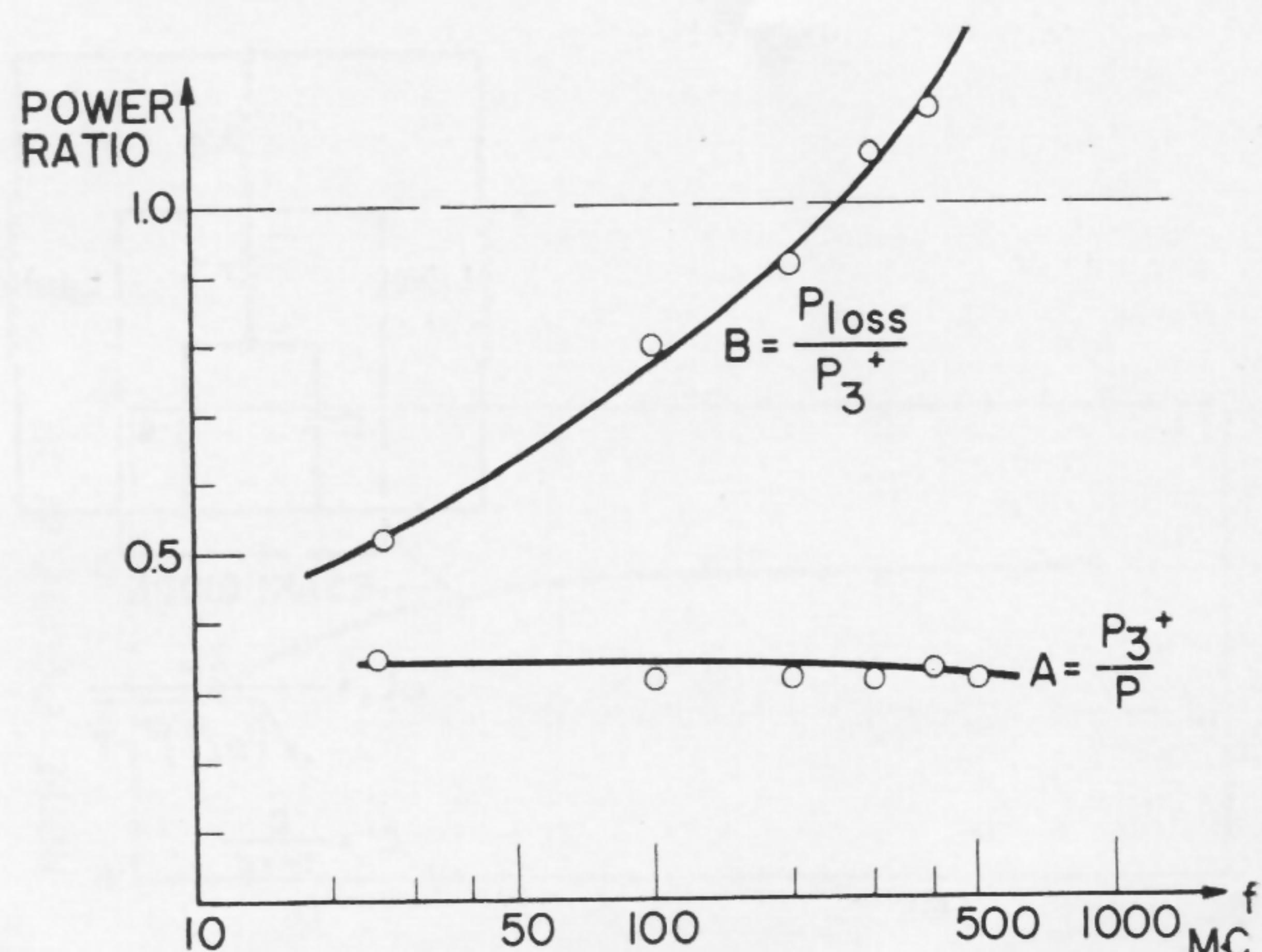


Figure 6—Power ratios versus frequency diagram. A is the ratio of the power available at the fat-muscle interface to the incident power. B is the ratio of the power loss in the layers to the power available at the fat-muscle interface.

## SESSION VII: Tunnel Diode Applications

## TA 7.4: A Low-Noise X-Band Esaki-Diode Amplifier

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Bell Telephone Laboratories, Inc.  
Holmdel, N. J.

ESAKI-DIODE microwave amplifiers are attractive because of their simplicity, compactness and low-power requirements. A cavity amplifier operating in the X band has been reported<sup>1</sup>, but its frequency could not be readily tuned, and it was difficult to couple the external circuit strongly enough to the cavity structure. This paper will describe a waveguide amplifier, whose gain and operating frequency can be adjusted more easily, and point out some of the problems which arise in the design of such an amplifier.

It is desirable that an X-band amplifier operate in a waveguide structure because of low losses and also the availability of waveguide components. The waveguide, however, is basically a high-pass filter, and the characteristic impedance becomes inductive below the cutoff frequency of the dominant mode ( $TE_{10}$ ). Figure 1 illustrates how an Esaki diode mounted in a long section of waveguide can always fulfill the phase condition for oscillation. The inductive reactance of the cutoff waveguide can be reduced substantially by placement of a shorting piston or tuning element closer to the diode than one wavelength at the guide cutoff frequency. Above the cutoff frequency,  $f_0$ , the waveguide impedance is resistive and proportional to  $[1 - (f_0/f)^2]^{-1/2}$ . It is then difficult to stabilize an amplifier which operates close to the cutoff frequency since the characteristic impedance is large.

<sup>1</sup> Trambarulo, R., "Esaki Diode Amplifiers at 7, 11, and 27 kMc," Proc. IRE, p. 2022; December, 1960.

Mounting a diode across the waveguide introduces an additional inductance ( $L_2$  of Figure 1) in series with the diode. Both this inductance and the characteristic impedance of the waveguide are proportional to the narrow dimension of the waveguide, and it is necessary to reduce this dimension in order to stabilize the diode.

At present, point-contact Esaki diodes are best suited to X-band amplifiers because of their low capacitances. Average characteristics for experimental germanium and gallium arsenide diodes are given in Figure 2. Germanium diodes are preferred for low-noise operation; however, higher output power at saturation is obtainable from gallium arsenide units. Figure 3 shows the current, negative conductance, and noise product,  $I/|g|$ , as a function of bias voltage for a typical germanium unit.

The experimental amplifier is a circulator-coupled reflection type. The circulator, designed to operate between 10.7 and 11.7 kMc, determined the frequency range of the amplifier. Figure 4 shows the broad wall view of the amplifier structure. The gain is adjusted by motion of the dielectric tuner in the constricted section of the waveguide which is cut off when the dielectric is removed. The waveguide height is .020" and tapers to the standard .400" at the output. Some operating characteristics of the amplifier using the diode of Figure 3 are shown in Figures 5 to 7. One of the chief difficulties encountered with this circuit is the tendency to oscillate at frequencies above the desired band. These oscillations can usually be suppressed by adjustment of the dielectric tuner and piston.

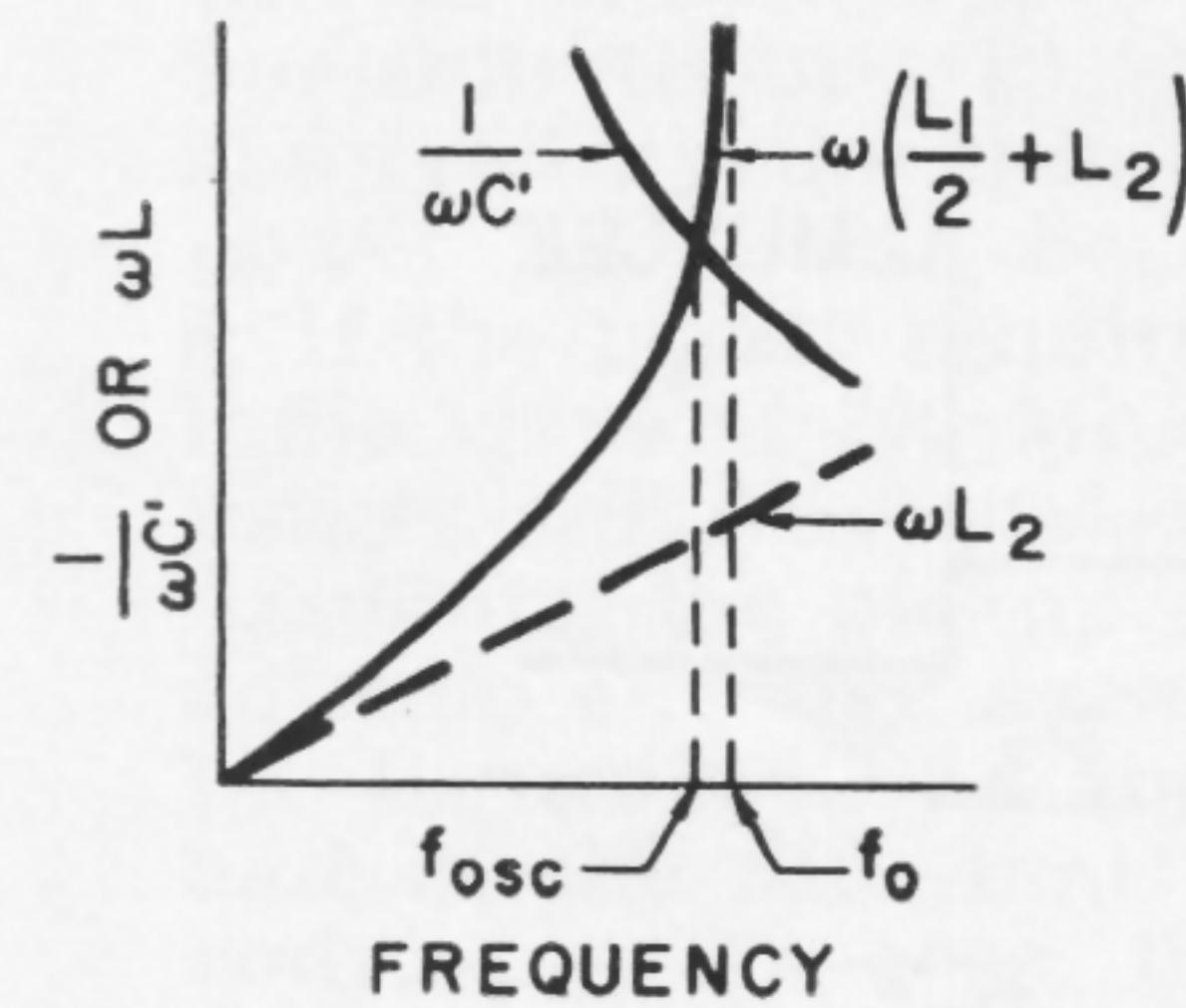
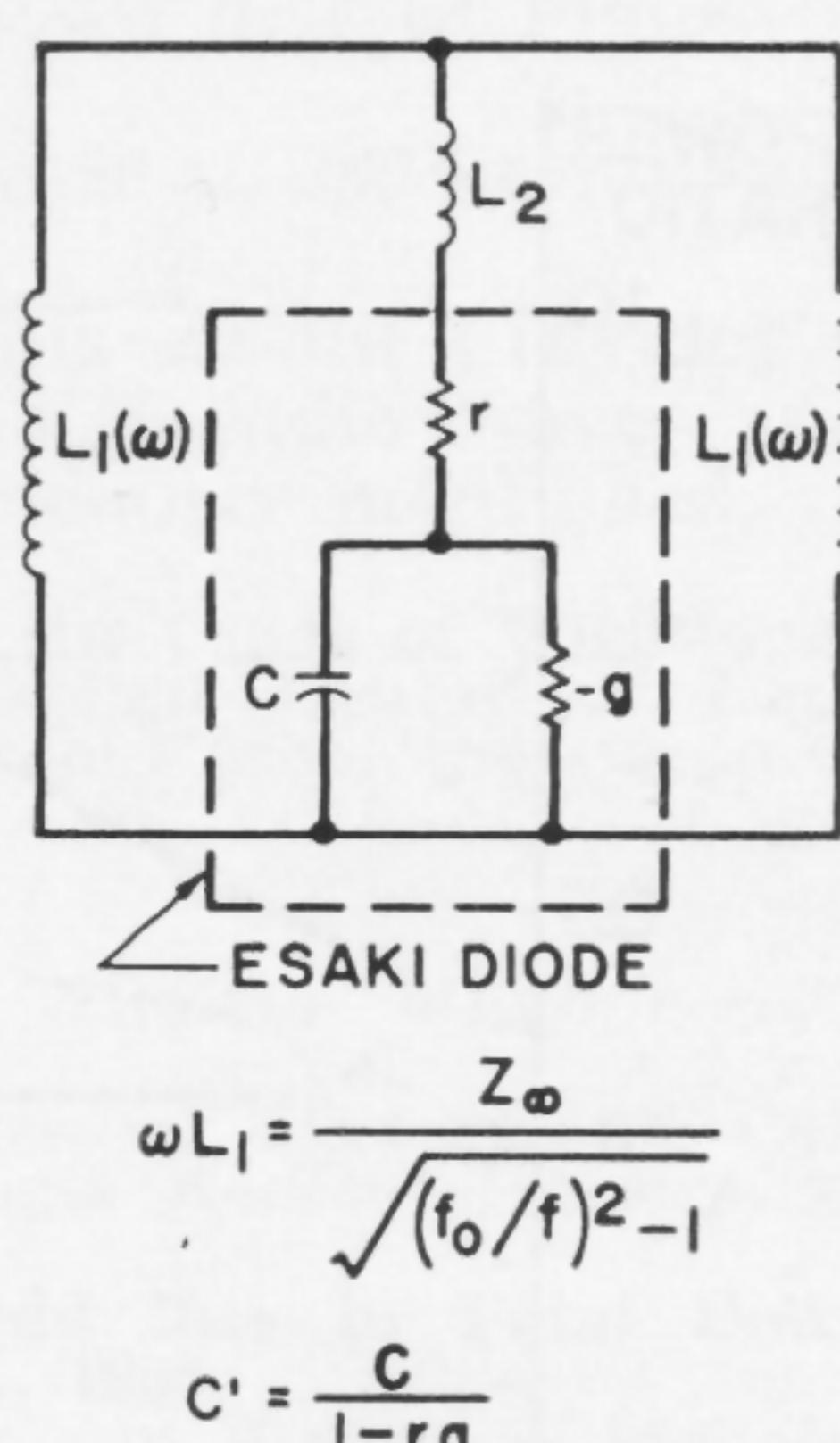


Figure 1—Equivalent circuit for an *Esaki* diode in a long length of waveguide below the cutoff frequency,  $f_0$ .  $L_1$  is the inductance equivalent to the waveguide on either side of the diode.  $L_2$  is the lead inductance. The circuit can oscillate at  $f_{osc}$ . Waveguide losses near  $f_0$  have been neglected.

BASE MATERIAL	p-Ge	p-GaAs
CARRIER CONCENTRATION	$5 \times 10^{19}$	$2-7 \times 10^{19}$
PEAK-TO-VALLEY RATIO	7:1	5:1
NOISE PRODUCT ( $I/I_{g1}$ )	0.07V	0.13V
FOR 1-MA PEAK CURRENT:		
NEGATIVE RESISTANCE	116 ohms	220 ohms
SERIES RESISTANCE	4.5 ohms	40 ohms
CAPACITANCE	0.13 pf	0.04 pf

Figure 2—Average characteristics of point-contact diodes used in X-band amplifier circuits.

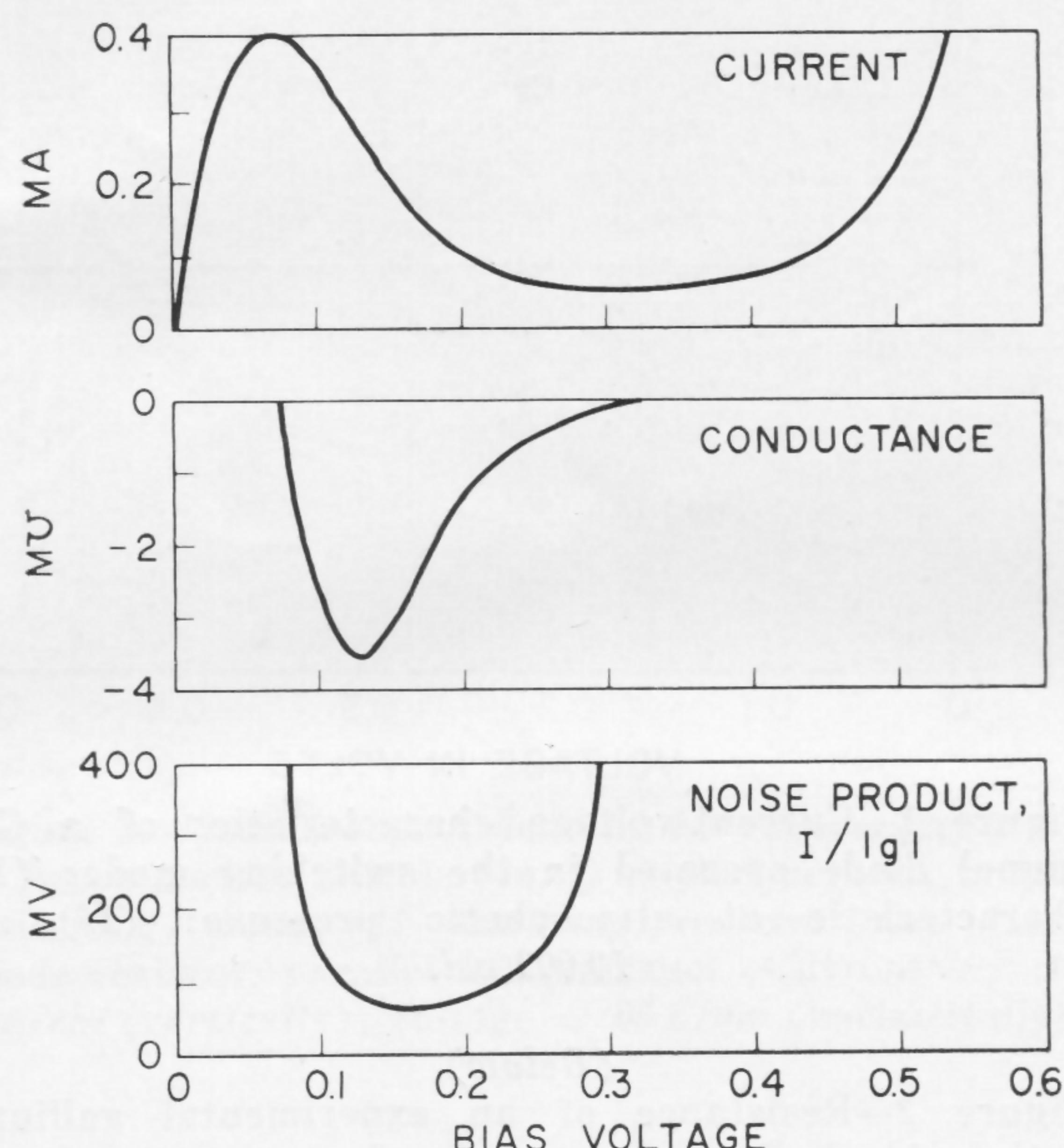


Figure 3—Current, negative conductance and noise product versus bias voltage for a germanium diode.

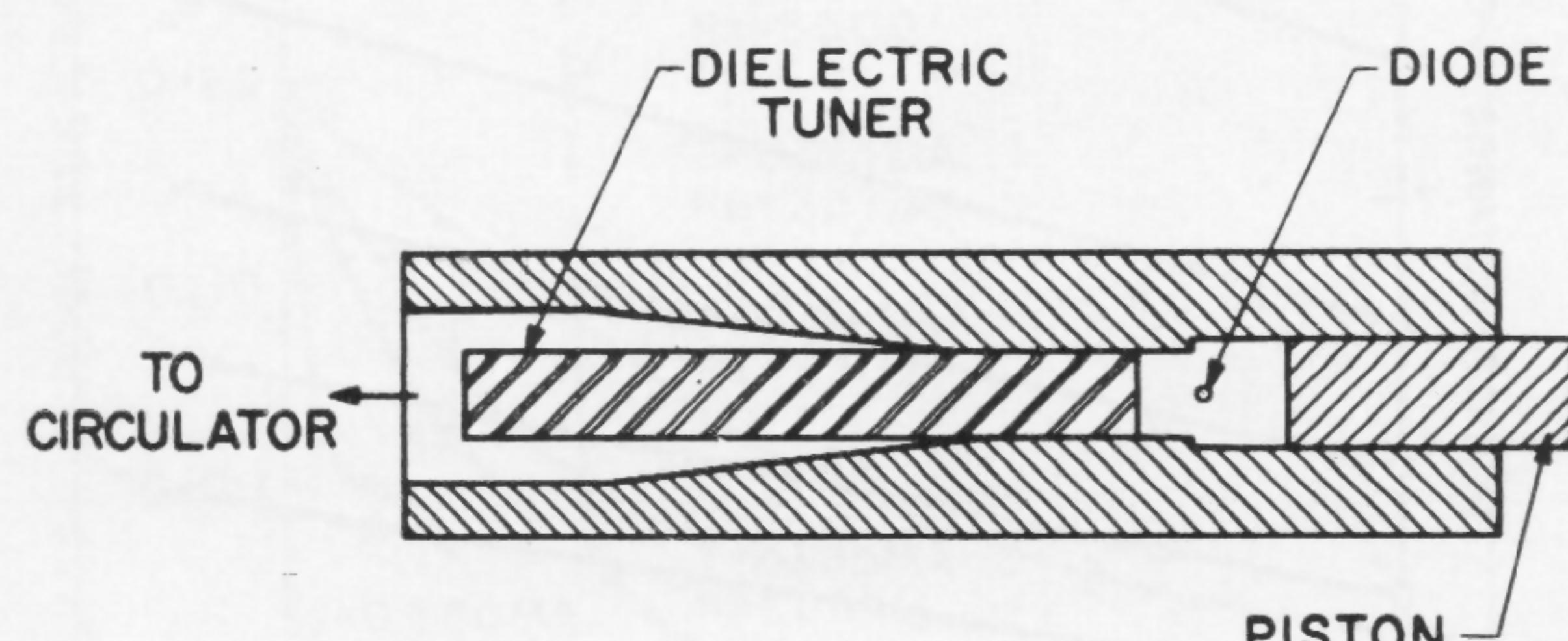


Figure 4—Broad-wall view of an X-band amplifier structure. The narrow dimension of the waveguide is reduced in the vicinity of the dielectric tuner and diode cavity.

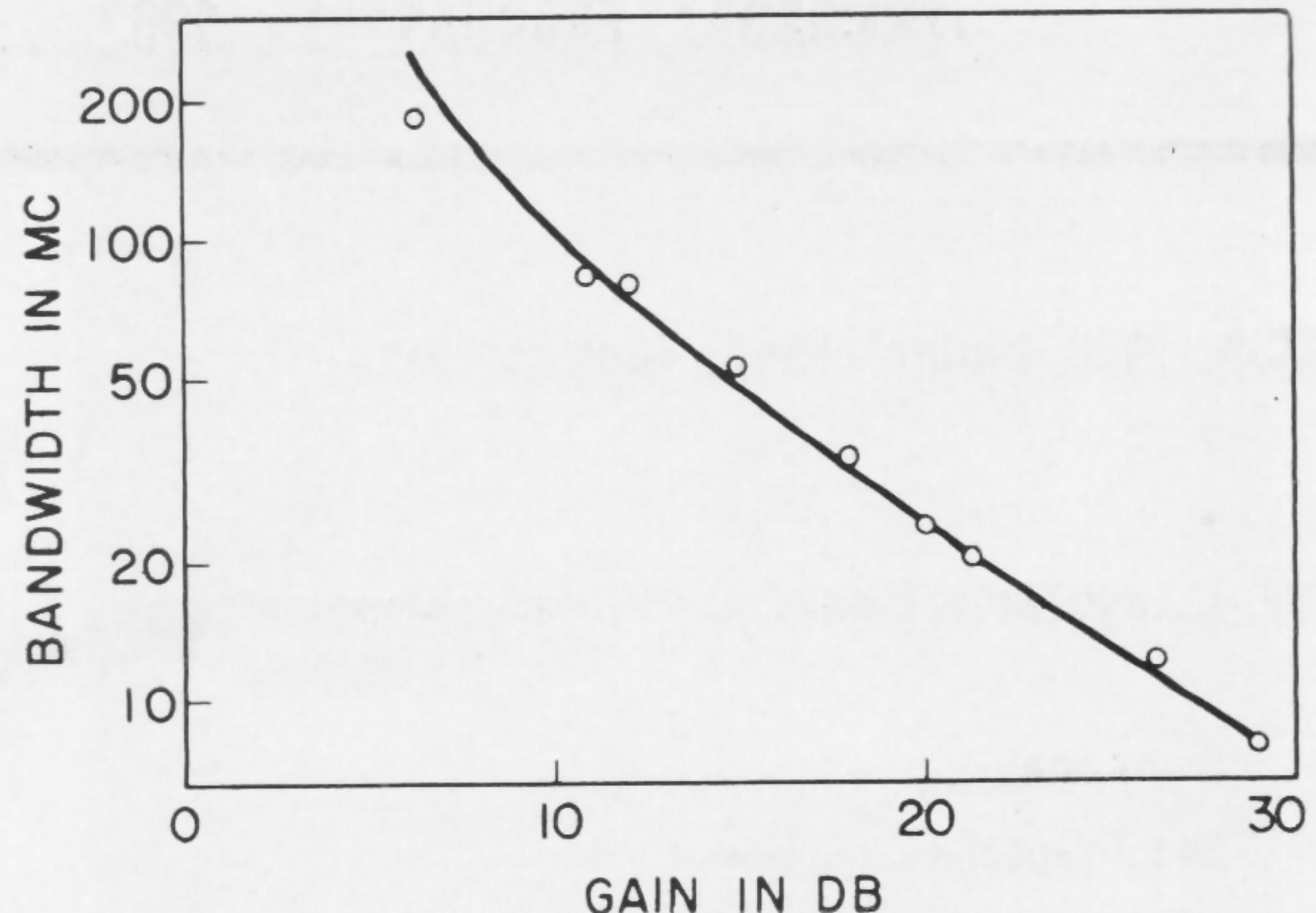


Figure 5—Bandwidth,  $\Delta f$ , versus gain at 11.5 kMc with the diode of Figure 3.

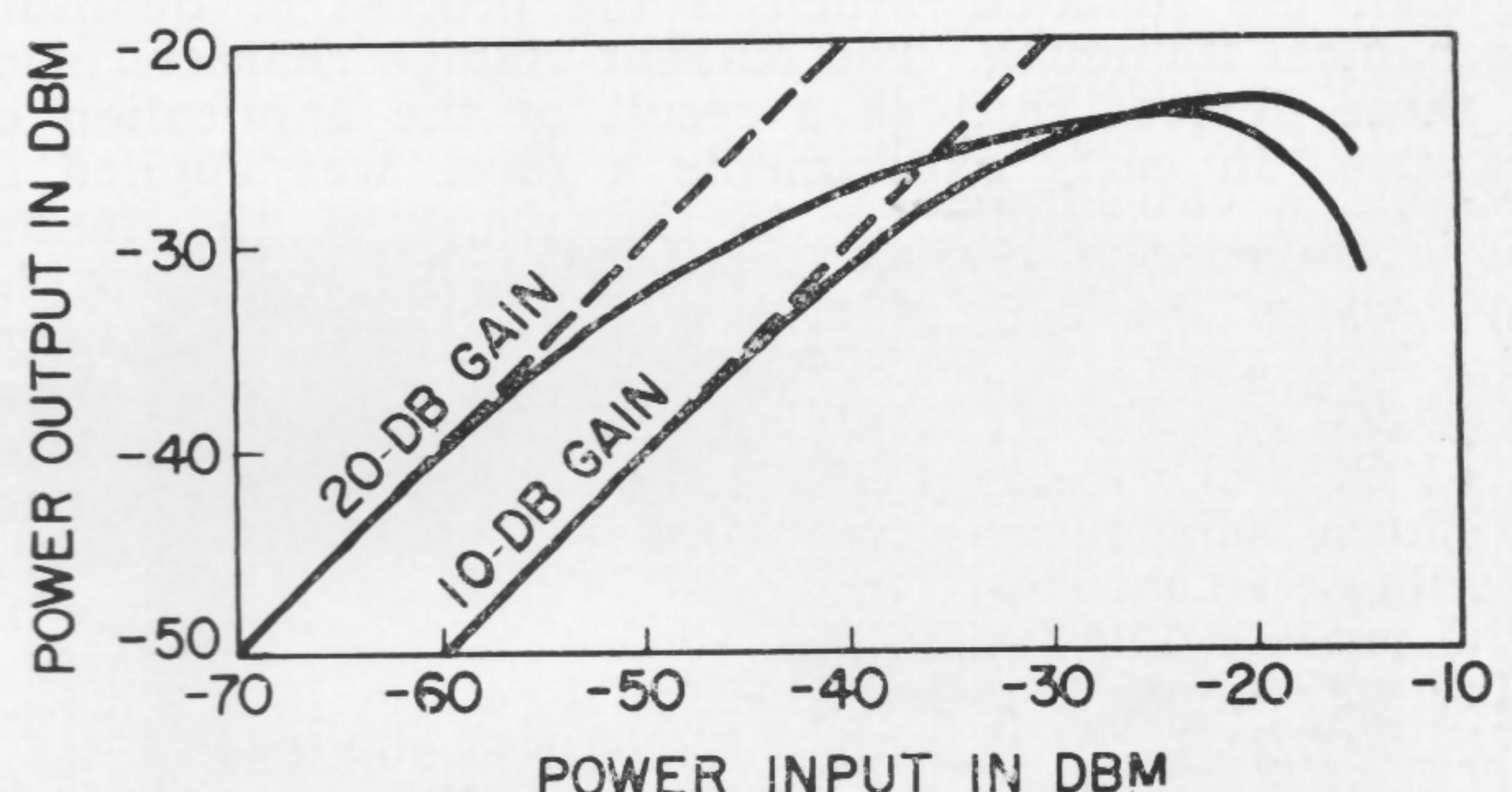


Figure 6—Saturation characteristic of the amplifier with the diode of Figure 3.

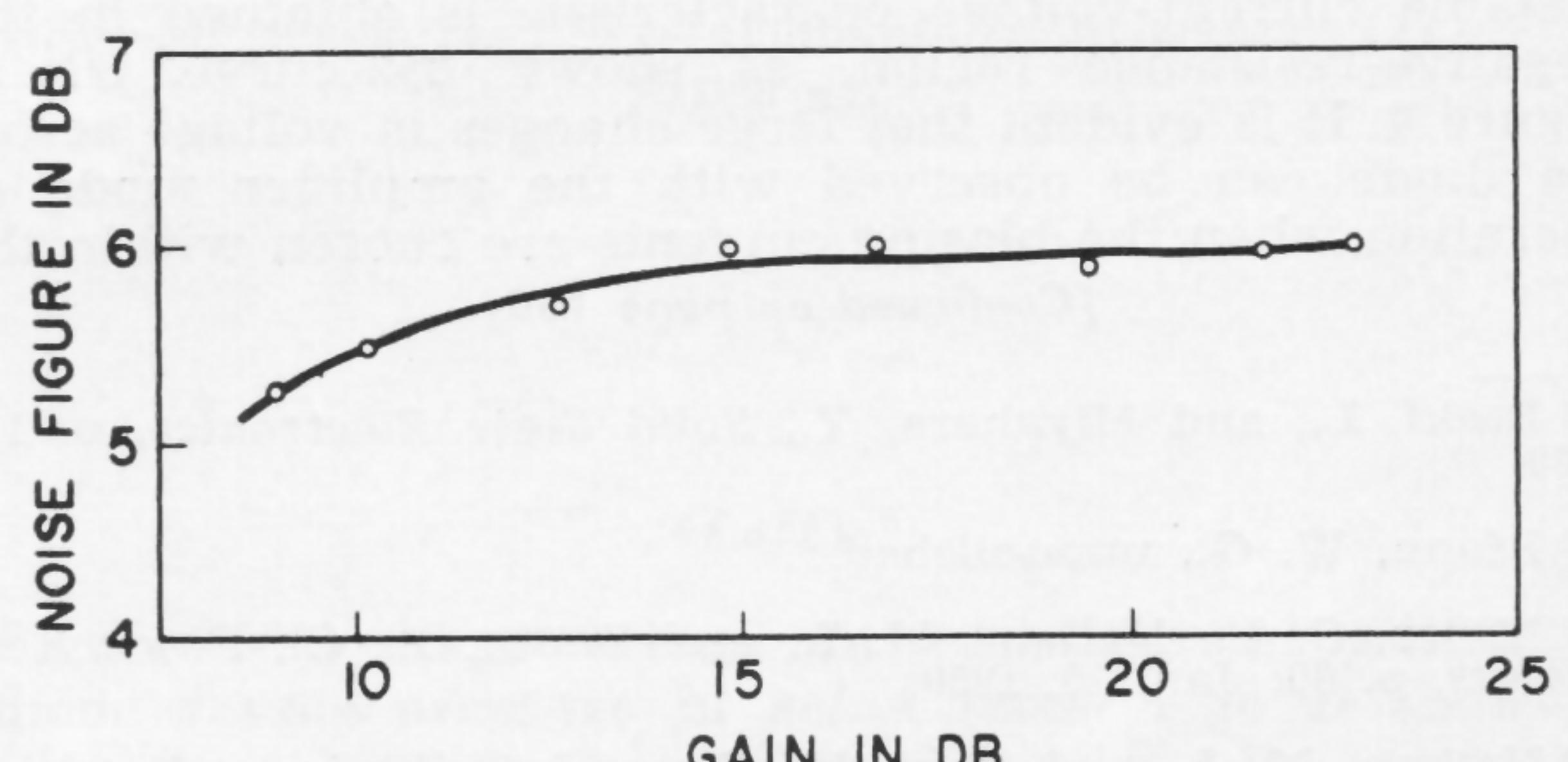


Figure 7—Noise figure versus gain for the diode of Figure 3 at 11.5 kMc.

## SESSION VII: Tunnel Diode Applications

## TA 7.5: Sensitive Tunnel-Diode Pressure Transducers

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THE PURPOSE of this paper will be to show that sensitive pressure measurements can be made with tunnel diodes using circuit control. These devices are among the most sensitive pressure transducers known, with the additional feature that they respond to static as well as dynamic pressures. They are also attractive because of very small size.

Tunnel diodes are narrow *pn* junctions. Their name is derived from the mechanism of conduction of electricity through the junction which is the process of quantum mechanical tunneling. The current-voltage characteristics of these devices shift as a result of the application of pressure. In early experiments a force was applied in a direction perpendicular to the plane of the tunnel junction by means of a gramophone needle<sup>1</sup>. A shift in the *I-V* characteristics was observed. Various mechanical magnification schemes can be used to utilize the above effect in pressure transducer applications. It was later found that the current-voltage characteristics of tunnel diodes are also sensitive to hydrostatic pressure variations<sup>2,3,4,5</sup>. Both of these effects are due to a change in the thickness of the *pn* junction through which tunneling takes place, and in a greater measure to a change in the energy gap of the semiconductor material. Regardless of what method is used in applying pressure to the junction, the sensitivity of a pressure transducer can be increased by the following method of circuit control. With a tunnel diode in the switching mode, let us assume that a Ge tunnel diode is biased at point *A* of its *I-V* characteristic (I) as shown in Figure 1. If the current is kept at a constant value *I<sub>b</sub>*, while the pressure is increased from atmospheric to 10,000 psi, the operating point will shift from *A* to *B*. The voltage change  $\Delta V_{AB}$  is then a measure of the increment in pressure. Similarly, constant voltage biasing can be used. Figure 2 shows results obtained on a gallium antimonide tunnel diode biased in this manner.

Now let us analyze the tunnel diode in the amplifier mode. A circuit used to study the effect of pressure on the characteristics of tunnel diodes is shown in Figure 3. The shunt resistor *R<sub>s</sub>* satisfies the stability conditions for operation of the diode in the amplifier mode. In this case, a stable current-voltage characteristic is obtained in the negative-resistance region, as shown by curve III in Figure 4. It is evident that large changes in voltage across the diode can be observed with the amplifier mode of operation when the biasing currents are chosen within the

[Continued on page 106]

<sup>1</sup> Esaki, L., and Miyahara, Y., *Solid State Electronics*, p. 13; 1960.

<sup>2</sup> Pfann, W. G., unpublished.

<sup>3</sup> Miller, S. L., Nathan, M. I., and Smith, A. C., *Phys. Rev. Letters*, p. 60; Jan. 15, 1960.

<sup>4</sup> Nathan, M. I., and Paul, W., *Proc. Int. Conf. on Semicon. Phys.*; Prague, 1960.

<sup>5</sup> Sikorski, M. E., and Andreatch, P., *Rev. Sci. Instr.*; to be published.

<sup>6</sup> The use of the switching characteristic as an alarm device was first considered by W. G. Pfann of Bell Telephone Laboratories.

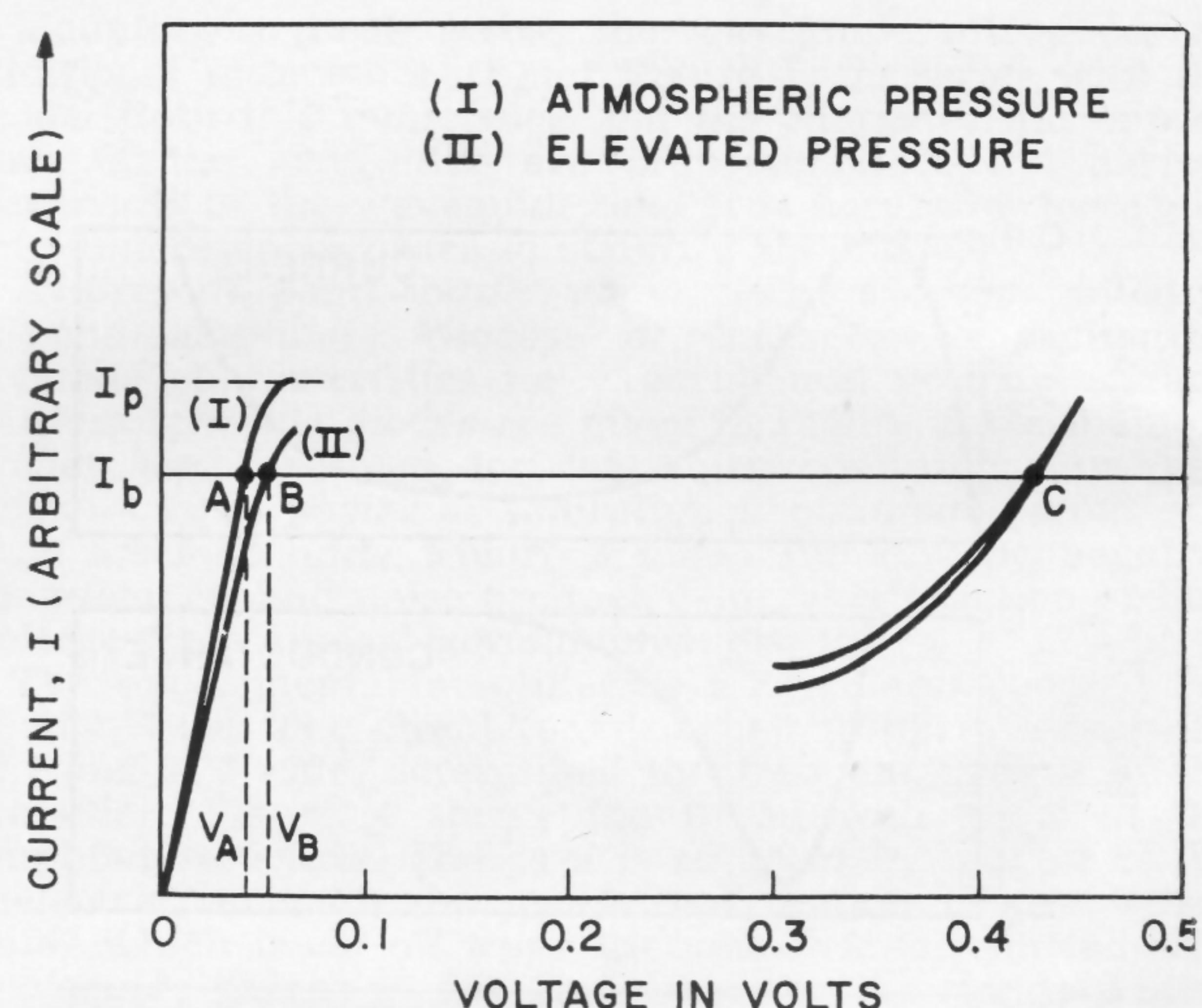
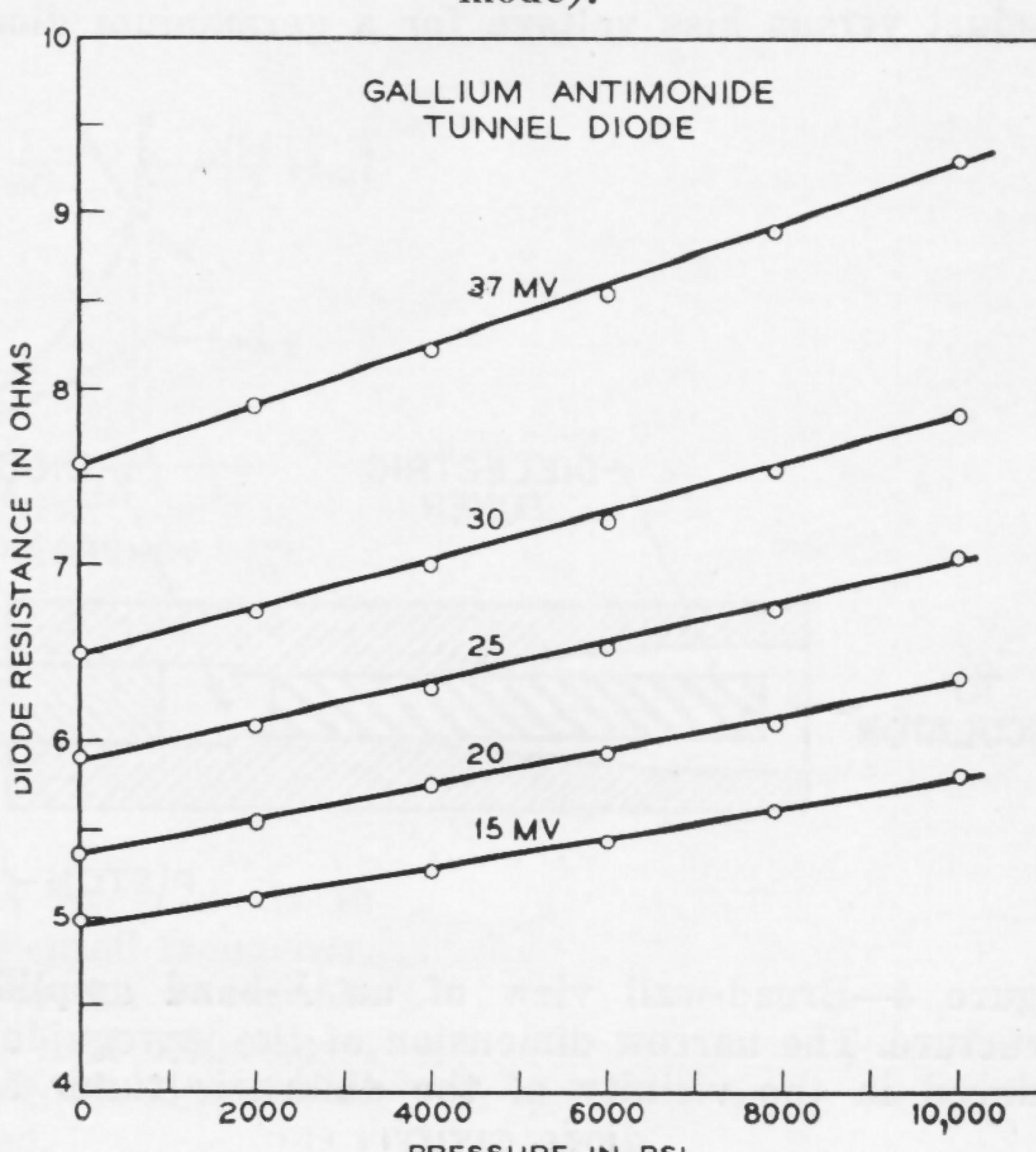


Figure 1—Current-voltage characteristics of a Ge tunnel diode operated in the switching mode: (I) characteristic at atmospheric pressure; (II) at 10,000 psi.

(Below)

Figure 2—Resistance of an experimental gallium antimonide diode versus pressure for constant-voltage operation in the positive-resistance region (switching mode).



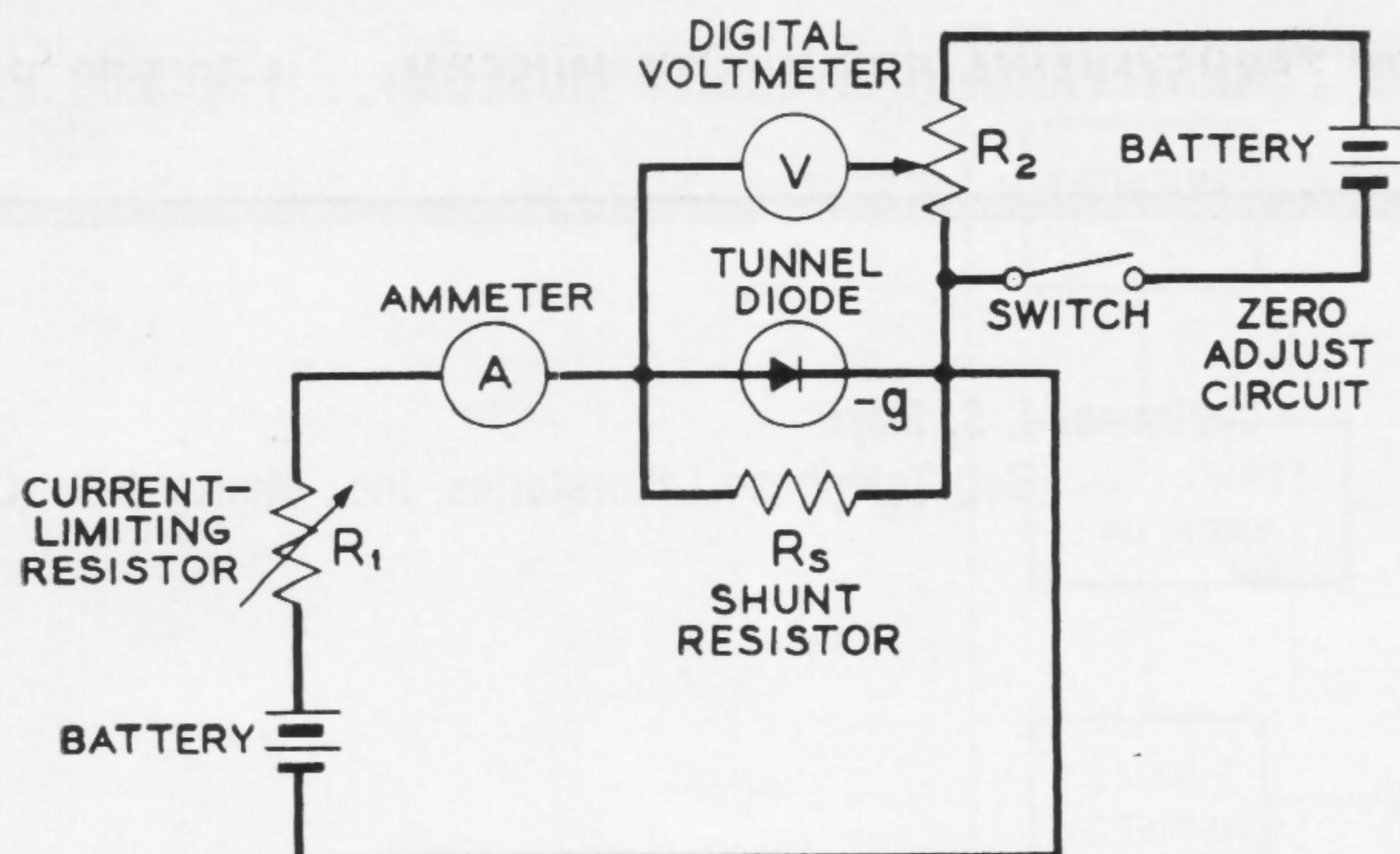


Figure 3—Circuit used to study the effect of pressure on the electrical characteristics of tunnel diodes.

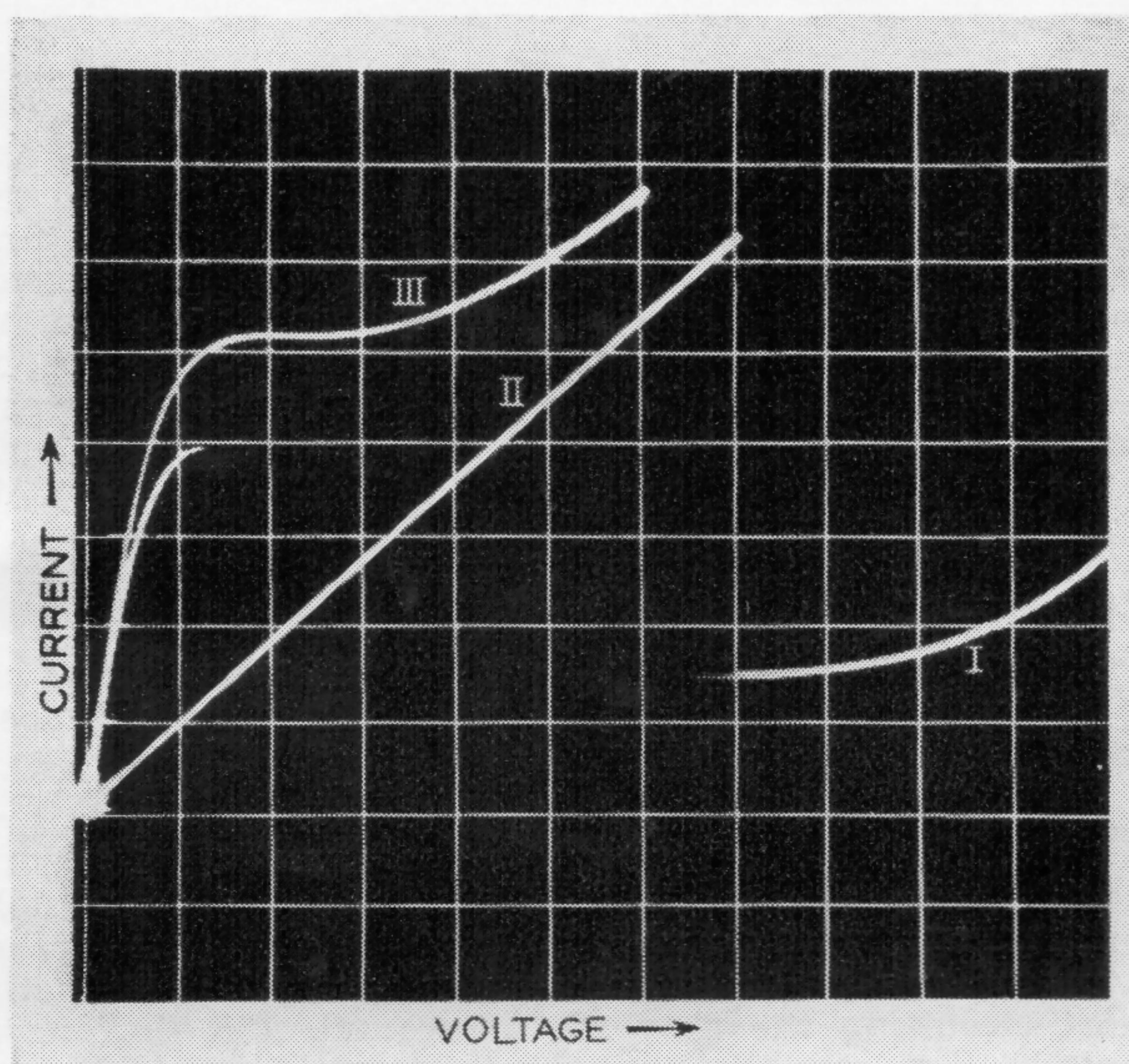


Figure 4—Oscilloscope traces of  $I$ - $V$  characteristics: I—experimental silicon tunnel diode operated in the switching mode; II—shunting resistor  $R_s$ ; III—diode-resistor parallel combination. Current = .17 ma/cm (vertically); voltage = .05 v/cm (horizontally).

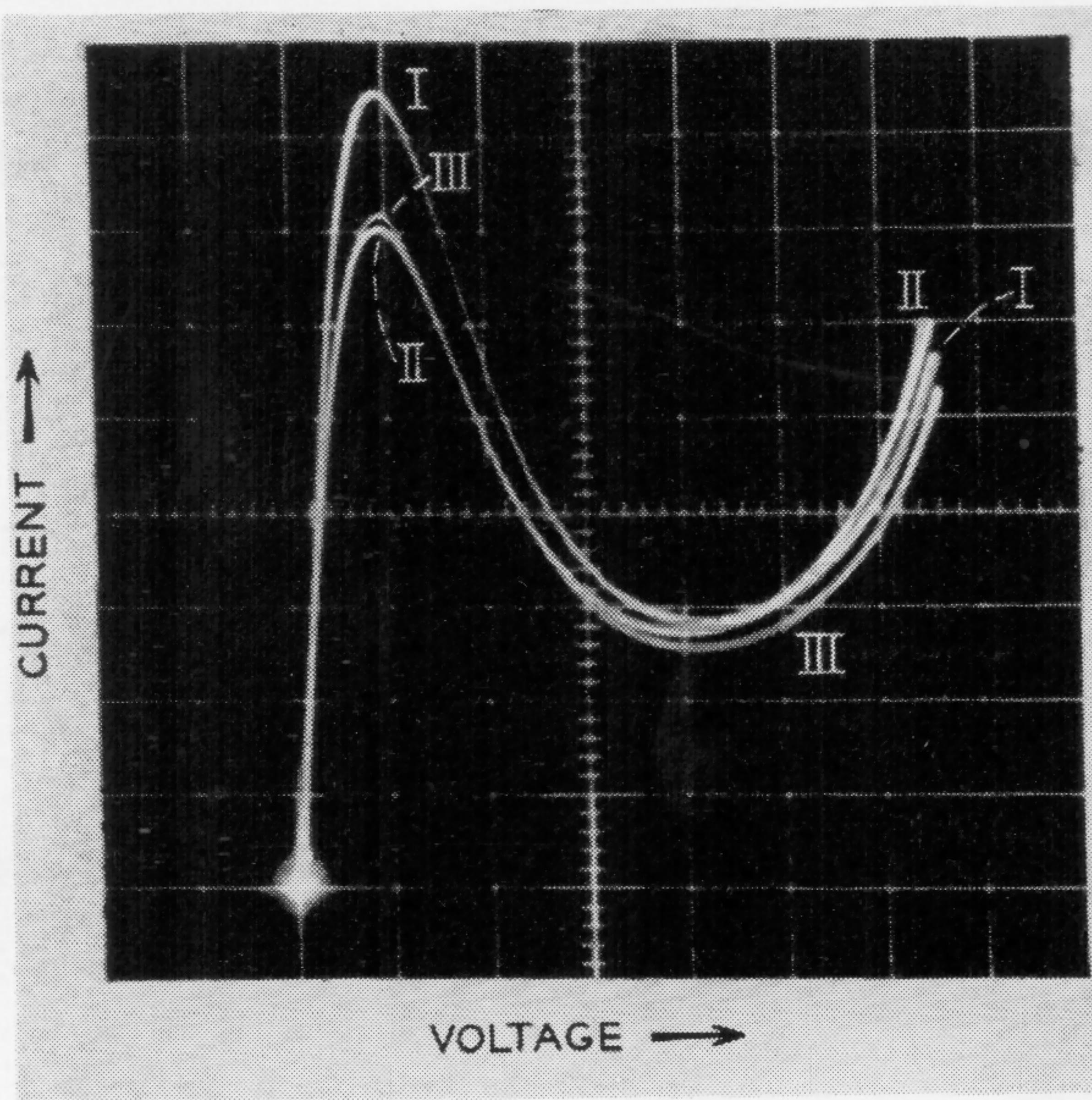


Figure 6—Oscilloscope traces of stabilized  $I$ - $V$  characteristics of a Ge tunnel diode: (I)—atmospheric pressure; (II)—20,000 psi pressure and temperature 8°C above room temperature; (III)—20,000 psi pressure and room temperature.

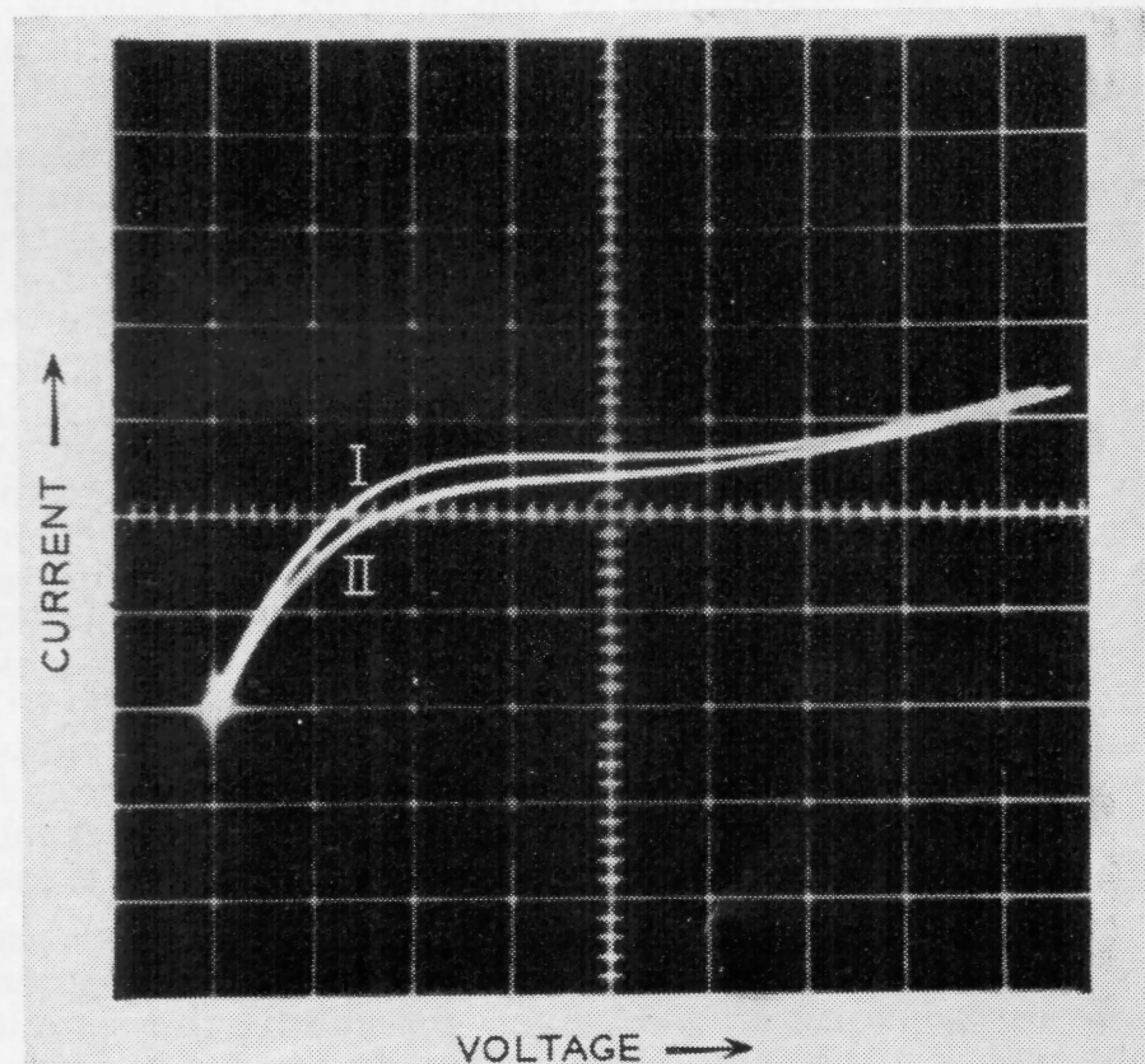
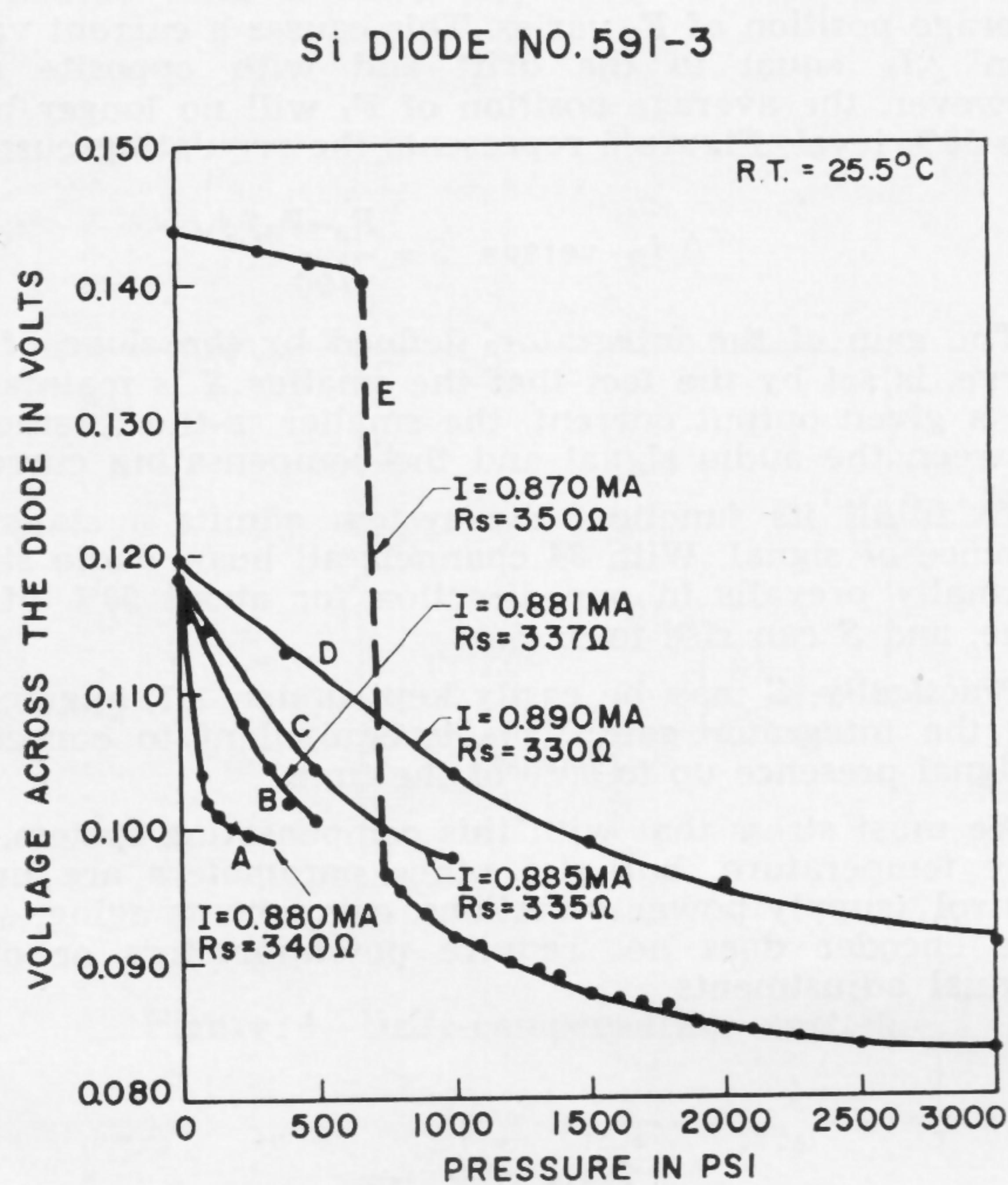


Figure 7—Stabilized current-voltage characteristics of the Ge tunnel diode-resistor combination at different pressures: (I)—atmospheric pressure; (II)—20,000 psi.



(Left)

Figure 5—Voltage across an experimental silicon diode versus pressure in psi. Curves A to D show that the sensitivity to pressure can be adjusted by varying the value of the shunt resistor. Curve E indicates that device can be used to signal the existence of a pressure exceeding a certain value. The signal takes the form of a sudden change in voltage across the diode.

## SESSION VIII: Digital Transmission

Chairman: J. S. Mayo

Bell Telephone Laboratories, Inc., Murray Hill, N. J.

## TA 8.1: A Drift-Free Hyperbolic Encoder

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Telettra S.p.A.

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THIS PAPER will discuss stabilization problems in an audio-signal hyperbolic encoder developed for a *pcm* telephone multiplexing system \*.

The coder is sequential, employs digital feedback, and is based on comparison between sample and reference currents produced by a switch-operated resistive network.

As noted in Figure 1 there are two resistive networks: One with a negative reference voltage to compare positive samples, and one with a positive voltage for negative samples.

Logic and digital parts are common. The network's choice is made according to the sign of the sample at the expense of the first bit. The remaining six bits are available for the sample amplitude.

An audio-signal encoder is different from other analog-digital converters, because of the non-linear relationship between signal and quantizing steps. Naturally this is true when the minimum quantization noise is desired for a given total bandwidth. The most suitable coding law for audio signals is the logarithmic law which is characterized by the fact that the spacing between the quantizing steps decreases proportionally with signal strength. A resistive network producing weighting currents with logarithmic distribution with a series of switches commuting between two positions is however rather complicated. An approximate solution was chosen using hyperbolic distribution which is fairly close to logarithmic distribution in the audio-signal dynamic range; 40-db were considered. It is possible to obtain such behavior with a relatively simple network; Figure 2. The relation between the voltage  $V$  and the  $n$  possible switch configurations is a hyperbola. A proportional current will be compared with the signal.

The application of the hyperbolic coding law increases noticeably the performance required from the system. In our case, having only 64 levels for coding the samples of one polarity, the samples corresponding to the minimum and maximum levels differ in the 1:1350 ratio; that is 20  $\mu$ a to 27 ma. This dynamic requirement is excessive for semiconductor systems which are limited by their thermal sensitivity and their lack of uniformity when improperly selected. Particularly, temperature variations will impair the performance because of current drifts that can submerge the weaker quantizing levels. Where these impairments may occur—at the switches and at the input of the limiter-amplifier—are illustrated in Figure 3. The internal resistance of saturated transistors used as switches is not zero because they present a voltage drop  $V_{sw}$ . Furthermore at point C where the comparison is made, there is a fixed potential  $V_c$ , due to the base-emitter voltage drop of the

input transistor of the limiter-amplifier. For a given temperature this is not a problem, because transistor internal resistance can be considered as part of weighting resistors, and  $V_c$  can be compensated by external bias. However, since a rather large temperature range is considered, i.e.,  $-10^\circ\text{C}$  to  $-50^\circ\text{C}$  or  $10^\circ\text{F}$  to  $120^\circ\text{F}$ , there are two types of drawbacks:

- (1)—Variations  $\Delta R$  of switch resistance impair the hyperbolic characteristic.
- (2)—Current drifts larger than the weakest signals take place.

Case (1) can be contained in acceptable limits. For case (2) a compensation system has been adopted, Figure 4, and operation is as follows:

Audio signal are coded with alternate samples; thus, for a time constant large enough the number of positive samples is equal to the number of negative samples. Furthermore during the coding process of a sample there is a time interval in which all switches are conducting, short circuiting the network to ground, and the current contribution from the network to point C should be zero. Checks with synchronized pulses at the gate G during this interval develop outputs which are functions of the audio signal only.

Pulses are therefore present in 50% of cases and  $F_1$  will operate following them. An integrator develops an output voltage proportional to the average voltage value at one of the collectors of  $F_1$ . The phase of the current flowing through resistance  $R_R$  is such that it automatically controls the equilibrium of point C. When a drift occurs, the average position of  $F_1$  varies. This causes a current variation  $\Delta I_R$  equal to the drift and with opposite sign. However, the average position of  $F_1$  will no longer be at the 50% level; Figure 5 represents the regulating currents

$$\Delta I_R \text{ versus } S = \frac{P_p - P_n}{100}$$

The gain of the integrator, defined by the slope of the curve, is set by the fact that the smaller  $S$  is maintained for a given output current, the smaller is the interaction between the audio signal and the compensating currents.

To fulfill its function, the system admits a statistical absence of signal. With 24 channels all busy, audio signal normally prevails in one direction for about 50% of the time, and  $S$  can rise to  $\pm .5$ .

Practically,  $S$  may be easily kept under  $.1$ , augmenting the integrator gain. This is equivalent to conceding a signal presence up to 90% of the time.

We must stress that with this compensating system, not only temperature, but also other parameters are under control (supply power variations, components aging, etc.). The encoder does not require potentiometers or other manual adjustments.

\* Encoder characteristics: Channel bandwidth — 4 kc; sampling rate — 8 kc; digits-per-sample — 7 resulting in  $2^7 = 120$  levels per sample; coding available time for sample  $\div 4.5 \mu\text{s}$  and  $4.5/7 = .65 \mu\text{s}$  for a bit.

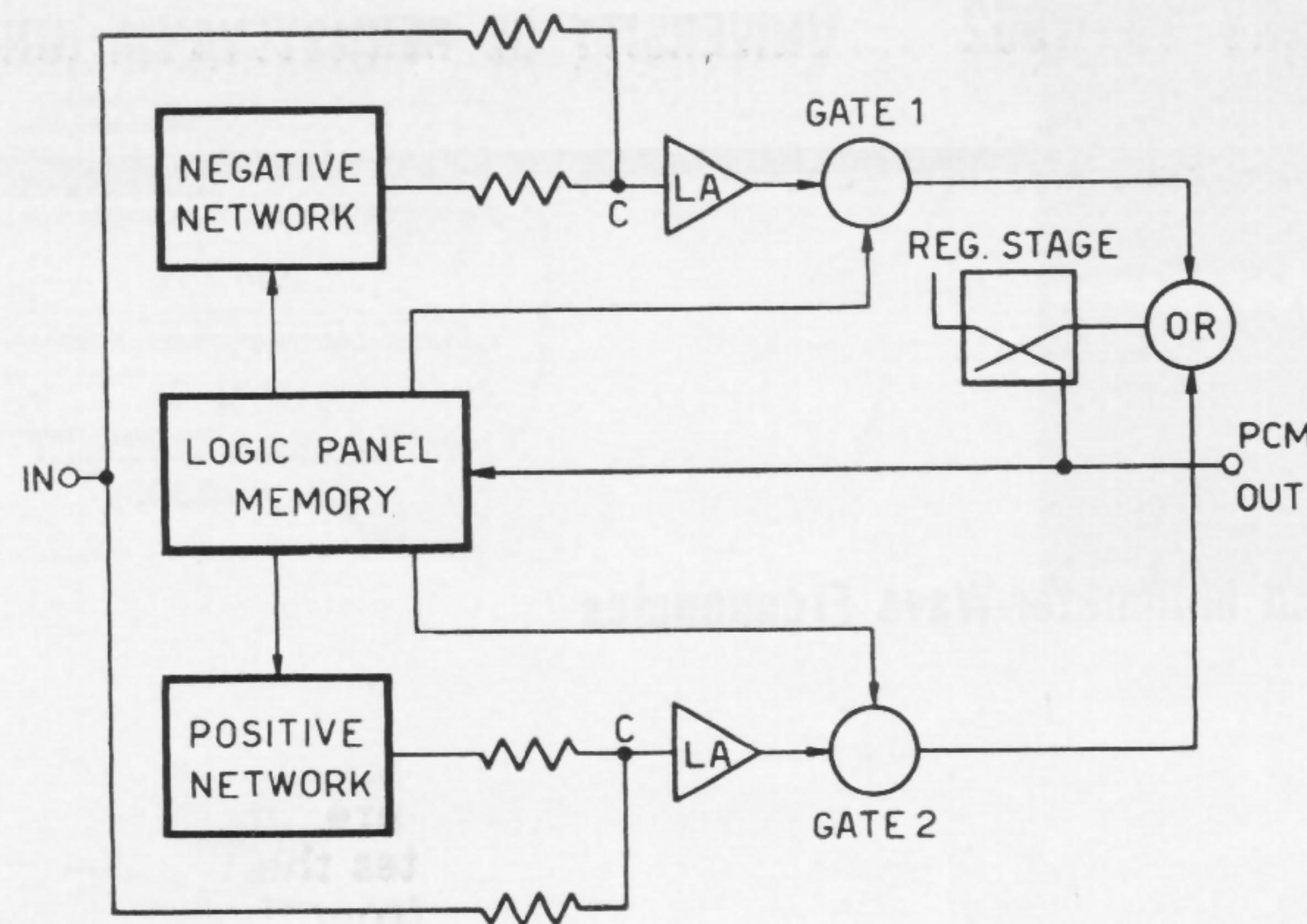


Figure 1—Block diagram of audio signal encoder.

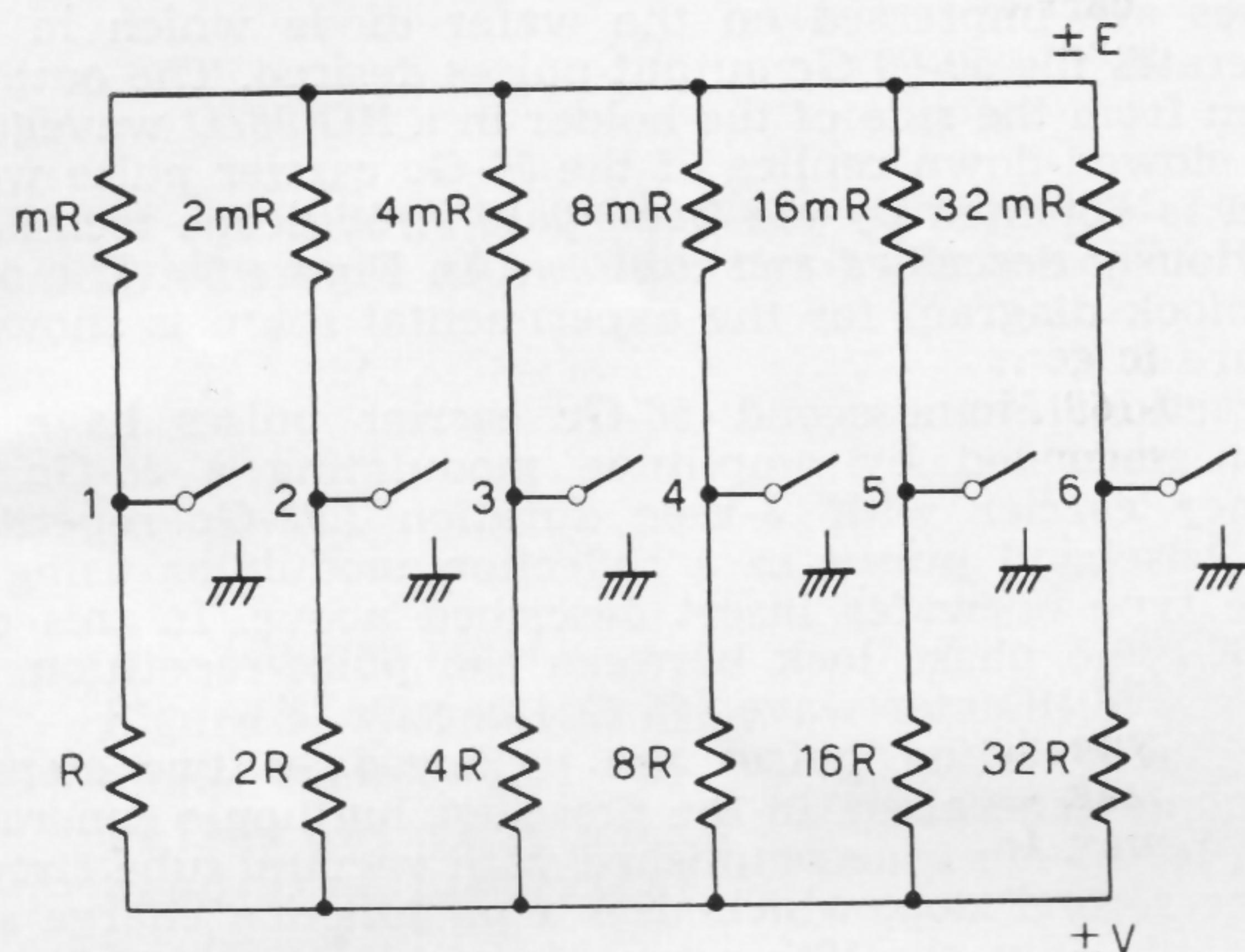


Figure 2—Hyperbolic network:  $V = nE/(m + 1) - nm$ , where E reference voltage

$$n = \frac{2^5 a_1 + 2^4 a_2 + 2^3 a_3 + 2^2 a_4 + 2^1 a_5 + a_6}{63}$$

where  $a_k = 0$ , if the switch is closed or = 1 if the switch is open.

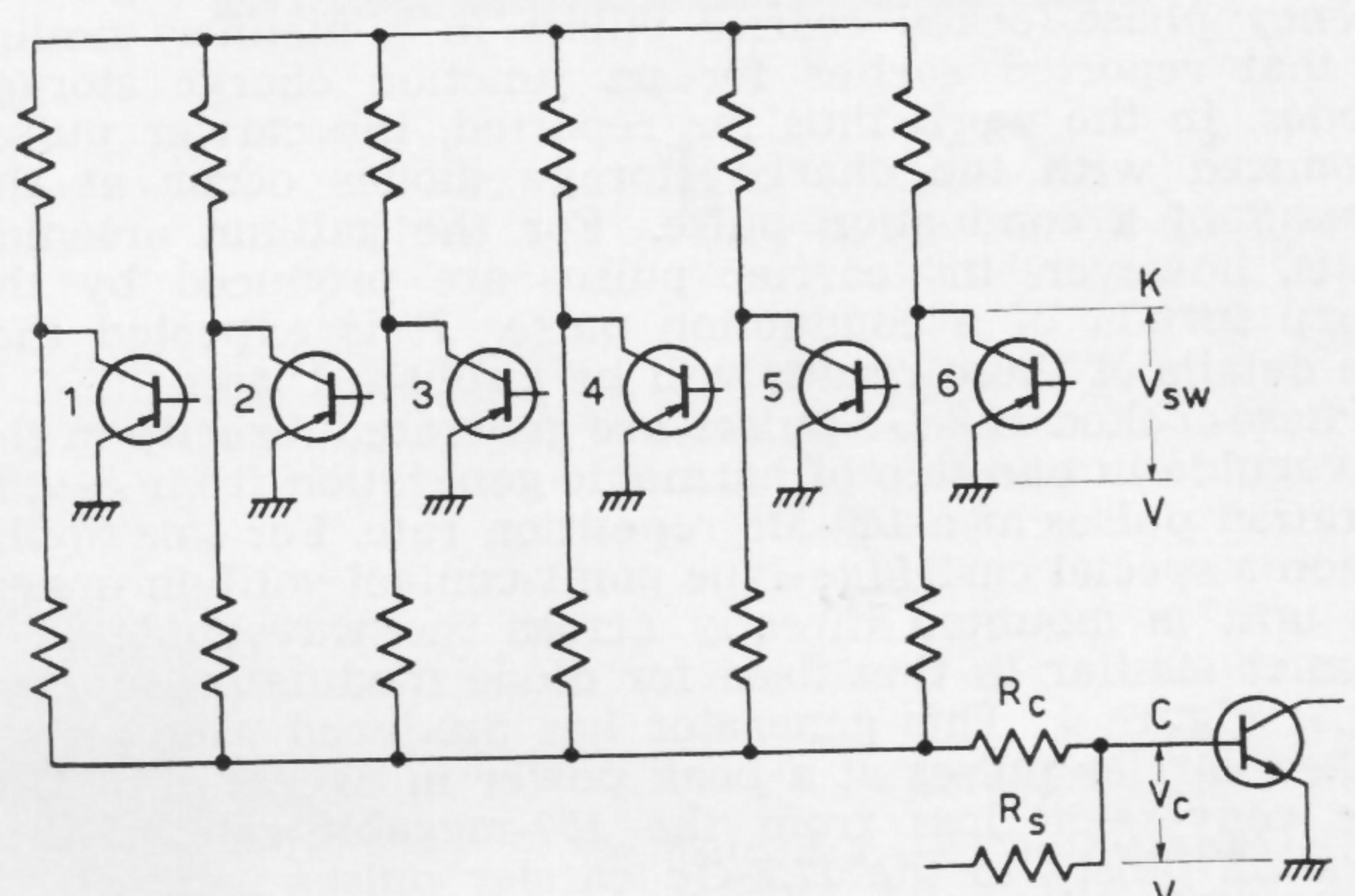


Figure 3—Actual network with thermosensitive points:  $V_{sw}$  = saturated transistor voltage drop;  $V_c$  = base-to-emitter potential of equilibrium-deciding transistor.

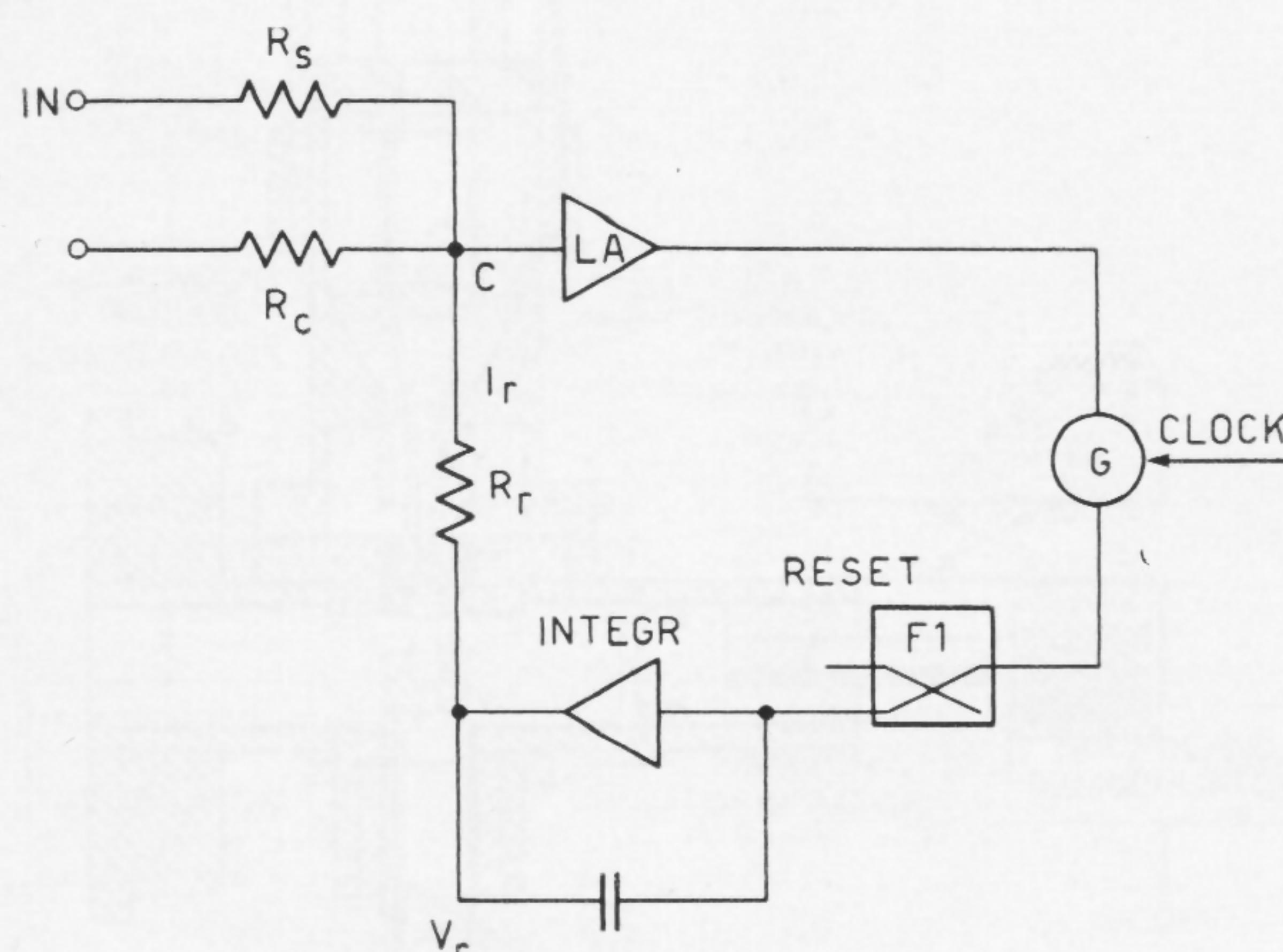


Figure 4—Drift-compensating system.

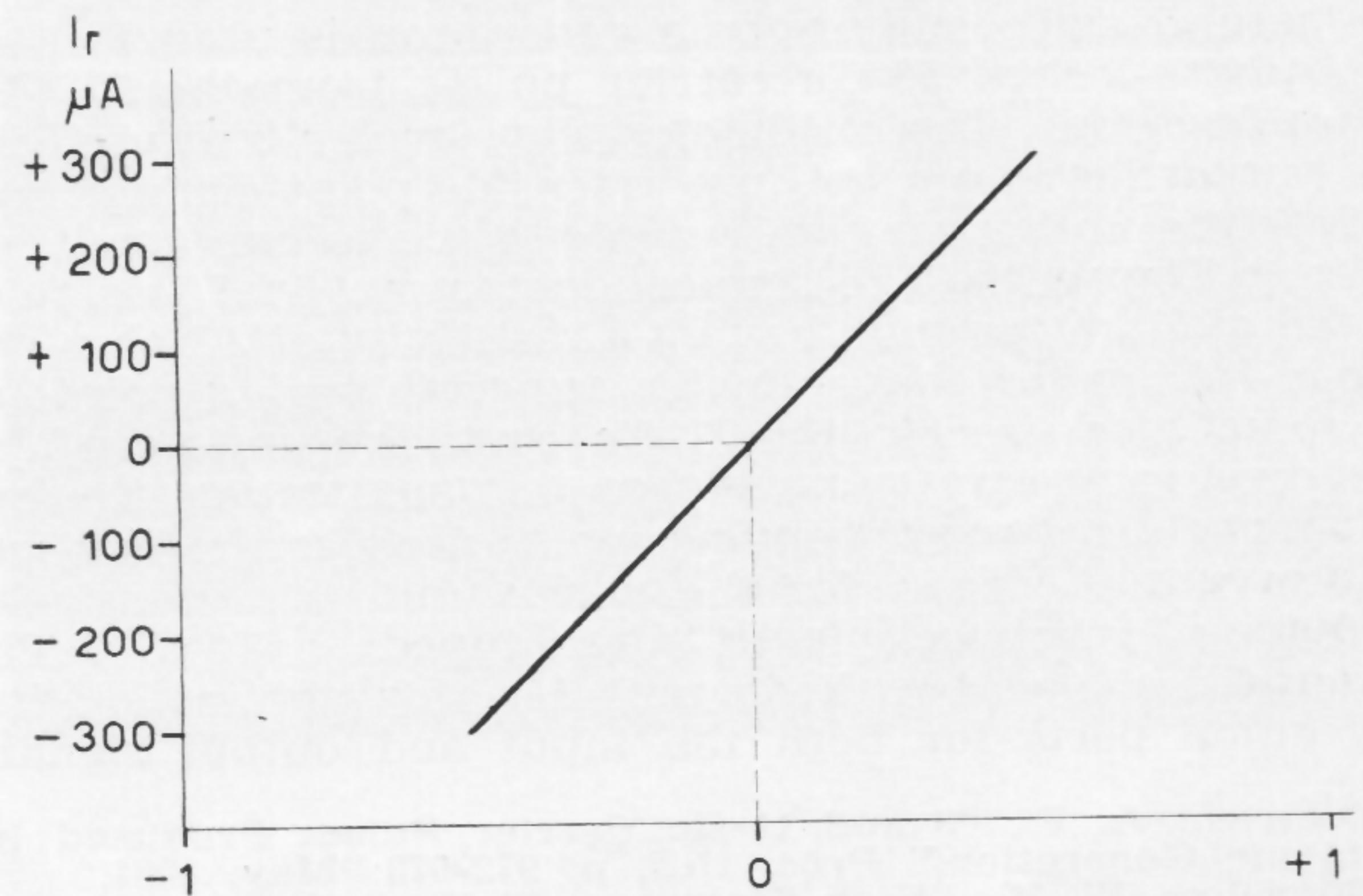


Figure 5—Plot illustrating results of  $I_R$  compensating-current versus  $S = P_p - P_n/100$ , where  $P_p$  = number of times that  $F_1$  has been set and  $P_n$  = number of times  $F_1$  has not set during the proper time constant.

## SESSION VIII: Digital Transmission

## TA 8.2: Carrier Pulses at Microwave and Millimeter-Wave Frequencies

A. F. Dietrich and W. M. Sharpless

Bell Telephone Laboratories, Inc.

Holmdel, N. J.

IT HAS BEEN FOUND that gallium arsenide point-contact diodes may be used to generate efficiently very high-frequency phase-locked carrier pulses in a manner similar to that reported earlier for *pn* junction charge storage diodes. In the work thus far reported, the carrier pulses produced with the charge storage diodes occur at the *turnoff* of a conduction pulse. For the gallium arsenide units, however, the carrier pulses are produced by the sharp *turnon* of a conduction pulse. It is expected that the details of these results will be published later.

Phase-locked 11.2-Gc pulses are generated directly in the waveguide in one step of harmonic generation from .5-nsec duration pulses at a 160-Mc repetition rate. For this application a special cartridge-type point-contact gallium arsenide unit is mounted directly across the waveguide in a manner similar to that used for diode modulator applications; Figure 1. This generator has produced *nsec* phase-locked carrier pulses at a peak power in excess of .5 *Mw*. The conversion loss from the 160-megabit rate, .5-nsec duration pulses to the 11.2-Gc carrier pulses is 32 db.

The special point-contact cartridge units employed here are similar in appearance to the units previously described<sup>2</sup>; Figure 2a. The present units, however, differ in the type and size of the point contact springs as well as in the techniques employed in forming the diodes. The semiconductor material is *n*-type single-crystal gallium arsenide having a resistivity of .002 ohm-cm. The *S*-spring points are made of one-mil tungsten wire for strength and are copper plated to supply the doping needed during the forming operation. A small amount of this copper (a *p*-type doping agent in gallium arsenide) diffuses into the *n*-type gallium arsenide during the forming process, which produces the small abrupt junction desired.

The 11.2-Gc carrier pulses generated with these diodes are amplified with a suitable broadband *twt* and then applied to a band-pass electrical stroboscope<sup>1</sup>. The individual cycles of the 11.2-Gc carrier and the carrier pulse envelope duration are shown on Figure 3a.

A second stage of harmonic generation is used to produce phase-locked 56-Gc carrier pulses from the 11.2-Gc pulses described. The millimeter-wave wafer unit used for this purpose is also a gallium arsenide point-contact type diode. This unit is similar in appearance to one described earlier<sup>3</sup>; Figure 2b. The semiconductor material is single-crystal gallium arsenide having a resistivity of .03 ohm-cm. One-mil diameter copper-plated tungsten spring points of the same type used in the 11-Gc cartridge units are also employed in the wafer units. For this application, the bypass-capacitor arrangement normally used as the low-frequency output circuit for the wafer unit was redesigned to form a  $\pi$ -network input filter tuned to 11 Gc. The holder for the wafer diode unit for this application has waveguide ports for both the input and output signals;

<sup>1</sup> Dietrich, A. F., "8 and 11-Gc Carrier Pulses Produced by Harmonic Generation," *Proc. IRE*, p. 972-973; May, 1961.

<sup>2</sup> Sharpless, W. M., "High-Frequency Gallium Arsenide Point-Contact Rectifiers," *BSTJ*; January, 1959.

<sup>3</sup> Sharpless, W. M., "Wafer-Type Millimeter Wave Rectifiers," *BSTJ*; November, 1956.

<sup>4</sup> Dietrich, A. F., and Goodall, W. M., "Solid State Generator for  $2 \times 10^{-10}$  Second Pulses," *Proc. IRE*, p. 791-792; April, 1960.

<sup>5</sup> Goodall, W. M., and Dietrich, A. F., "Fractional Millimicrosecond Electrical Stroboscope," *Proc. IRE*, p. 1591-1594; September, 1960.

Figure 4. In this respect it differs from the converter unit previously described<sup>3</sup>. This device is used here as a harmonic generator. It has a short section of RG 52/U waveguide at the input port and the previously-amplified 10-12 Gc pulses are introduced at this port. In the holder, these pulses are impressed on the wafer diode which in turn generates the 50-60 Gc output pulses desired. The output is taken from the side of the holder in a RG 98/U waveguide.

A slowed-down replica of the 56-Gc carrier pulse waveform is obtained by the band-pass stroboscope techniques previously described and is shown in Figure 3b. The overall block diagram for the experimental setup is shown in Figure 5.

Fractional nanosecond 56-Gc carrier pulses have also been generated by amplitude modulating a 56-Gc frequency carrier with .3-nsec duration 1.92-Gc repetition-rate baseband pulses in a reflection modulator using the same type of wafer insert described above. In this case, there is no phase lock between the pulse-repetition rate and the millimeter-wave (56 Gc) carrier.

The modulating pulses are produced in two steps of harmonic generation. In the first step, harmonic generation from 10-160 Mc is accomplished with vacuum tube circuits. In the second step, which uses a *pn* junction charge storage diode only, the 12th harmonic of 160-Mc (1920-Mc sine wave) is filtered out<sup>4</sup>. The 2-v peak-to-peak 1.92-Gc sine wave obtained in this manner is then applied to a series and shunt clipper utilizing gallium arsenide cartridge units of the type described. After clipping, 1.92-Gc clock pulses of 1-v peak amplitude are obtained.

The waveform of the detected envelope of the 1.92-gigabit rate, 56-Gc carrier frequency clock pulses is shown in Figure 6. This presentation was obtained by using the baseband electrical stroboscope<sup>5</sup>.

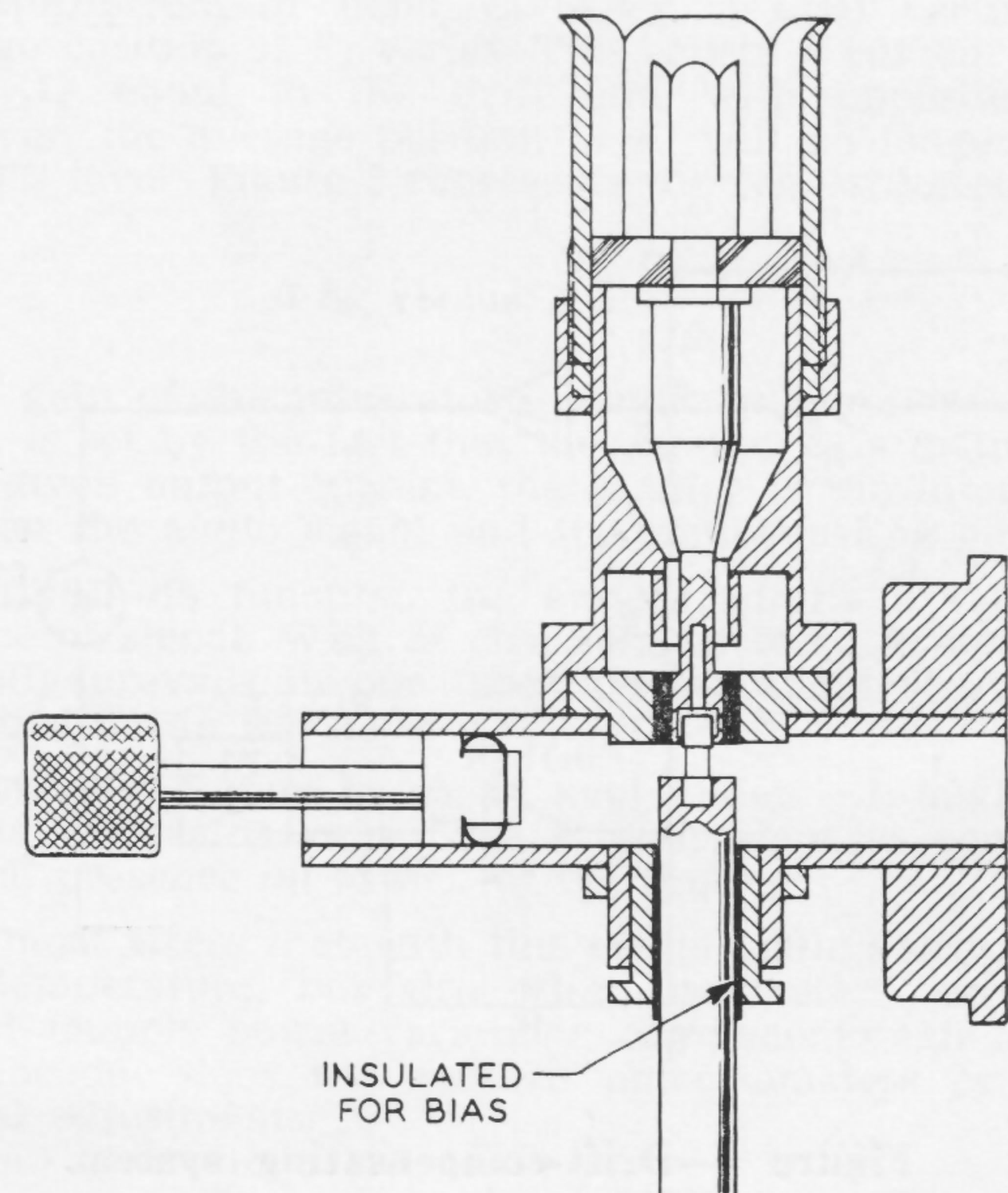
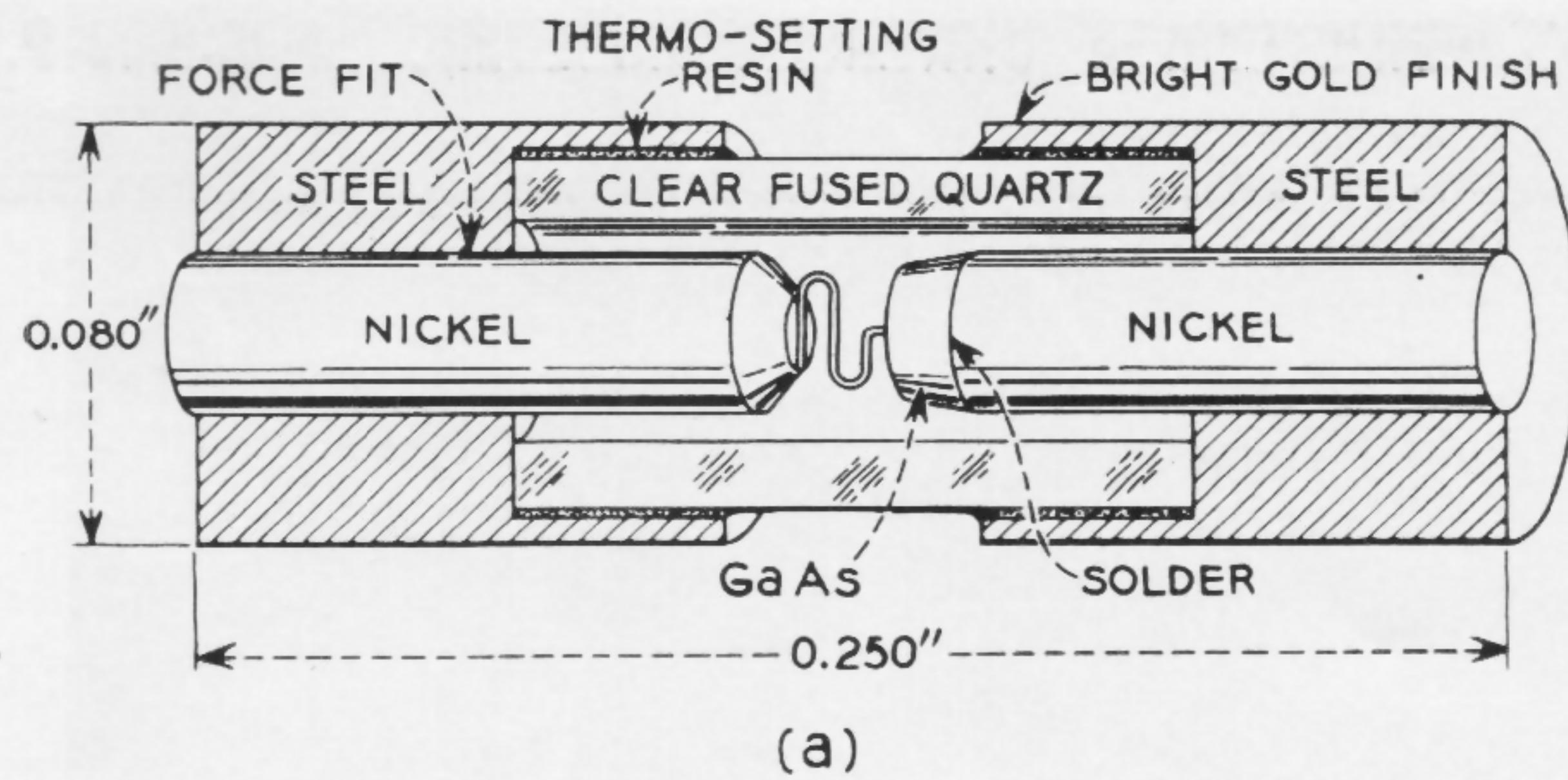
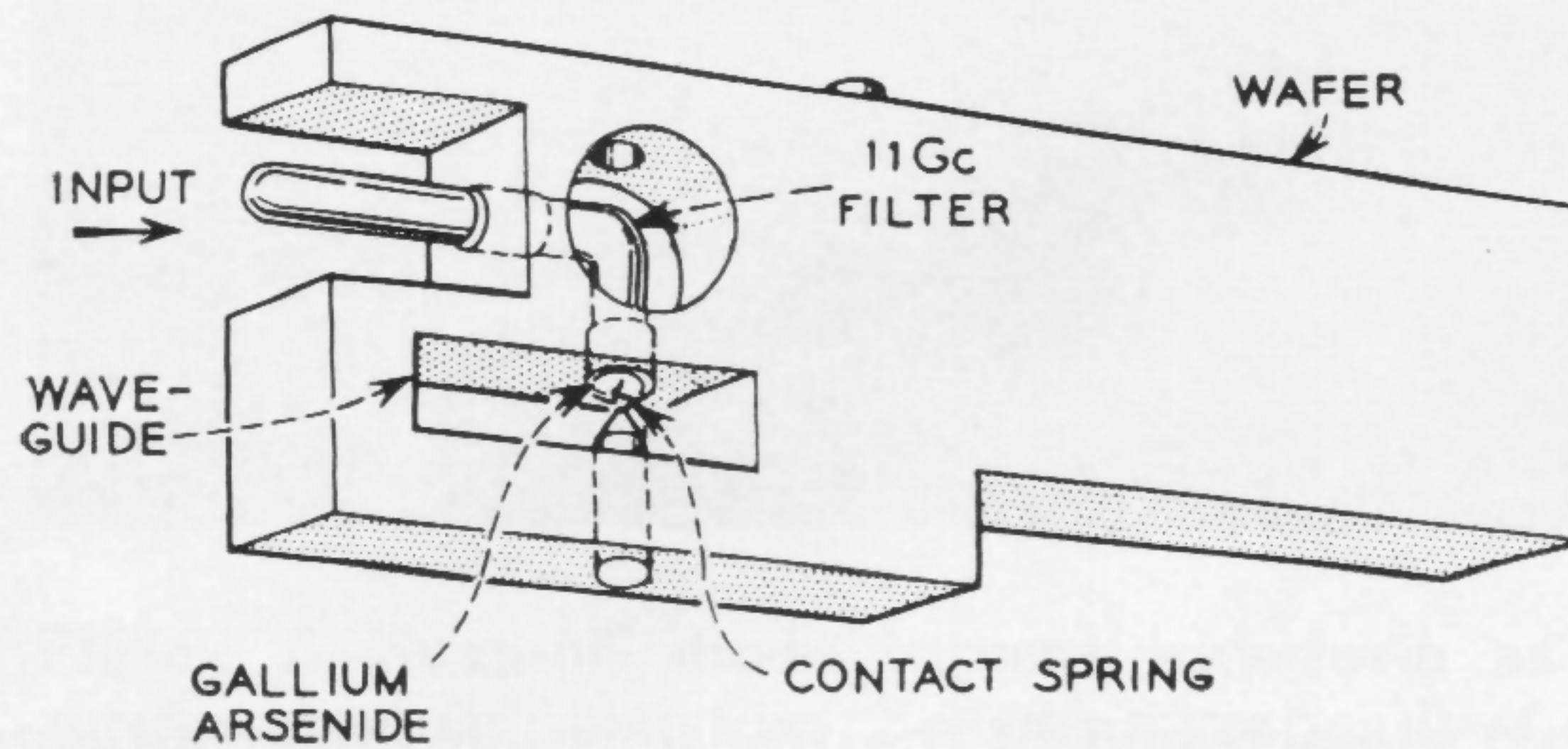


Figure 1—Crosssectional view of X-band waveguide mount.

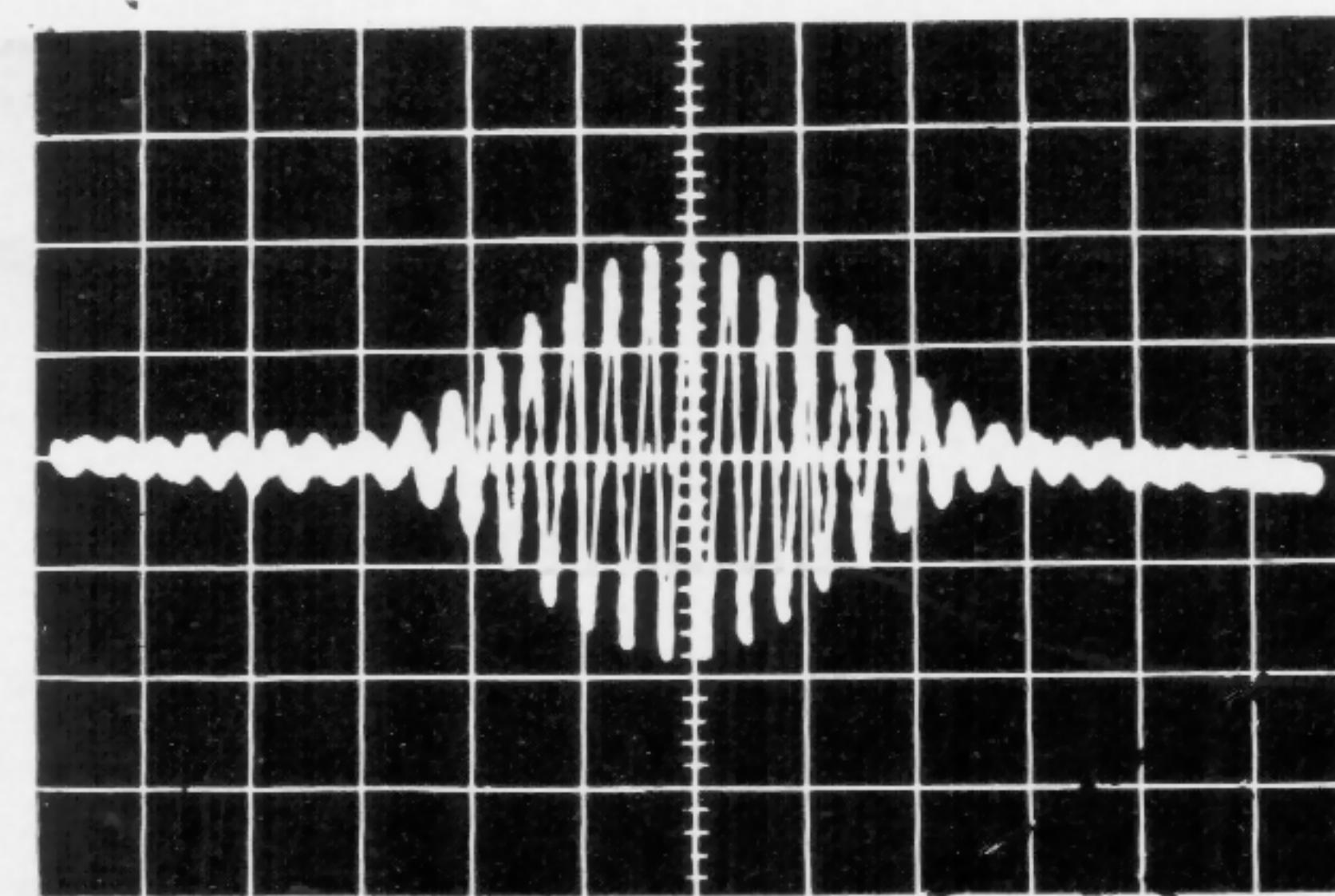


(a)

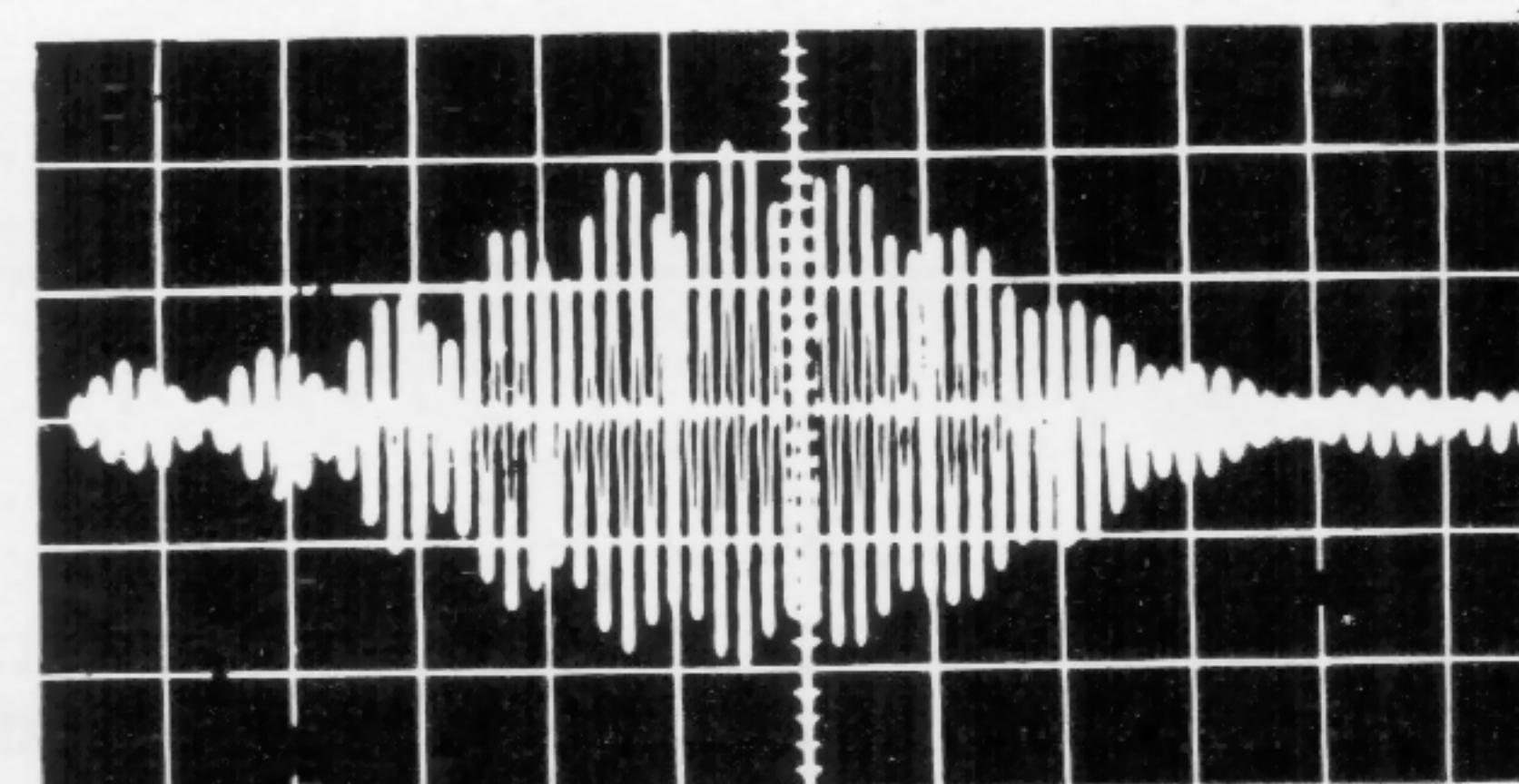


(b)

Figure 2—Gallium arsenide diode assemblies: (a)—cartridge unit; (b)—millimeter-wave wafer unit.



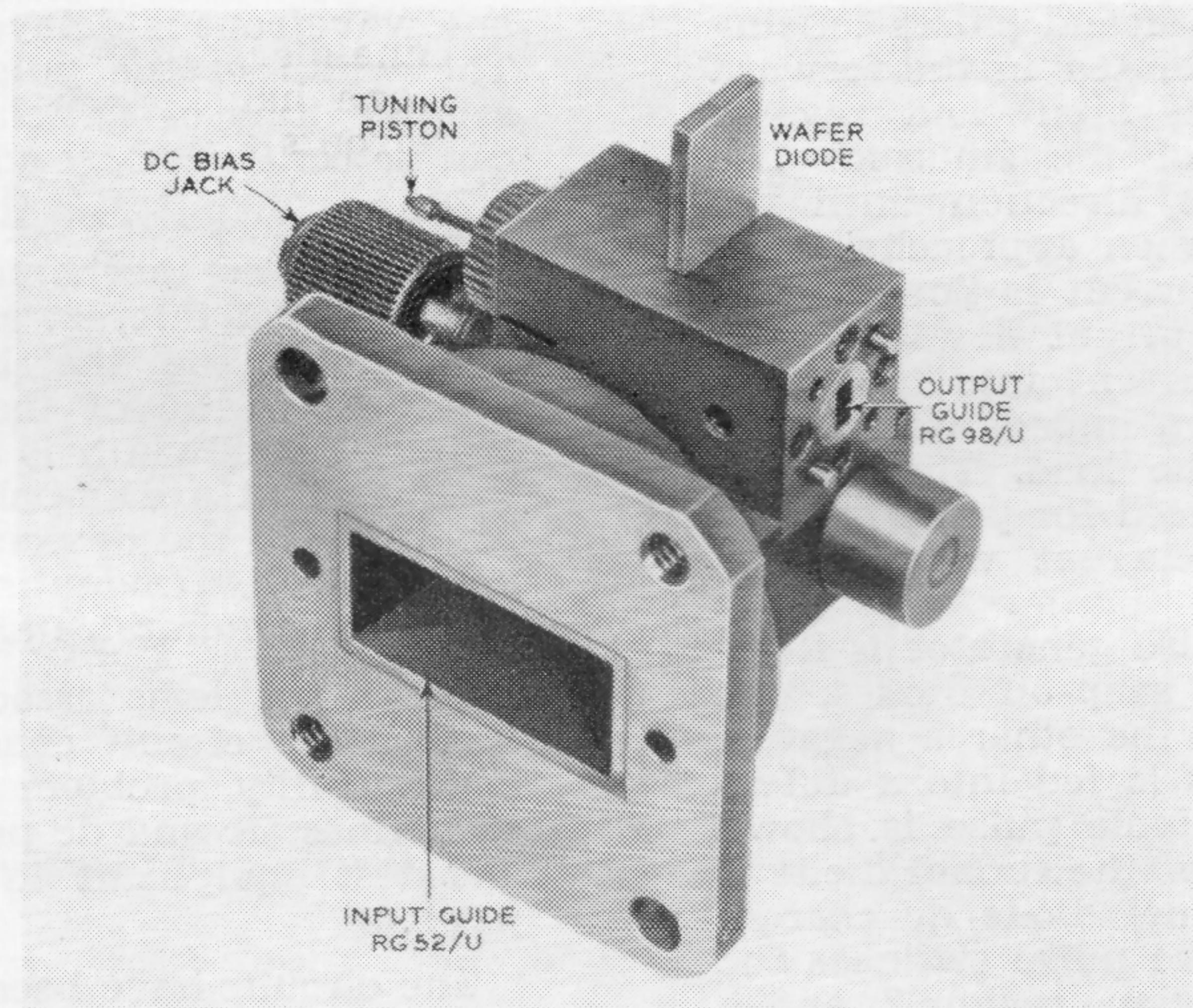
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Figure 3—Waveforms of phase-locked carrier pulses obtained with band-pass electrical stroboscope: (a)—160-megabit rate, 11.2-Gc pulses (horizontal .25-nsec/div); (b)—160-megabit rate, 56-Gc pulses (horizontal 100-psec/div).



(Left)

Figure 4—Photograph of X band to millimeter-wave band harmonic generator unit.

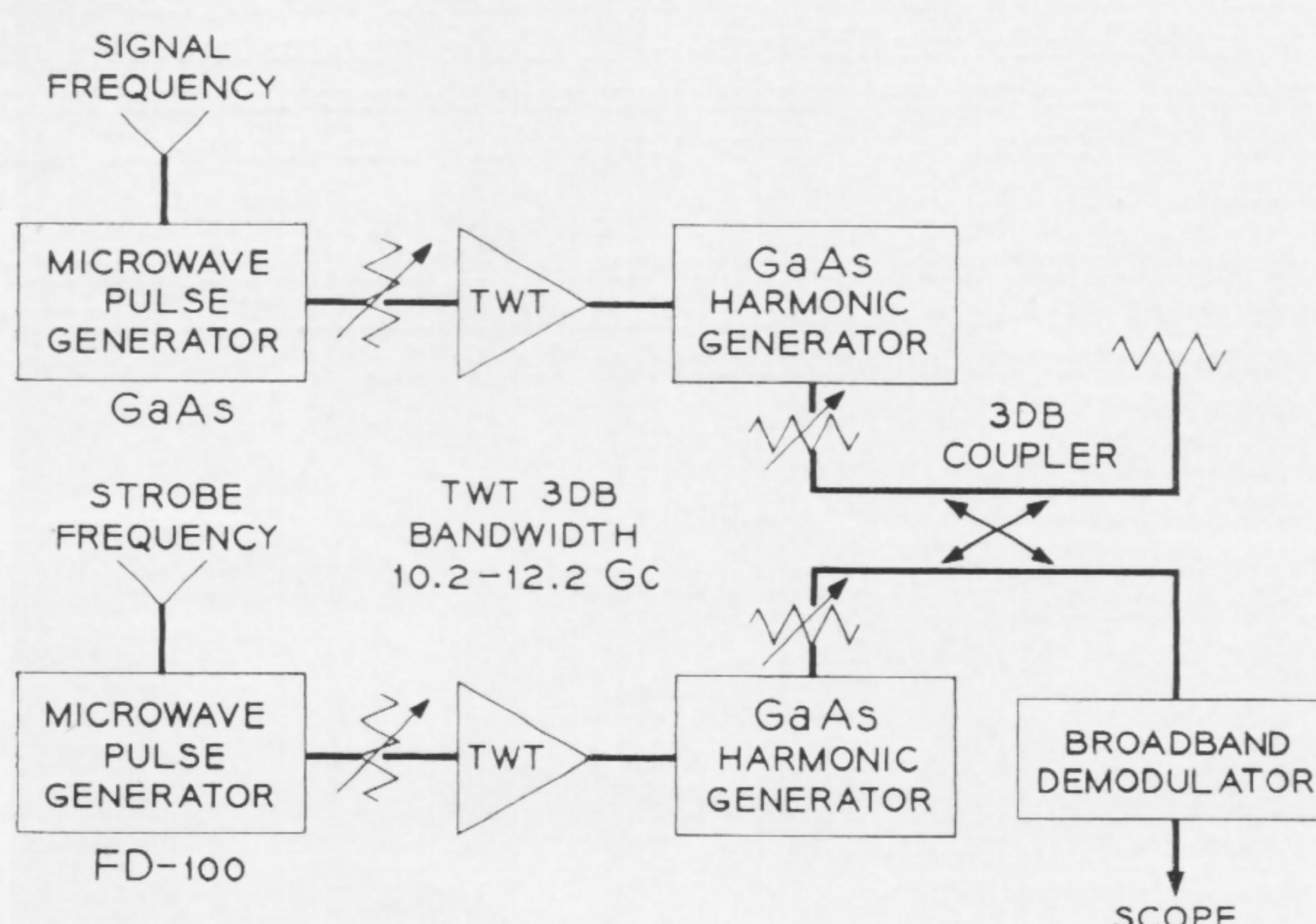
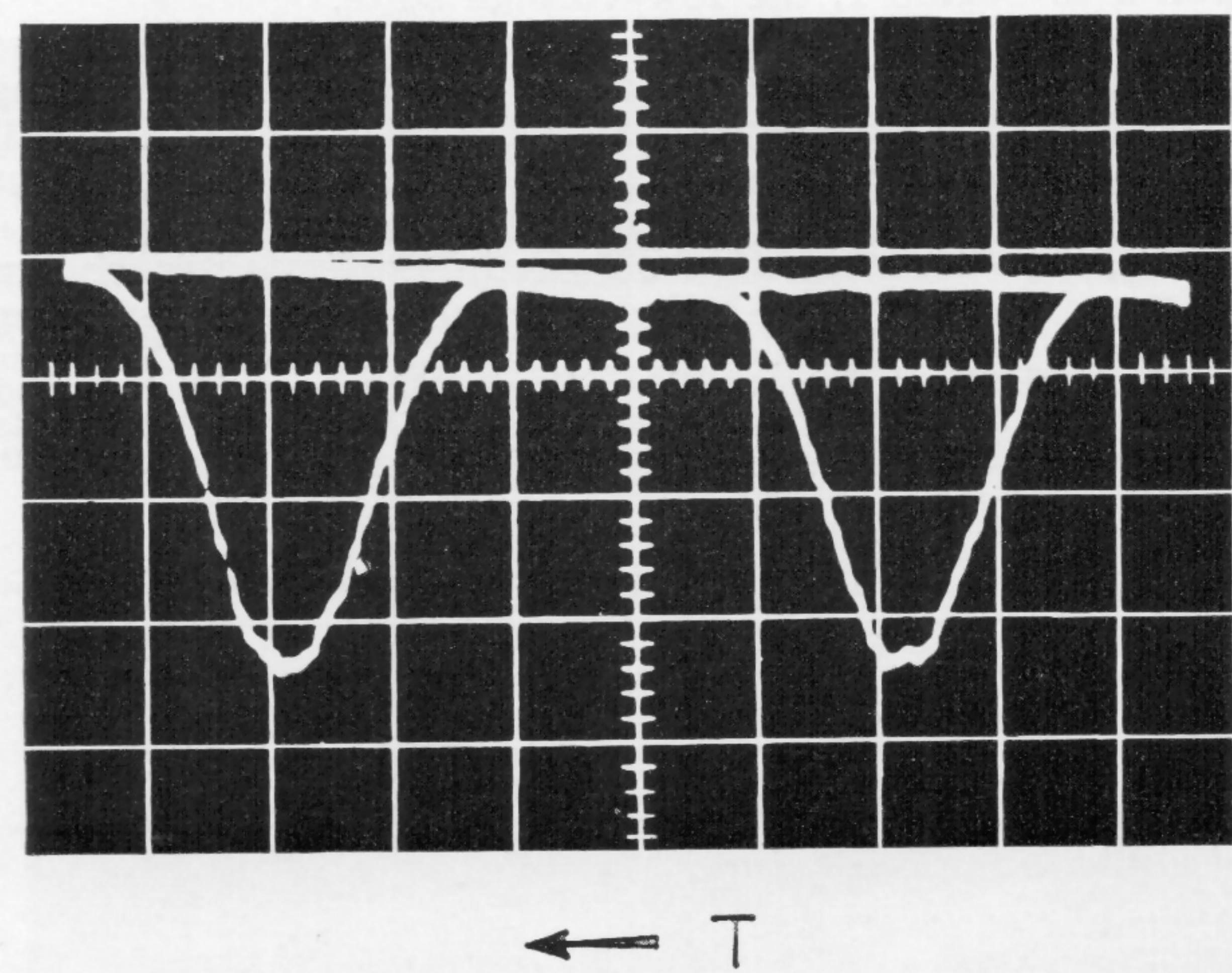


Figure 5—Block diagram of experimental setup for generating and viewing phase-locked carrier pulses.



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Figure 6—Waveform of detected 1.92-gigabit rate 56-Gc carrier-frequency clock pulses obtained with the baseband electrical stroboscope; horizontal 100 psec/div.

## SESSION VIII: Digital Transmission

## TA 8.3: Variable-Width Fractional-Nanosecond Pulse Generators

D. L. Berry

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Syracuse, N. Y.

THIS PAPER will describe two variable-width fractional-nanosecond pulse generators utilizing tunnel diodes, back diodes, and snap-off diodes. These diodes have two impedance states whose magnitudes differ by approximately two orders of magnitude. The diodes can be switched between the two impedance states during a fraction of a nanosecond in either direction. The pulse repetition frequency for the generators is in the 40 to 50-Mc range.

The recovery characteristics of snap-off diodes are used for the generation of fractional nanosecond pulses<sup>1</sup>. Using a sinusoidal ac bias, the diodes are biased in the forward direction by part of the sinusoidal input and reverse biased by the remaining portion of the sinusoid. The diodes can conduct in the reverse direction until the minority carrier density of the junction approaches zero. During the time that the reverse current is flowing into the diode, only a small amount of current flows into the load. After the reversed flow of current into the diode has stopped, the diode becomes a high impedance and the reversed current now flows into the load. This abrupt change in the current waveform is used for pulse generation. An illustration of the load current waveform is shown in Figure 1.

The circuit of the tunnel diode pulse generator is illustrated in Figure 2. There are two snap-off diodes, one generating a positive waveform and the other a negative waveform. Each of these waveforms is fed into a differentiating capacitor. The resultant dipole pulse is shown in Figure 3. The mode of operation of the tunnel diode is described with reference to the tunnel diode dc characteristic shown in Figure 4. A positive pulse switches the tunnel diode to the high voltage region, region 2, and a negative-trigger pulse resets the tunnel diode back from region 2 to region 1, the low-voltage state.

The width of the pulse is determined by the relative time of switching between the two diodes. By adjusting the total bias on the snap-off diodes, this relative time will either decrease or increase, depending on whether the bias on the diodes has been increased or decreased.

The circuit for the snap-off diode generator is shown in Figure 5. Two snap-off diodes are used, one diode being

mounted at each end of the transmission line. The output terminals of the generator are located on the transmission line one half the distance between the two diodes. The wavefronts generated by each diode travel in the transmission line until they collide at the output terminals on the transmission line. If the wavefronts, except for the polarities, are identical in shape and they both arrived at the same time at the output terminals, the sum of the two wavefronts at the output terminal is zero. However, if one wavefront is delayed, the difference is no longer zero. The width of the pulse can be varied by changing the relative time of switching between the diodes. This time can be controlled by adjusting the total bias in the diodes.

The devices used for the pulse generators need certain electrical and mechanical characteristics. Electrical characteristics of interest are the intrinsic reactances because they determine the bandwidth and the high to low impedance ratio of the diodes. For a .5 nsec pulse, the required bandwidth is at least 2 kMc. Mechanical characteristics that are important revolve about packaging and mounting of the devices into the circuits. The problem of packaging and mounting devices is important because of the need to minimize external reactances.

Other problems associated with nanosecond-pulse generators are circuit construction techniques including the compatibility problem that exists between coaxial and strip lines, ac and dc power requirements, reproducibility, and test equipment to measure pulse shapes and pulse jitter.

The circuits have been experimentally verified. A repetition rate of 40 Mc was used for the generators. The pulse width for the tunnel-diode generator can be varied between .5 and 8 nsec and for the snap-off diode generator from .4 to 3 nsec. The base line is negligible for the tunnel-diode generator. Back diodes improved the signal-to-base line noise ratio for the snap-off diode generator. The peak power of the pulses varies between 20 mw for the tunnel-diode generator to one watt for the snap-off diode generator.

A spectrum analysis was made of the pulse waveform generated by the snap-off diode generator. The first zero crossing was at approximately 3.4 kMc.

<sup>1</sup> Boff, A. F., Moll, J., and Shen, R., "A New and High-Speed Effect in Solid State Diodes," International Solid-State Circuits Conference Digest of Technical Papers, p. 50-51; February, 1960.

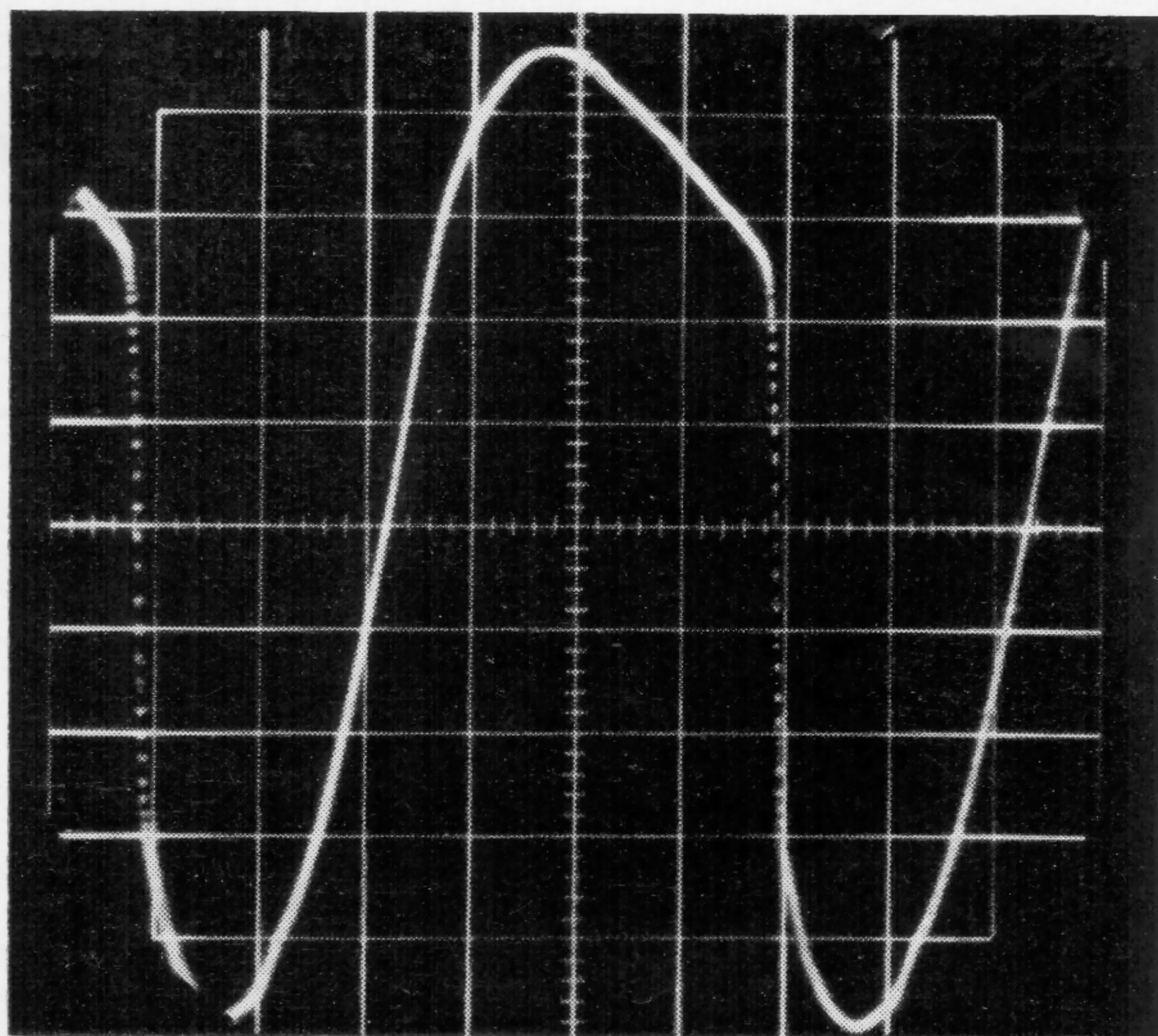


Figure 1—Snap-off diode current waveform as seen across the load resistor: .5 v/div; vertically 4-nsec/div.

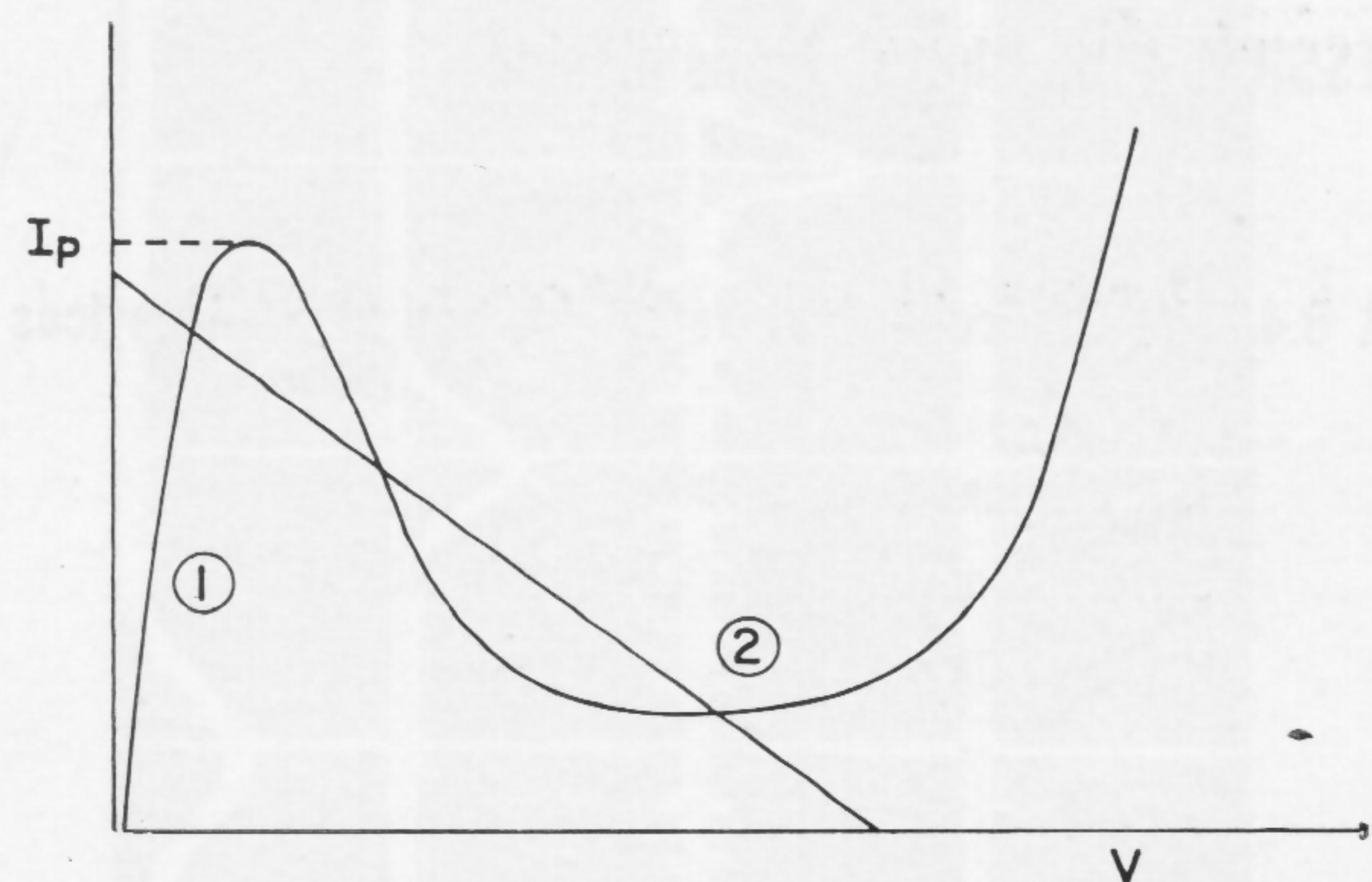


Figure 4—Tunnel-diode load line.

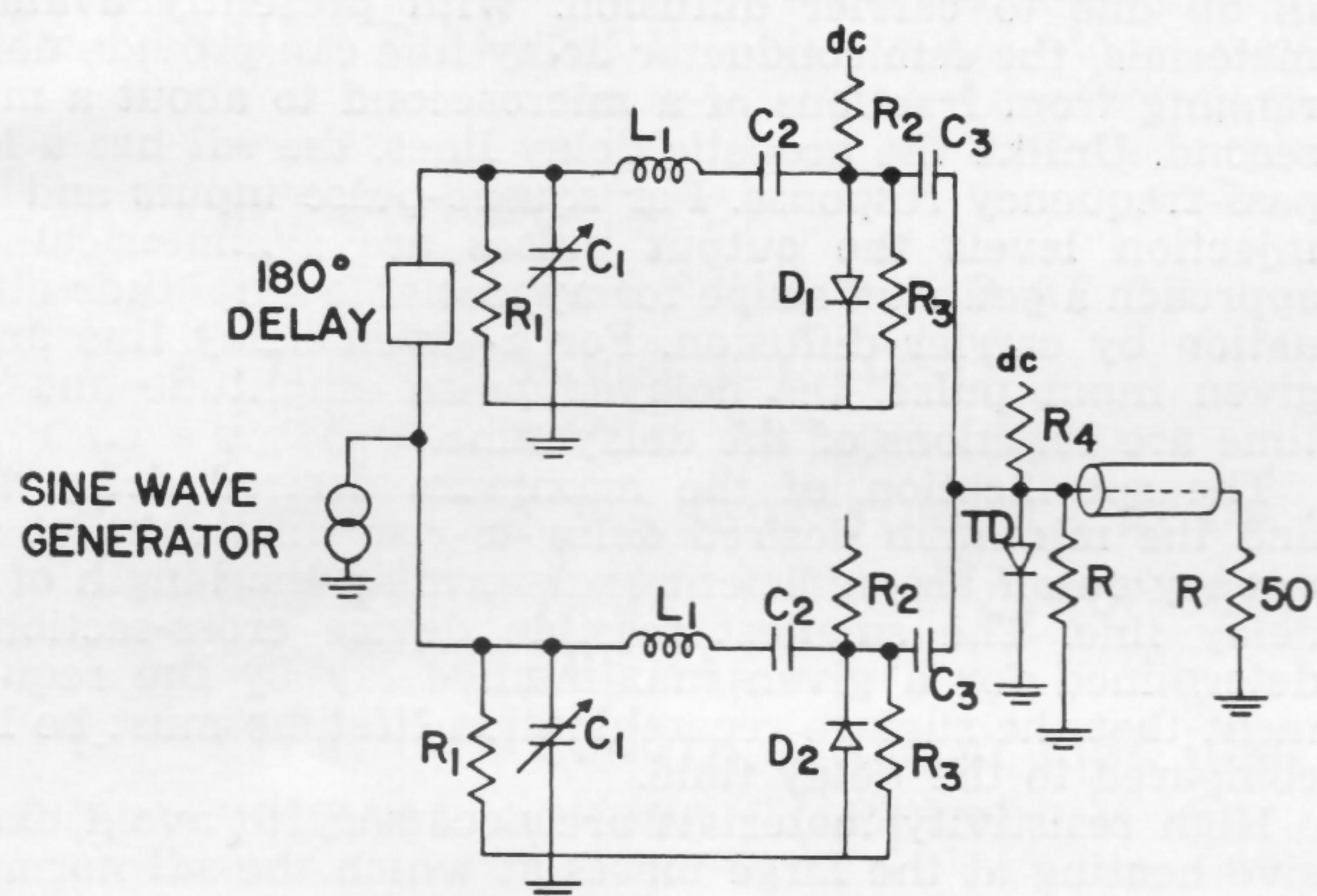


Figure 2—Tunnel-diode pulse-generator circuit.

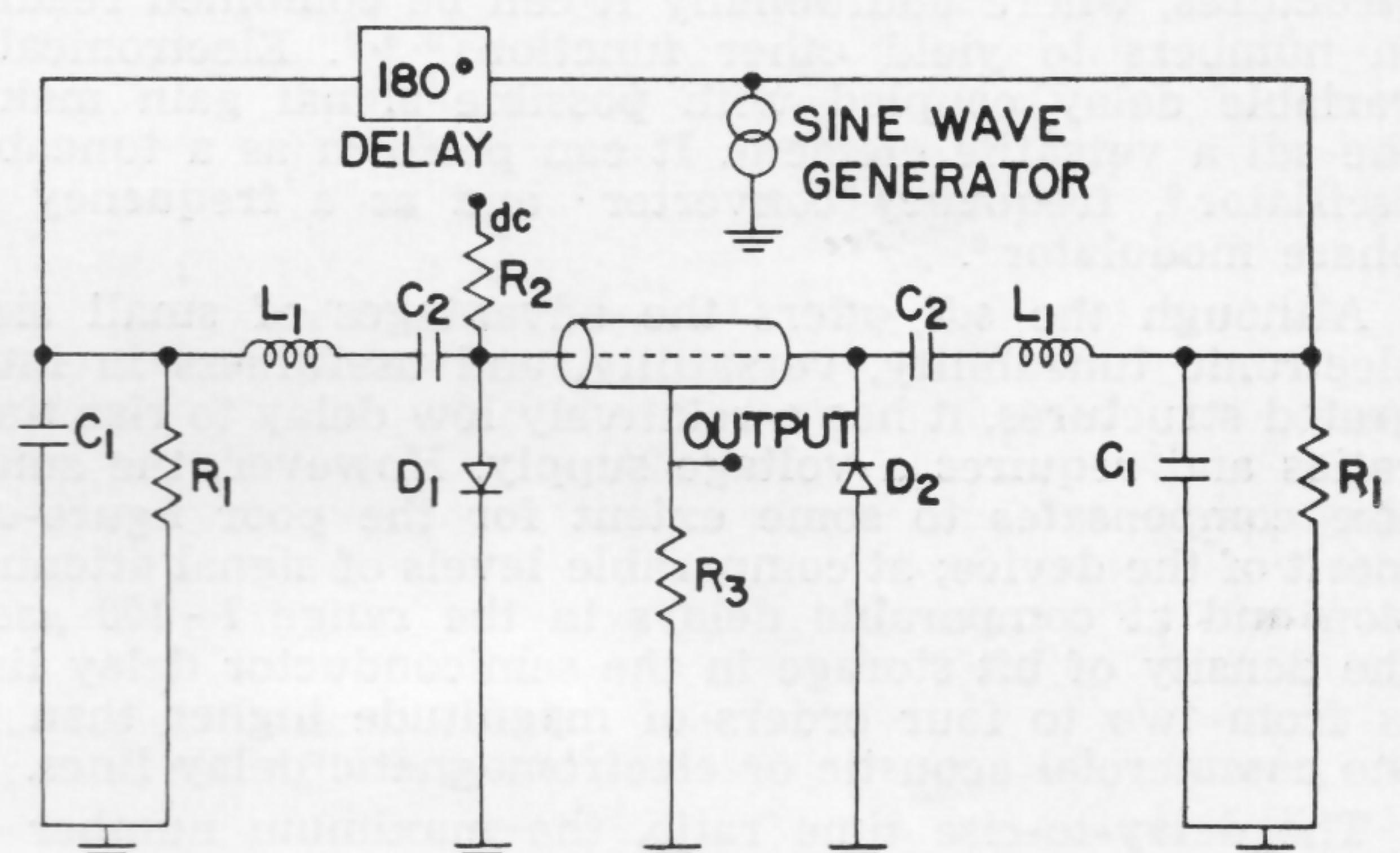


Figure 5—Snap-off diode generator circuit.

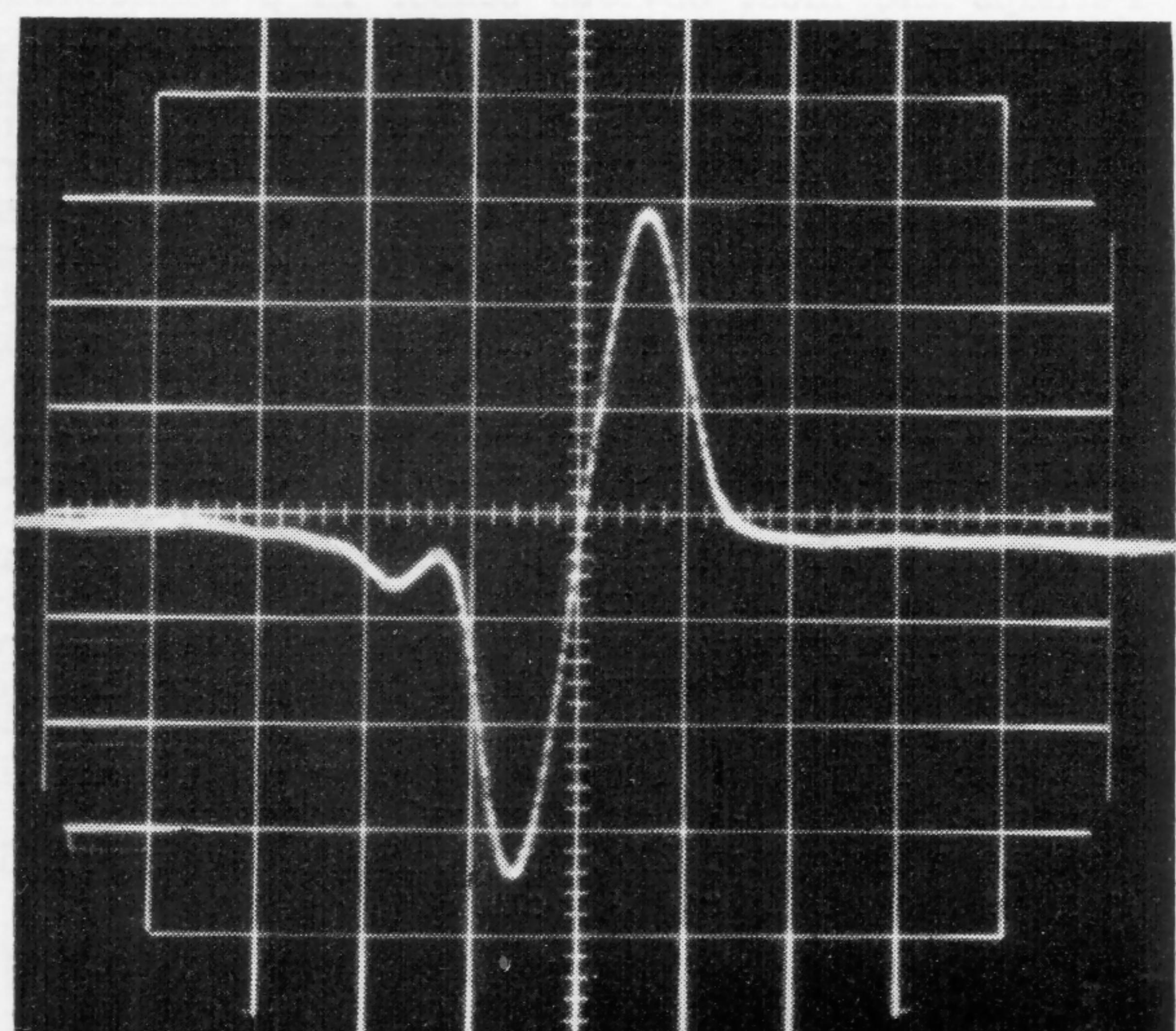


Figure 3—Dipole pulse used to trigger the tunnel diode: 1 v/div; vertically 1-nsec/div.

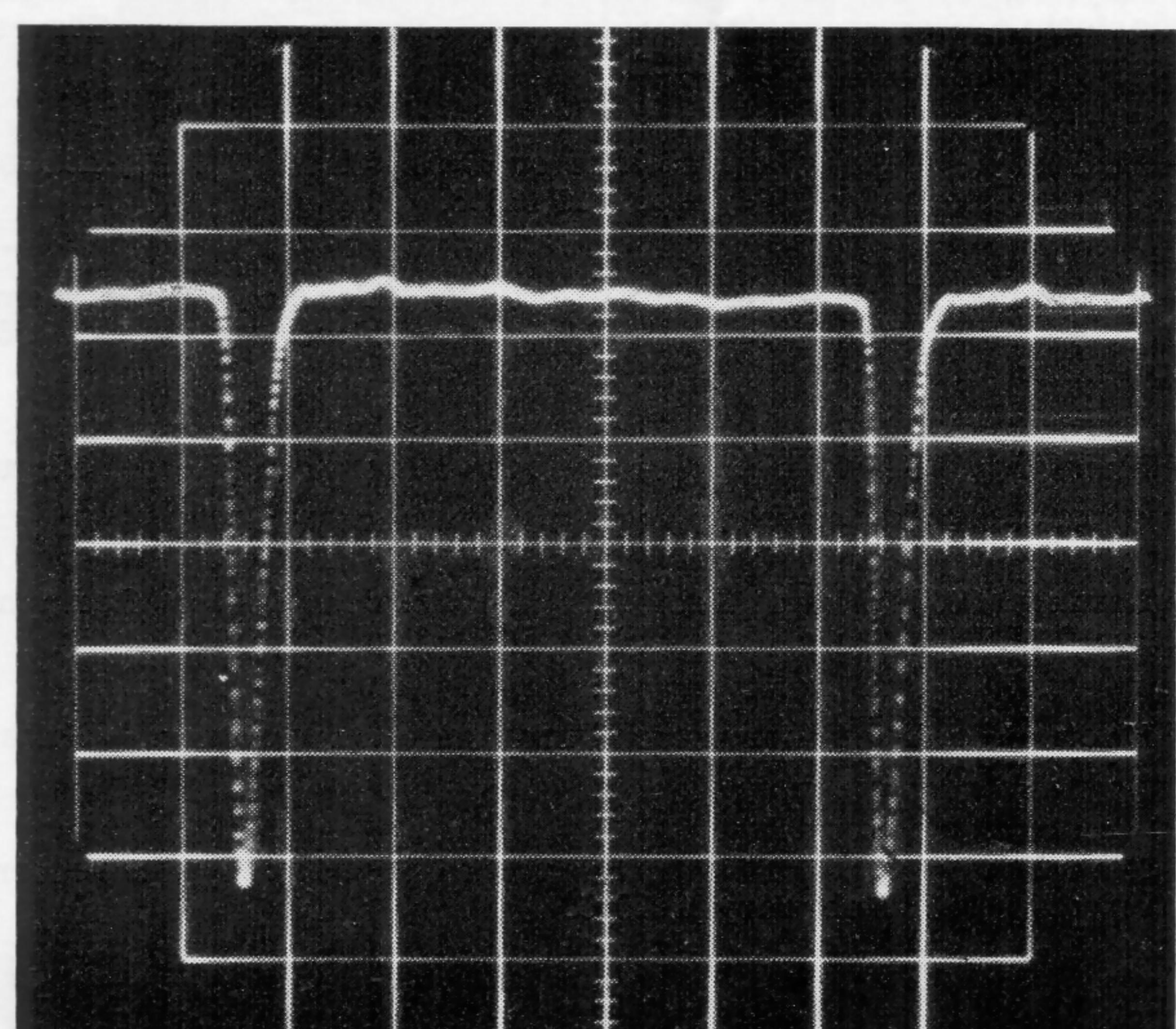


Figure 6—Output of the snap-off diode generators: 5 v/div; vertically 4-nsec/div.

## SESSION VIII: Digital Transmission

## TA 8.4: The Semiconductor Delay Line and Related Devices

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THE SEMICONDUCTOR DELAY line<sup>1, 2</sup> is an active circuit element with an electronically variable delay and a high delay per-unit volume. It utilizes the time of propagation of an excess minority carrier pulse along a filamentary transistor; however, it differs from the latter in that it requires a localized sensor to effect pulse readout.

Small size and structural simplicity make the *sdl* (semiconductor delay line) applicable in integrated electronic structures, where additionally it can be combined readily in numbers to yield other functions<sup>3, 4, 5</sup>. Electronically variable delay coupled with possible signal gain makes the *sdl* a versatile element. It can perform as a tuneable oscillator<sup>6</sup>, frequency converter<sup>7</sup> and as a frequency or phase modulator<sup>8</sup>.

Although the *sdl* offers the advantages of small size, electronic tuneability, versatility, and usefulness in integrated structures, it has a relatively low delay to rise time ratios and requires a voltage supply. However, the small size compensates to some extent for the poor figure-of-merit of the device; at comparable levels of signal attenuation and at comparable delays in the range 1-100  $\mu$ sec, the density of bit storage in the semiconductor delay line is from two to four orders of magnitude higher than in the commercial acoustic or electromagnetic delay lines.

The delay-to-rise time ratio, the maximum number of bits which can be stored in a *sdl* at any given tempera-

ture, and the attenuation level are a function of the voltage across the line only; Figure 3. At frequency cutoff, delay-to-rise time ratios of about 20 are obtainable with a drift bias of 100-v at room temperature. The maximum number of pulses which can be stored under the same conditions is about 6. Pulse storage per device increases directly as the square root of pulse amplitude attenuation in db due to carrier diffusion. With presently available materials, the semiconductor delay line can provide delays ranging from fractions of a microsecond to about a millisecond. Unlike the acoustic delay lines, the *sdl* has a low-pass-frequency response. For square-pulse inputs and low injection levels the output pulses are symmetrical and approach a gaussian shape for appreciable amplitude attenuation by carrier diffusion. For a given delay line and a given input pulse, the delayed pulse amplitude and rise time are functions of the delay time.

The specification of the maximum desired delay time and the minimum desired delay-to-rise time ratio at frequency cutoff are sufficient to determine the length of the delay line. The smallest feasible device cross-section is determined for a given maximum delay by the requirement that the surface recombination lifetime must be long compared to the delay time.

High resistivity materials are necessary to avoid excessive heating at the large biases at which the *sdl* normally operates. Of course, a reduction in the level of steady power dissipation means a corresponding decrease in the maximum signal level. The carrier lifetime should be long relative to the delay time. Given the delay and the corresponding delay-to-rise time ratio at frequency cutoff, the lower the ambipolar mobility, the shorter the device and accordingly the higher the power dissipation per unit volume.

Perhaps the most obvious sensor in a semiconductor delay line is a reverse biased *pn* junction. The geometry of the delay line is such, however, as to make a *pn* collector inefficient. Because of this and because the heating associated with the making of a *pn* junction leads to carrier lifetime degradation and, in high resistivity materials, to non-uniform resistivity changes, it would seem advisable to effect pulse readout through conductivity modulation. The pulse is then sensed by means of a proper arrangement of ohmic contacts on the semiconductor filament and pulse injection may be accomplished with a rectifying metal to semi-conductor contact; Figure 1. All the contacts may be made either with an ultrasonic welder or through electroplating. The complete process is simple and leaves the properties of the material unaltered.

Experimental semiconductor delay lines have been made from high-resistivity *p*-type silicon by the described technique. Delays in the 10-500  $\mu$ sec range with delay-to-rise time ratios of up to 15 have been measured in these lines at attenuations of 0-20 db. Typical dimensions of a line providing a delay of 200  $\mu$ sec, variable within  $\pm 50\%$ , would be .3 cm  $\times$  .3 cm  $\times$  3 cm.

\* Current Address: Oyster Bay, N. Y. State University of New York.

<sup>1</sup> Haynes, J. R., and Shockley, W., "Semiconductor Signal Translating Device with Controlled Carrier Transit Times," Patent 2,600,500; June 17, 1952.

<sup>2</sup> McCue, J. J. G., "Semiconductor Delay Lines," MIT Lincoln Lab. Tech. Rept. No. 179; April 15, 1958.

<sup>3</sup> Wallmark, J. T., and Marcus, S. M., "An Integrated Semiconductor Shift Register," IRE Trans. Electr. Dev., p. 350; September, 1961.

<sup>4</sup> Shockley, W., "Frequency Selective Semiconductor Circuit Elements," Patent 2,761,020; August 28, 1956.

<sup>5</sup> Levine, S. N., and Sein, J. J., "Semiconductor Bandpass Filters," IRE Internat. Conv. Rec., Part 6, p. 133; 1961.

<sup>6</sup> Kock, W. E., "Transistor Frequency Modulation," Patent 2,632,146; March 17, 1953.

<sup>7</sup> Giacoletto, L. J., "Semiconductor Frequency Converter," Patent 2,701,302; February 1, 1955.

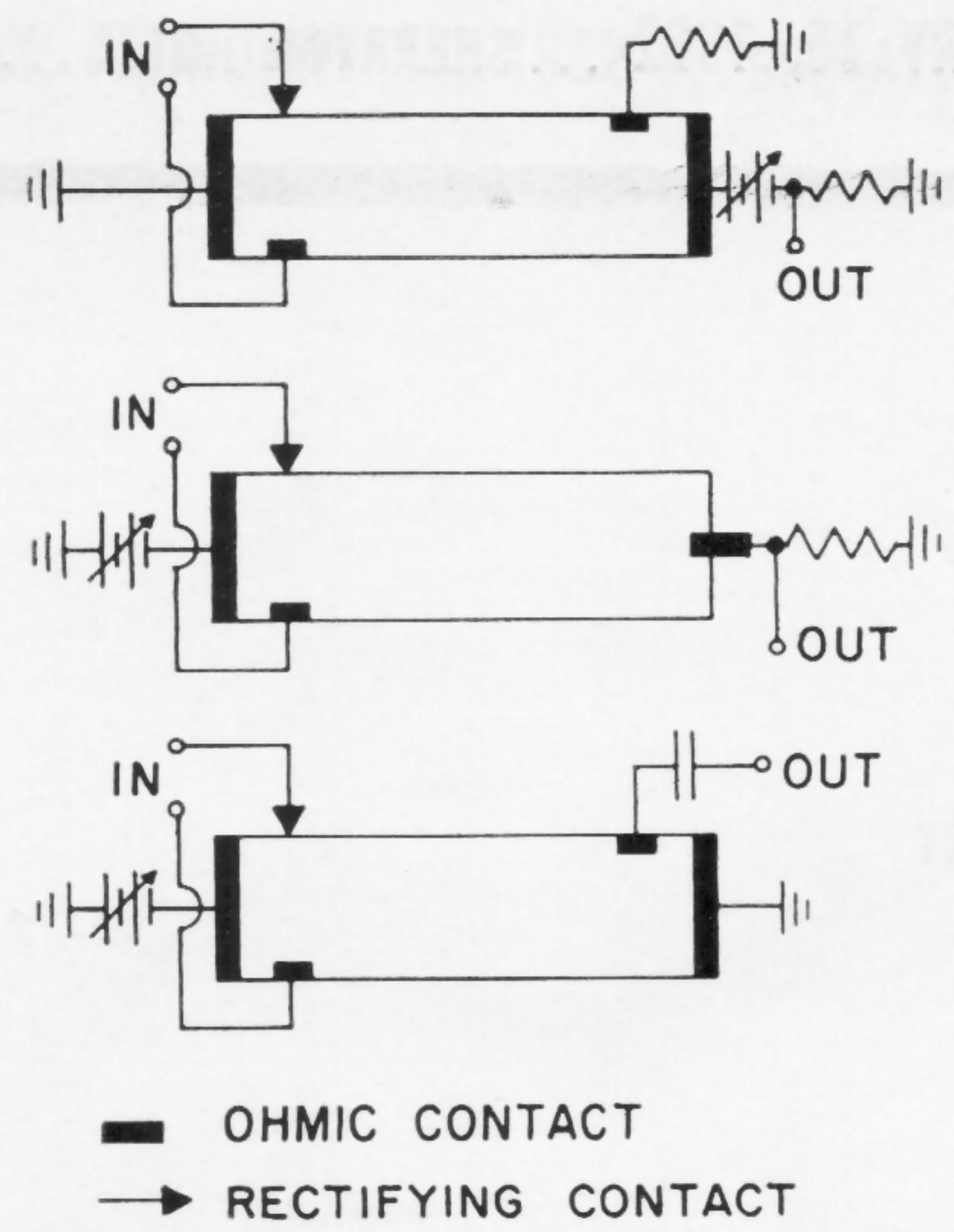


Figure 1—Semiconductor delay lines. The three lines shown differ in their method of pulse readout.

CUTOFF POINT (CP) DEFINED BY PULSE AMPLITUDE ATTENUATION OF 3 DB DUE TO CARRIER DIFFUSION.

$t$  = DELAY TIME (SEC)  
 $\Delta_c$  = DELAY TO RISE TIME RATIO AT CP  
 $f_c$  = CUTOFF FREQUENCY (CPS)  
 $t_{pc}$  = CUTOFF PULSE DURATION (SEC)  
 $N_c$  = NUMBER OF PULSES STORABLE AT CP  
 $u$  = AMBIPOLAR MOBILITY ( $\text{cm}^2/\text{volt-sec}$ )  
 $T$  = TEMPERATURE ( $^{\circ}\text{K}$ )  
 $L$  = EFFECTIVE LENGTH OF DELAY LINE (CM)  
 $V$  = VOLTAGE ACROSS  $L$  (VOLTS)

Figure 2—Definition of symbols.

#### RESPONSE TO A SQUARE PULSE:

$$t = \frac{L^2}{uV} \quad \Delta_c = 39 \sqrt{\frac{V}{T}}$$

$$t_{pc} = \frac{t}{\Delta_c} \quad N_c = \frac{1}{3} \Delta_c$$

#### RESPONSE TO A SINUSOIDAL SIGNAL:

$$f_c = 10 \frac{u}{L^2} \sqrt{\frac{V^3}{T}}$$

$$N_c = 10 \sqrt{\frac{V}{T}}$$

Figure 3—Significant relationships in the semiconductor delay line.

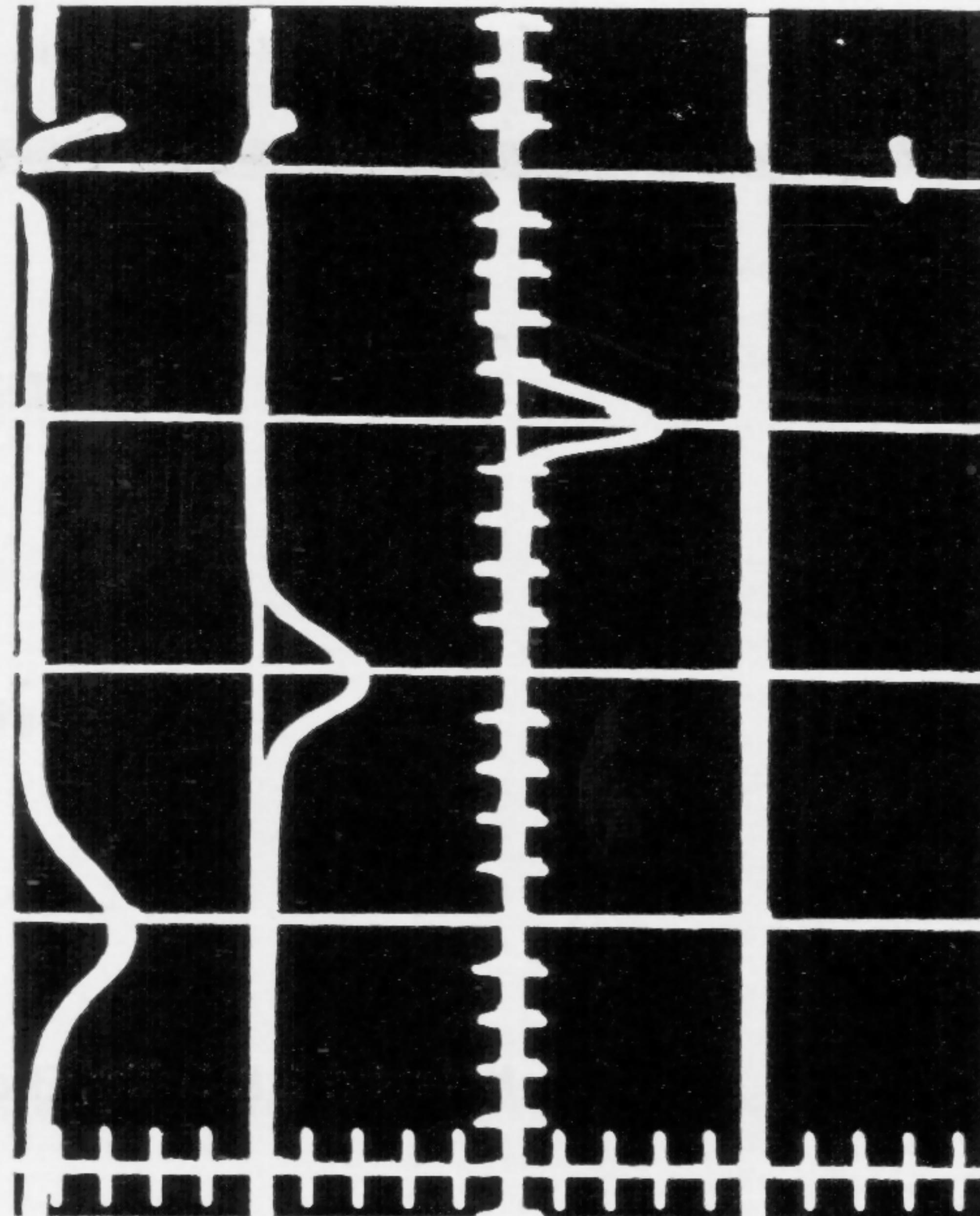


Figure 4—Typical results: Input pulse and corresponding delayed pulse as a function of delay; vertical scale different for each trace. Vertical scales: 2, 1, .5, .2 v/sq. Horizontal scale: 100  $\mu\text{sec}/\text{sq}$ .

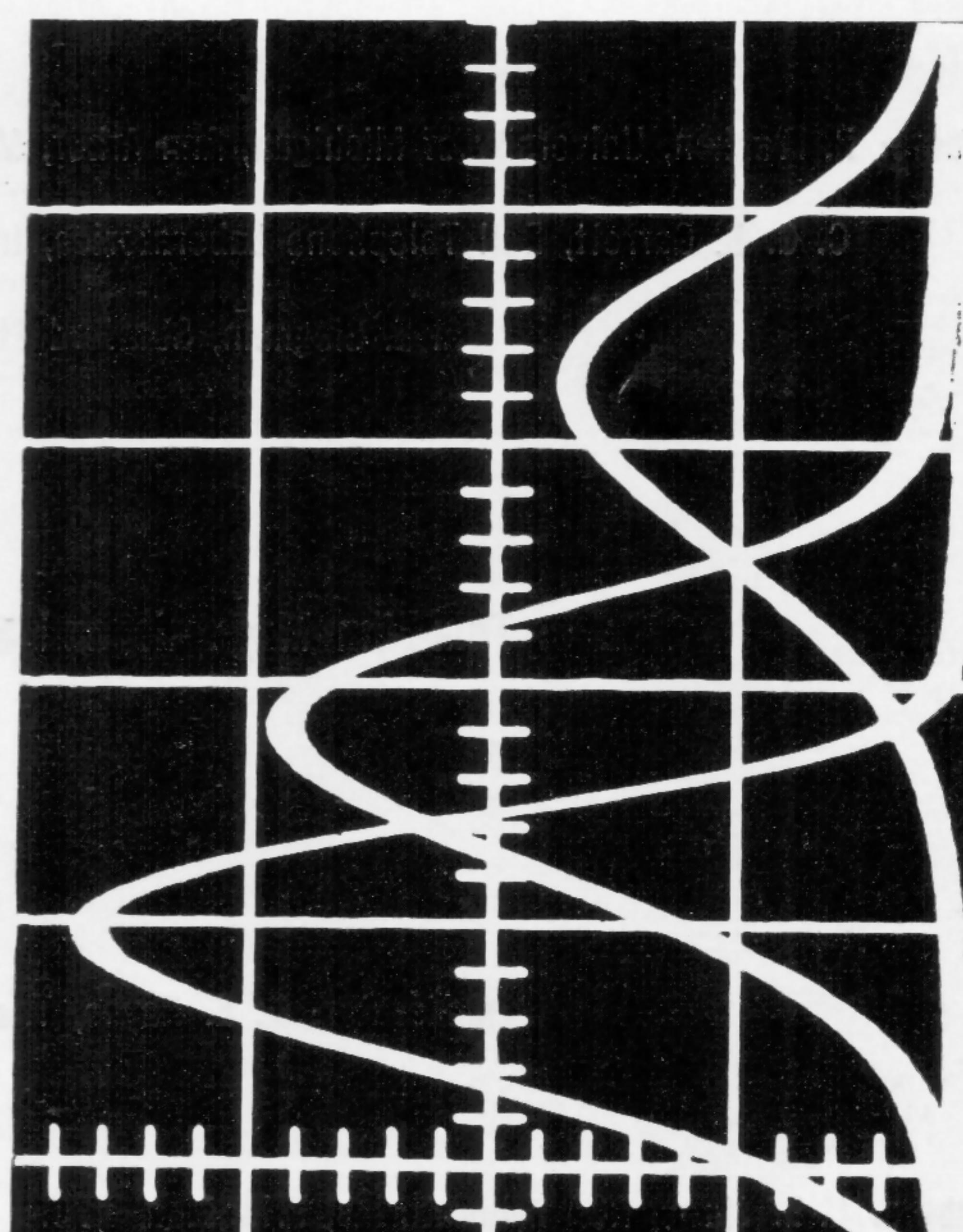


Figure 5—Shape of delayed pulse as a function of the voltage across the line. Delays of 240, 285, 350  $\mu\text{sec}$  corresponding to biases of 48, 41, 33 v, respectively. Vertical scale is .05 v/sq; horizontal scale, 50  $\mu\text{sec}/\text{sq}$ . Input is a 3-v, 30  $\mu\text{sec}$  square pulse.

### Informal Discussion Sessions

#### TE 7: Nanosecond Circuitry

*[West Ballroom]*

**Moderator:** E. P. Stabler, Electronics Lab., General Electric Co., Syracuse, N. Y.

**Panel Members:** B. J. Lechner, RCA, Camden, N. J.

J. R. Turnbull, IBM Corp., Poughkeepsie, N. Y.

W. Peil, Electronics Lab., General Electric Co., Syracuse, N. Y.

C. N. Winningstad, Tektronix, Inc., Beaverton, Ore.

W. M. Goodall, Bell Telephone Laboratories, Inc., Holmdel, N. J.

W. F. Chow, Remington Rand, Sperry Rand Corp., Philadelphia, Pa.

D. Berry, Electronics Lab., General Electric Co., Syracuse, N. Y.

M. M. Kaufman, RCA, Camden, N. J.

#### TE 8: Optical Masers

*[East Ballroom and Assembly]*

**Moderator:** R. H. Kingston, MIT Lincoln Laboratory, Lexington, Mass.

**Panel Members:** P. Franken, University of Michigan, Ann Arbor, Mich.

C. G. B. Garrett, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

A. E. Siegman, Stanford Electronics Lab., Stanford University, Stanford, Calif.

H. Scharfman, Raytheon Company, Waltham, Mass.

M. L. Stitch, Hughes Aircraft Co., Malibu, Calif.

#### TE 9: Thin-Film Magnetic and Superconductive Techniques in Future Computers

*[Pennsylvania West]*

**Moderator:** R. E. Hayes, The Plessey Co., Ltd., Romsey, Hampshire, England

**Panel Members:** L. L. Burns, RCA Laboratories, Princeton, N. J.

M. L. Cohen, A. D. Little, Inc., Cambridge, Mass.

A. E. Slade, A. D. Little, Inc., Cambridge, Mass.

D. R. Young, IBM Corp., Poughkeepsie, N. Y.

### Informal Discussion Sessions

#### TE 10: Low-Level Signal Processes

*[Pennsylvania East]*

**Moderator:** D. Hilbiber, Fairchild Semiconductor, Div. Fairchild Camera and Instrument Corp., Palo Alto, Calif.

**Panel Members:** R. D. Middlebrook, California Institute of Technology, Pasadena, Calif.

G. S. Bahrs, Vidar Corp., Sunnyvale, Calif.

B. W. Fuller, Redcor Development Corp., Canoga Park, Calif.

J. A. Ekiss, Philco Corp., Lansdale, Pa.

#### TE 11: High-Power, High-Speed Switching

*[Independence-Constitution]*

**Moderator:** R. Bieselle, Shockley Transistor, Palo Alto, Calif.

**Panel Members:** H. Hurd, Stanford Radiation Lab., Stanford University, Stanford, Calif.

C. Fisher, Signal Corps Laboratory, Ft. Monmouth, N. J.

J. M. Goldey, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

C. E. Smith, Texas Instruments, Inc., Dallas, Tex.

SESSION IX: Functional Components

Chairman: T. O. Stanley

RCA Laboratories Division, RCA, Princeton, N. J.

FM 9.1: Photoconductor-Electroluminescent Display Panels on Fotoform Glass\*

Z. Szepesi

Westinghouse Electric Corporation  
Elmira, N. Y.

THE PRINCIPAL ELECTROOPTICAL characteristics of the *pc-el* display panels can be derived from the basic circuit, which consists of the series connection of a *pc* and an *el* element; Figure 1a. The simplest realization of a *pc-el* display panel is the sandwich construction as shown in Figure 1b. In building such a sandwich panel difficulties arise from the requirement of satisfying an impedance relation between the *pc* and *el* components, and the simple sandwich construction does not give satisfactory characteristics with standard *pc* and *el* layers. Many different structure designs have been suggested<sup>1</sup>, one of which proposed a construction<sup>2-3</sup>, where *Fotoform* glass plates<sup>†</sup>, could be advantageously used. This material is an ideal substrate for this construction because it offers an easy way to make a mosaic of regularly spaced holes on a glass plate and also because it is possible to build an opaque pattern into the glass plate. This construction enables the separation of the *pc* and *el* layers and hence *pc* elements with lateral electrodes can be used. These lateral cells have the necessary low capacitance and the impedance relation is easily satisfied. The display panel in this construction is built mosaicwise according to the hole pattern. Around every hole there is a *pc* cell on one side of the plate and a corresponding *el* cell on the other side. They are connected in series through the hole. Opaque *Fotoform* glass can be used for image intensifiers and white *Fotoform* glass with a lattice of opaque lines between the elements is ideal for storage display panels.

We have built both image intensifiers and storage panels using this construction. An evaporated *CdS* layer was used for the *pc* component and plastic embedded *ZnS* for the *el* layer. The resolution of the panels was 14 or 16 elements per-linear-inch. The different fabrication steps are:

- (1)—The *Fotoform* glass plate, with the appropriate mosaic of holes, is completely coated (both sides and holes) with a transparent conductive layer of tin oxide (*NESA*).
- (2)—An electrode pattern is etched out on both sides (as shown on Figure 2), with a photographic-chemical method.
- (3)—*CdS* is evaporated in high vacuum on the *pc* pat-

tern side and sensitized by *CdCl<sub>2</sub>* and *CuCl<sub>2</sub>* diffusion at around 500° C.

- (4)—The *el* layer is sprayed on the other side of the *Fotoform* glass and a semitransparent Au electrode layer is evaporated in high vacuum on the top of the *el* layer.

The requirements for the characteristics of the *pc* and *el* layers for the image intensifier are different from those for the storage panel. A low slope in the current-light intensity relation of the *pc* layer and in the brightness-voltage relation of the *el* layer is desirable for the image intensifier, but a high slope in both characteristics is required for the storage panel. By different sensitizing processes, photolayers with sublinear and superlinear current versus light-intensity dependence were prepared on the *Fotoform* substrate as shown in Figure 3. The characteristics of the *el* layers—one with a low, the other with a high slope<sup>4</sup>—are shown in Figure 4.

Figure 5 shows the characteristics of an image-intensifier panel which had a resolution of 16 elements-per-linear inch and a size of 1" x 1". Similar intensifier panels have been made with a maximum luminous gain of 170.

Due to the relatively loose tolerances with which the *Fotoform* glass plates can be fabricated, the size and the resolution of these panels were limited to 4.6 inches square and 16 elements-per-inch, respectively. Other difficulties were caused by the poor reproducibility of the *Fotoform* glass. The incomplete control in the manufacturing and processing of these plates gave rise to poor reproducibility of the *pc* characteristics, because they are highly influenced by the composition of the substrate. If *Fotoform* glass could be made with more reproducible characteristics, the described construction would become an excellent solution for building low-resolution display panels.

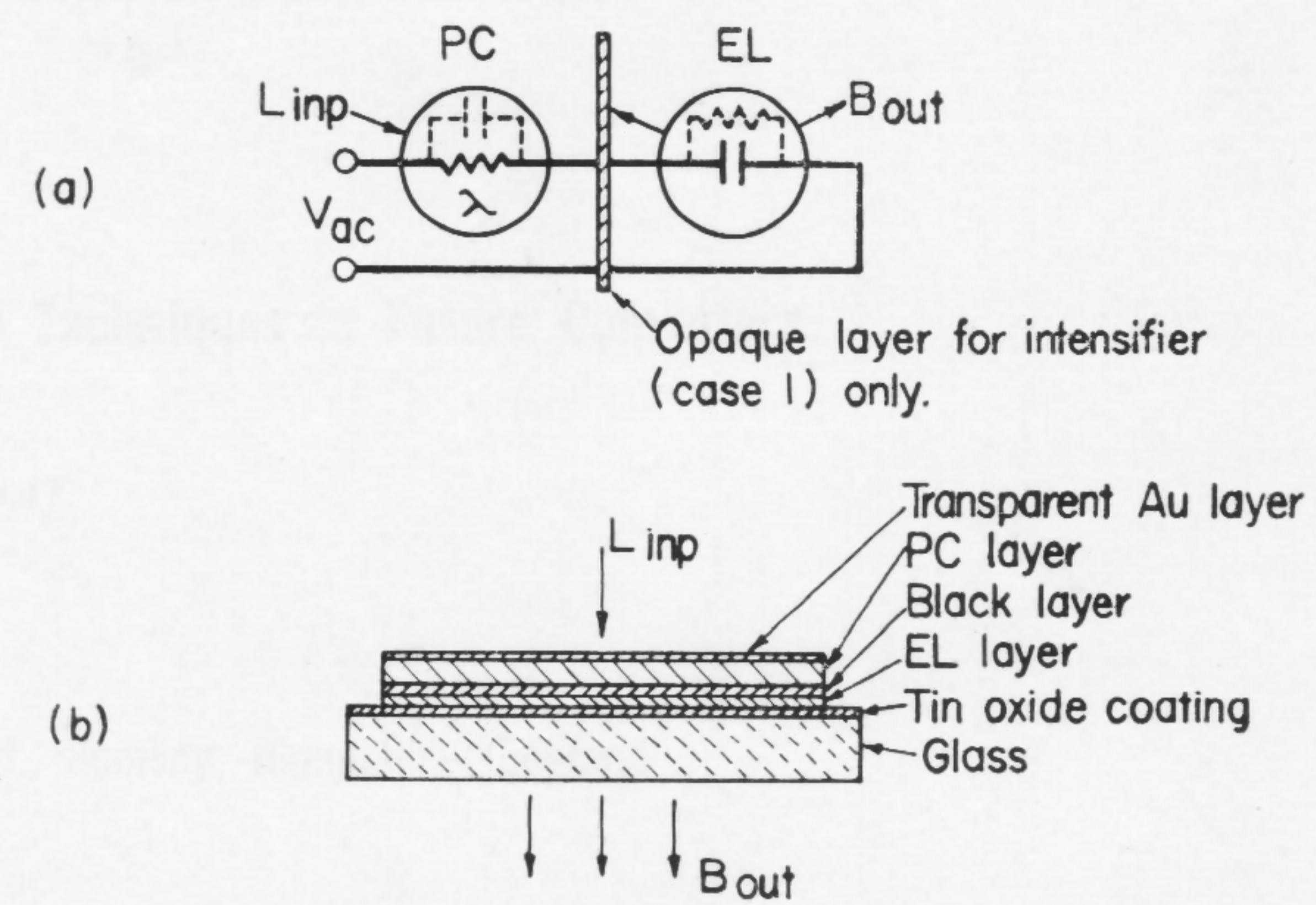


Figure 1—(a)—Basic circuit of *pc-el* display panels: Case 1—light barrier between *pc* and *el*—light intensifier; case 2—light feedback from *el* to *pc* cell—bistable or storage element. (b)—Sandwich type construction of *pc-el* display panels. Black layer is continuous for image intensifier and is in cross-grid pattern for storage panels.

\* Work on image intensifier panels supported by the U. S. Naval Training Device Center, Port Washington, N. Y., under contract No.: N61339-562. Storage display panel work supported by Canadian Westinghouse Co., Ltd., Hamilton, Ontario, Canada. Subcontract under prime contract No.: AF-30(635)14382, Rome Air Development Center.

† Corning Glass.

<sup>1</sup> Josephs, J. J., "A Review of Panel Type Display Devices," *Proc. IRE*, vol. 48, p. 1380-1395; 1960.

<sup>2</sup> Rosenthal, J. E., "Theory and Experiments on a Basic Element of a Storage Light Amplifier," *Proc. IRE*, vol. 43, p. 1882-1888; 1955.

<sup>3</sup> Evans, H. J., "Display Device with Storage," Patent No. 2,920,232; Jan. 5, 1960.

<sup>4</sup> Ivey, H. F., and Thornton, W. A., "Preparation and Properties of Electroluminescent Phosphors for Display Devices," *IRE Trans. Electron Dev.*, ED8, p. 265-279; 1961.

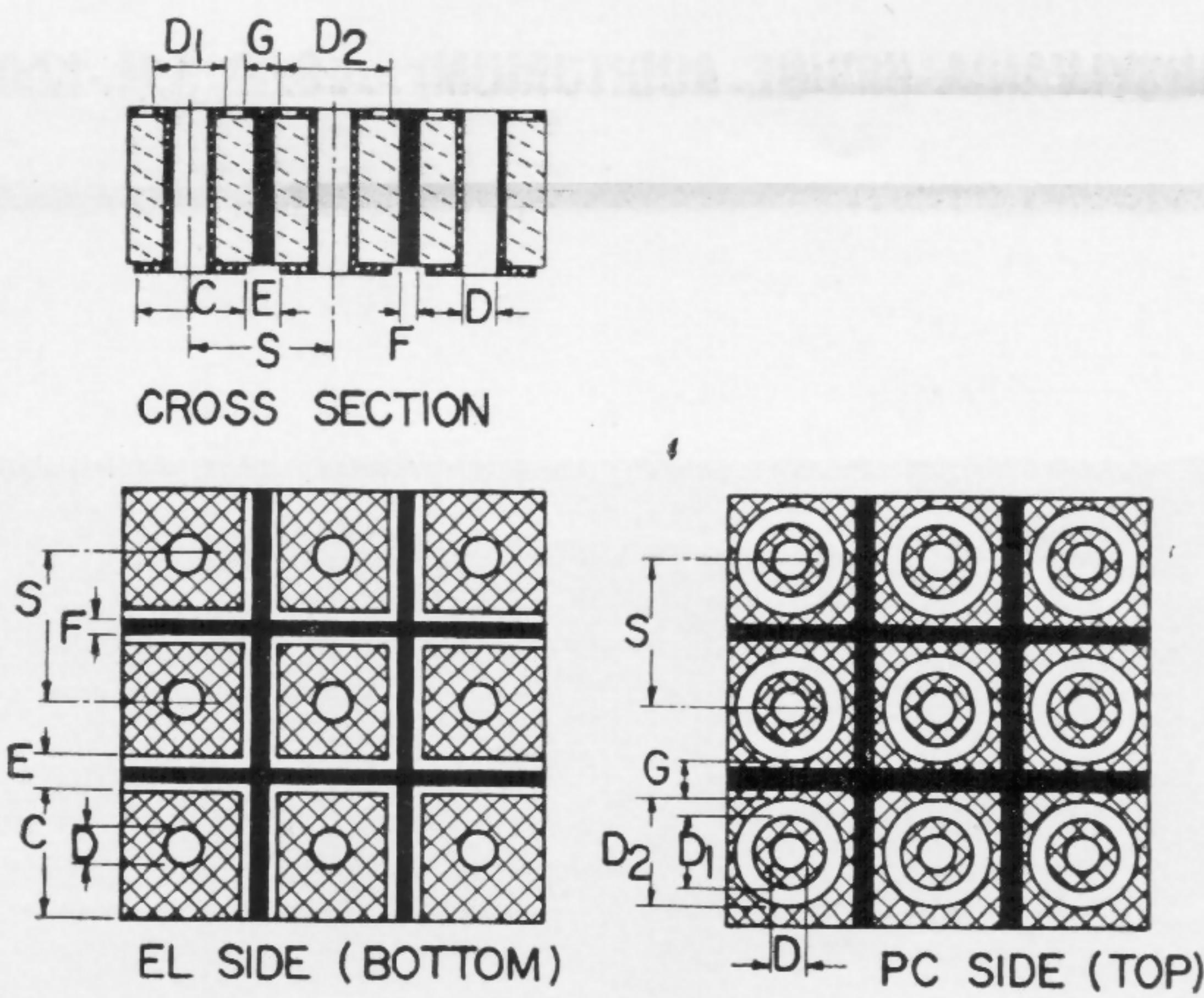


Figure 2—Fotoform substrate, showing the conductive electrode patterns on both sides. The layers and areas with crossed lines are transparent conductive coatings (tin oxide).

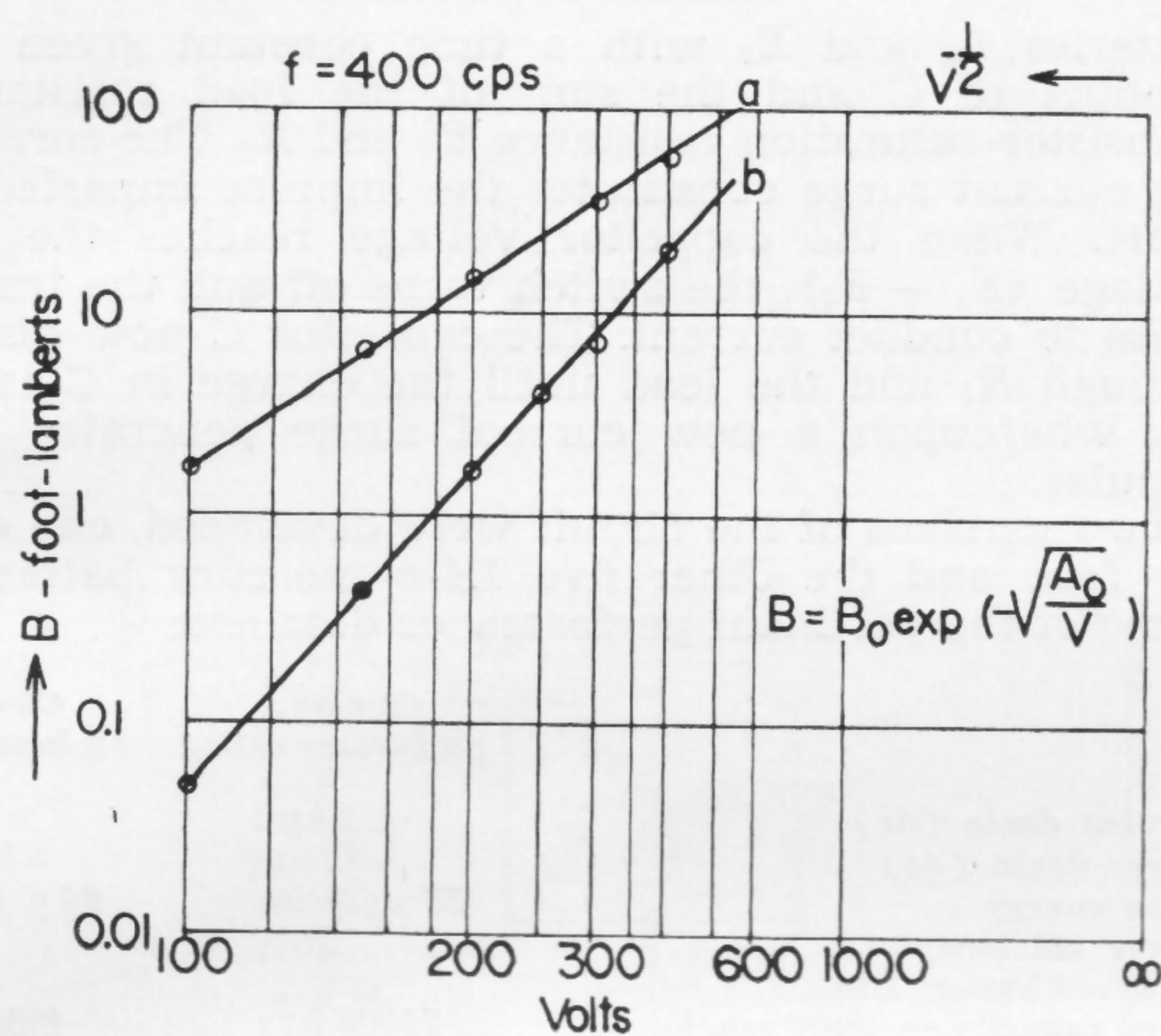


Figure 4—Brightness versus voltage curves of *el* layers: (a)—Low-slope phosphor\*\* for image intensifier; (b)—high-slope phosphor\*\*\* for storage display panel. Brightness measured through Au layer of 64% transmission.

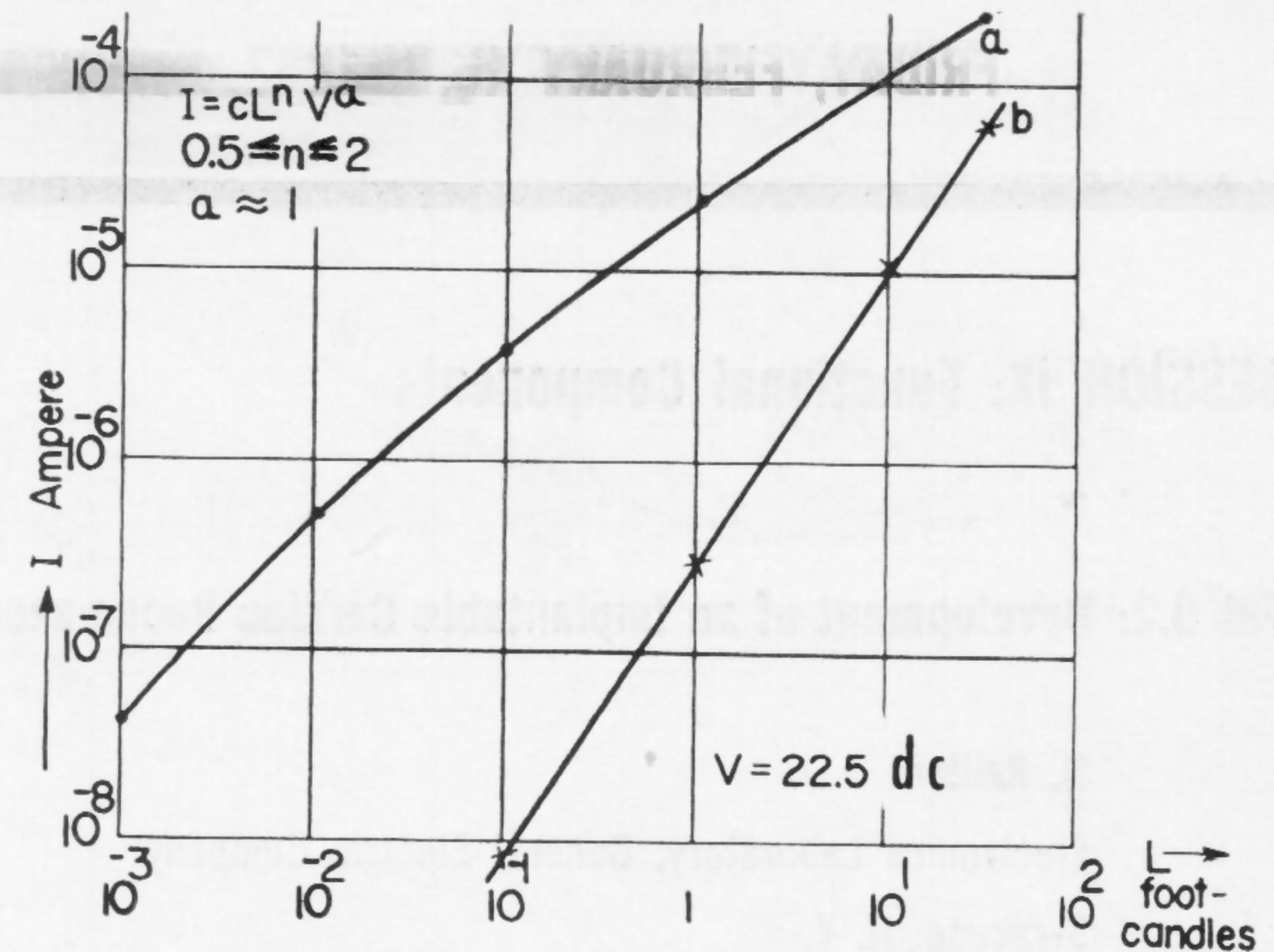


Figure 3—Current versus light-intensity curves of evaporated CdS layers of *pc* elements on *Fotoform* panel: (a)—Sublinear cell for image intensifier; (b)—superlinear cell for storage display panel.

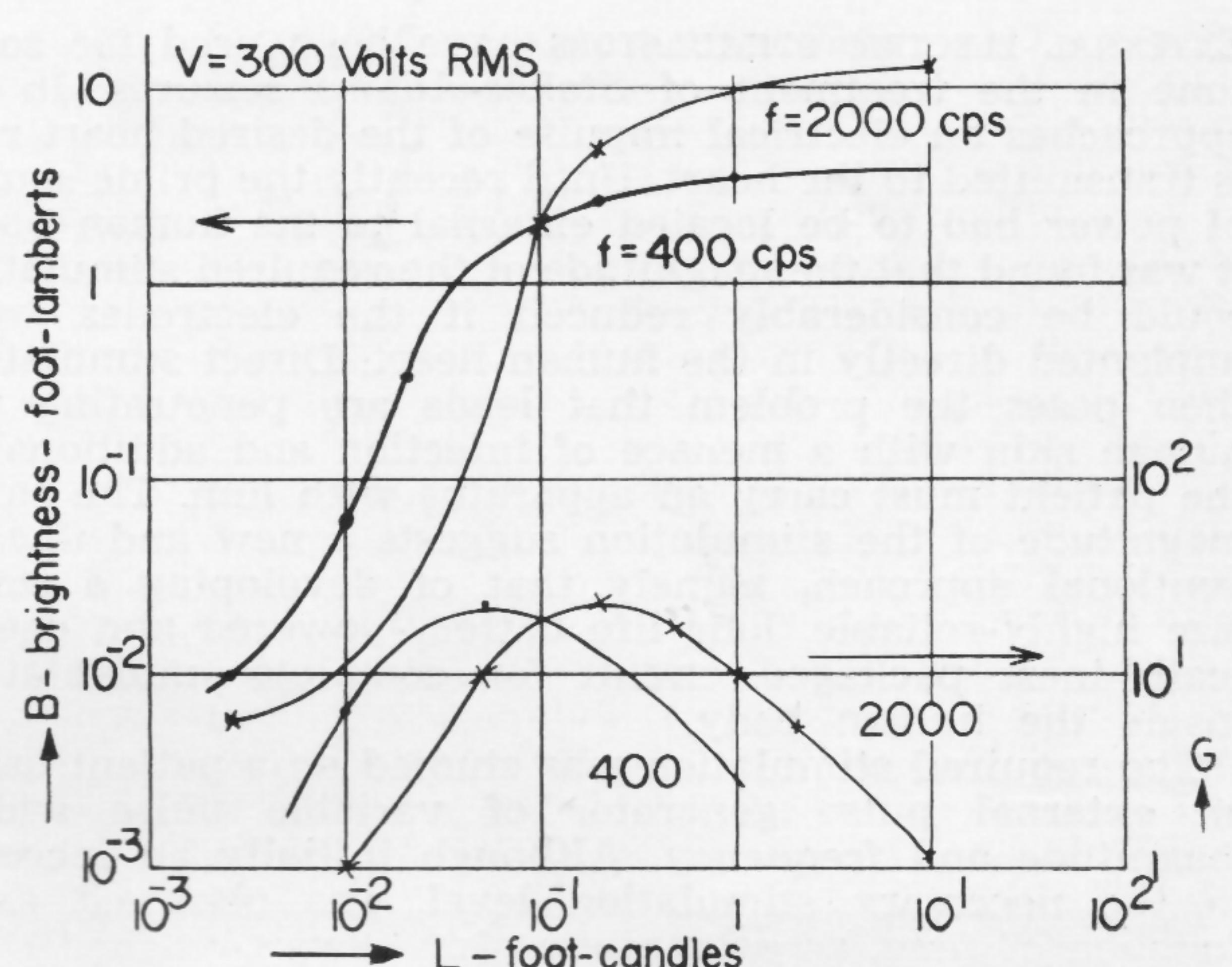


Figure 5—Typical brightness output versus light-intensity input curves and luminous gain of an image-intensifier panel.



Figure 6—Photograph of a 4.6-inch square storage display panel with 64 x 64 elements. Resolution 14 elements-per-inch. Character written by projecting the image from a photographic slide.



Figure 7—Same panel as Figure 6, with characters written by an *el* x-y panel activated by 10-msec long electric pulses; writing time of a character is 80-msec.

\*\* WL-2019. \*\*\* WL-1658.

## SESSION IX: Functional Components

## FM 9.2: Development of an Implantable Cardiac Pacemaker\*

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Syracuse, N. Y.

EXTERNAL ELECTRIC STIMULATORS have been used for some time in the treatment of Stokes-Adams seizures. In all approaches an electrical impulse of the desired heart rate is transmitted to the heart. Until recently the prime source of power had to be located external to the human body. It was found that the magnitude of the required stimulation could be considerably reduced if the electrodes were implanted directly in the human heart. Direct stimulation then poses the problem that leads are penetrating the human skin with a menace of infection and additionally, the patient must carry an apparatus with him. The small magnitude of the stimulation suggests a new and unconventional approach, namely that of developing a small size highly-reliable, long-life battery-powered and chemically-inert packaged circuit for complete implantation inside the human body.

The required stimulation was studied on a patient using an external pulse generator of variable pulse width, magnitude and frequency. Although initially an increase in the necessary stimulation level was observed as a function of time, an asymptotic plateau was reached after several months. Under such a time-invariant condition, the voltage and current thresholds were studied in detail for generator pulse widths ranging from .3 to 7 msec. A typical response pattern is shown in Figure 1. It appears that the heart load impedance is approximately equivalent to a series network of a 20- $\mu$ f capacitance and 300-ohms resistance. In addition, the average current, rms current, charge and energy for each pulse width were determined. Of these, it was found that the only quantity which is fairly constant and showing only a somewhat random dependency on pulse width is the energy delivered to the load as shown in Figure 2. The stimulation threshold appears to be approximately 15 $\mu$  joules-per-pulse. This result is in substantial agreement with the findings of others<sup>1</sup>.

Based on the preceding information, construction of a small-size reliable pulse oscillator was considered. The basic configuration found suitable for this purpose is shown in Figure 3. Its operation may be summarized as follows: When the capacitor C is completely discharged, the transistor configuration becomes regenerative and acts as a closed switch. The capacitor C is charged from

\* The work described represents a joint effort of the Surgical Research Division of Maimonides Hospital, Brooklyn, N. Y. and the Electronics Laboratory, General Electric Company, Syracuse, N. Y.

<sup>1</sup> Chardack, W. M., Gage, A. A., and Greatbatch, W., "Experimental Observations and Clinical Experiences with the Correction of Complete Heart Block by an Implantable Self-Contained Pacemaker," *Trans. Am. Soc. for Artificial Internal Organs*, vol. 8, p. 286; 1961.

batteries  $E_1$  and  $E_2$  with a time constant given by the product of C and the sum of the load resistance  $R_L$ , transistor-saturation resistance  $R_S$  and  $R_3$ . The corresponding current surge constitutes the impulse imparted to the heart. When the capacitor voltage reaches the battery voltage ( $E_1 + E_2$ ), the switch turns off and the transistors cease to conduct current. The capacitor C now discharges through  $R_1$  and the load until the charge in C is almost nil, whereupon a new current surge generates another impulse.

Two versions of the circuit were developed, one employing four and the other five 1.4-v mercury battery cells. Some of the pertinent performance data are:

	Circuit A (4 battery cells)	Circuit B (5 battery cells)
Current drain (dc)	14 $\mu$ A	25 $\mu$ A
Power drain (dc)	82 $\mu$ W	184 $\mu$ W
Pulse energy	23 $\mu$ joules	64 $\mu$ joules
Power efficiency	30%	38%
Expected battery life:		
Rated capacity — 1000 ma/hr	71000 hrs	40000 hrs
Packaged volume	2.4 in <sup>3</sup>	4 in <sup>3</sup>

Typical current and voltage waveforms as generated by a five-cell pacemaker circuit are shown in Figure 4. The circuit is potted in epoxy and hermetically sealed in teflon which is chemically inert to body fluids. It has been successfully installed in a surgical procedure in several patients suffering from heart block.

The circuit of Figure 3 is pulsing at a fixed rate. It does not require care or maintenance during its life-time. No patient has complained of any discomfort from the presence of the circuit inside the body.

As an optional addition, there has also been developed an external rate-control circuit which permits acceleration of the pulse rate if an increased cardiac output is required. This circuit employs a *pnpn* complementary transistor configuration connected in a relaxation oscillator mode similar to the implantable circuit described. Generated is a sharp current pulse which energizes an induction coil and thus triggers the internal circuit magnetically. The rate of the trigger may be varied by approximately 5:1. The minimum and maximum rate of an operational circuit may be adjusted by selecting two resistors. With a variable resistance, continuous external rate control between the limits is then possible. The flat induction coil has a diameter of 3.5" and is connected to the circuit by a 15" long cable. This arrangement permits the patient to attach the coil to the skin close to the internal pacemaker. The area of the coil is considerably larger than that of the internal unit, permitting the two units to be placed up to 1.5" off center.

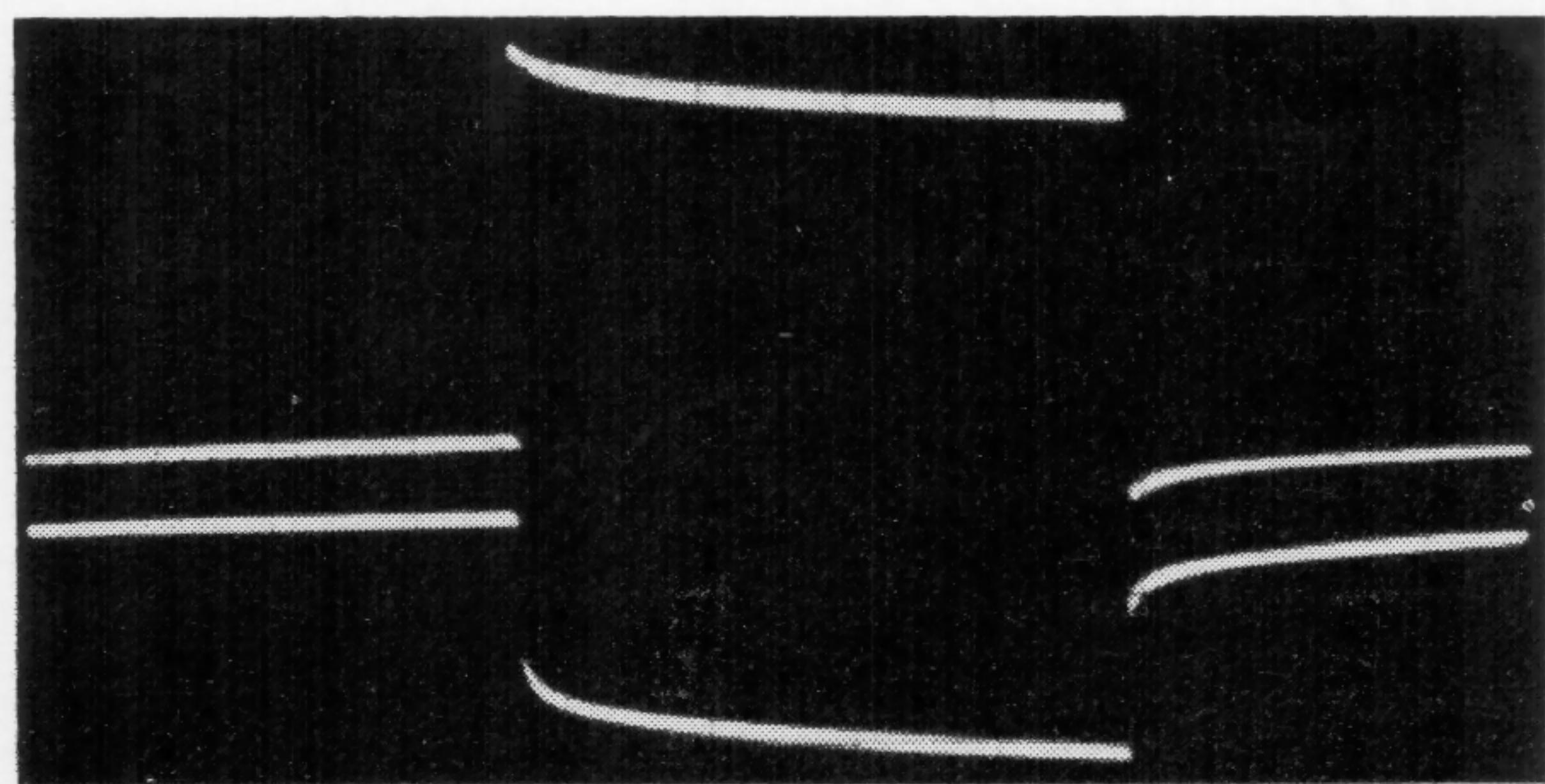


Figure 1—Typical pulse response of human heart: Pulse width—2 msec; scales—1-v/div (top), and 2-ma/div (bottom).

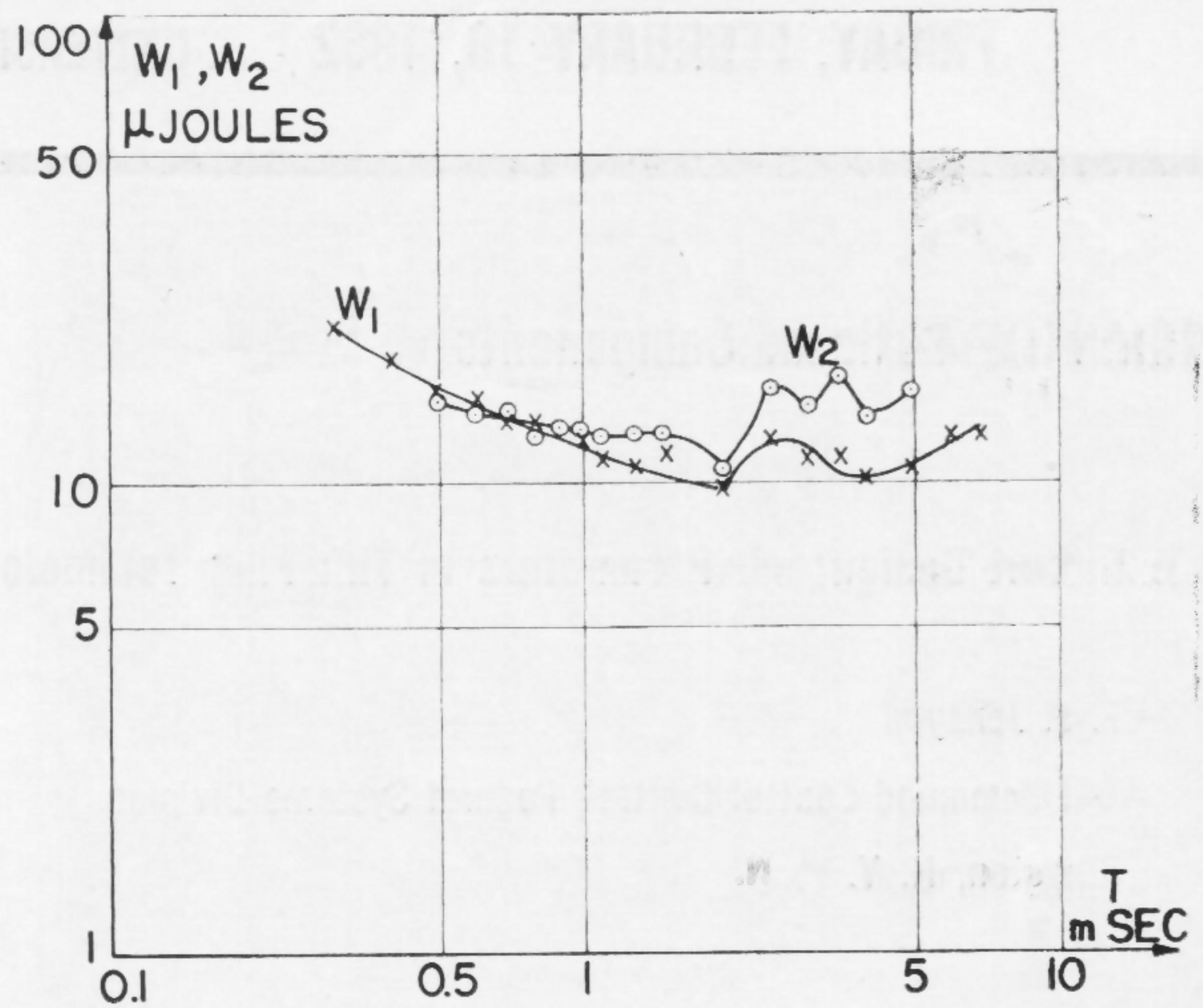


Figure 2—Pulse energies  $W_1$  and  $W_2$  as a function of pulse width  $T$  where

$$W_1 = \int_0^T I^2 R dt ; R = 300 \text{ Ohms}$$

$$W_2 = \int_0^T V I dt$$

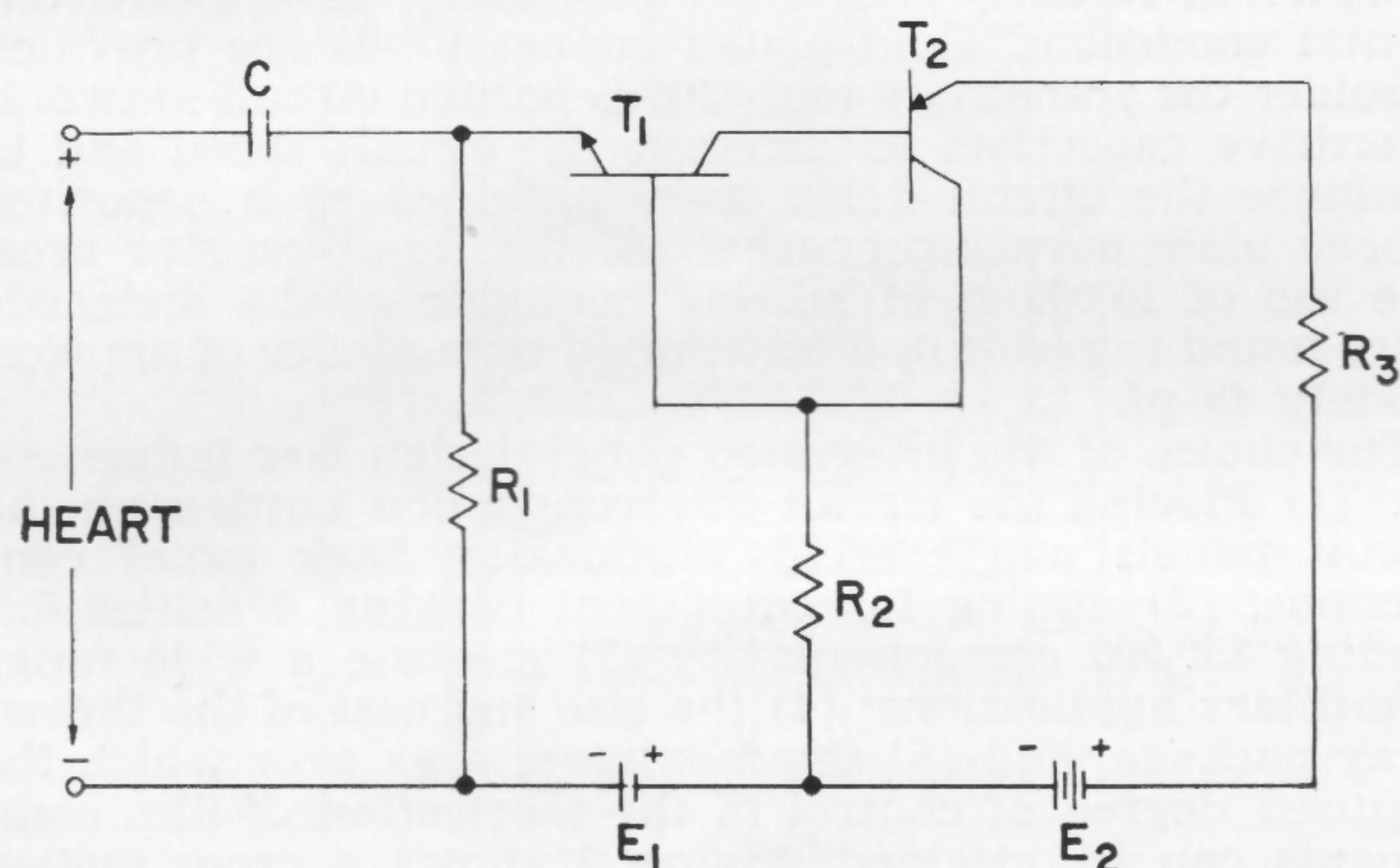


Figure 3—Implantable pacemaker circuit.

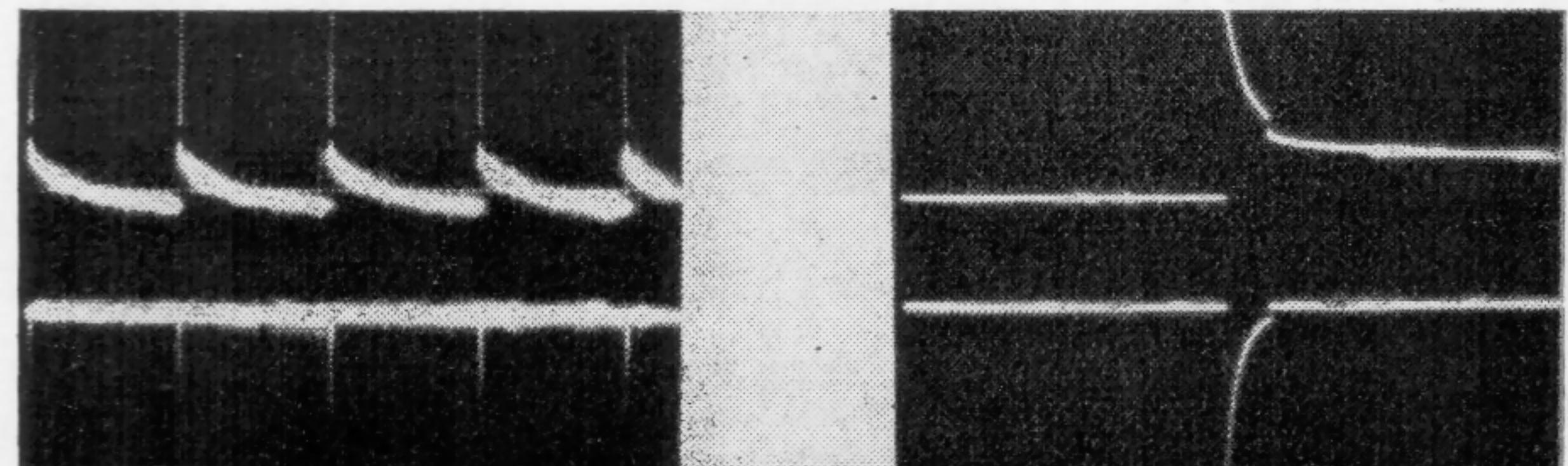


Figure 4—Response of human heart to pacemaker pulse: Scales—1-v/div (top traces); 5 ma/div (bottom traces); .5 msec/div (left), and 10 msec/div (right).

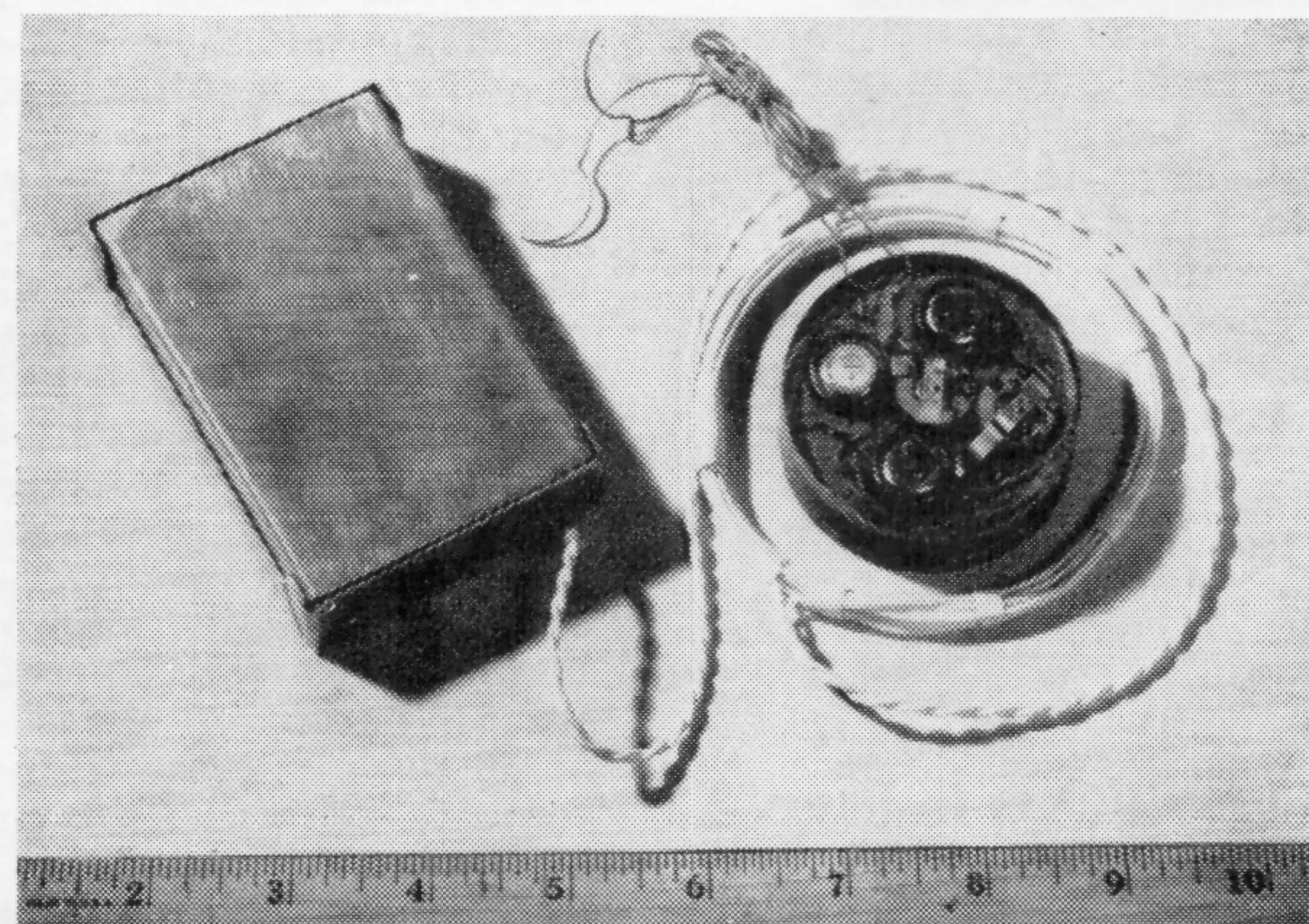


Figure 5—Photo of a 5-cell pacemaker and rate-control circuit.

## SESSION IX: Functional Components

### FM 9.3: Circuit Design and Parameters in Thin-Film Technology\*

F. F. Jenny

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THE TECHNOLOGY of thin-film electronics is aimed at a reduction of the physical size and production costs of electronic equipment as well as at increased reliability and improved performance. This paper will show how complex logic functions can be obtained by integrating many thin-film circuits of one type at the panel level. This can be accomplished by altering the thin-film interconnection pattern from panel to panel, while retaining the basic circuit configuration throughout. Familiar design techniques for lumped parameter networks can be utilized. The design of an integrated thin-film panel will also be described.

To reduce fabrication costs and improve reliability, the basic circuit of the integrated thin-film panel must use a minimum number of non-deposited components, such as transistors and diodes. In addition, microminiature-packing densities require the circuit to dissipate power in the low milliwatt range and utilize resistors and capacitors that are restricted in value. Transistor-resistor logic (*trl*) employing the *NOT-OR* (*NOR*) function was chosen as the basic circuit of the integrated thin-film panel because it fulfills all or most of the foregoing criteria.

Having selected the basic circuit configuration, ground rules governing the circuit design were formulated. These ground rules required that the circuit have a usable fan-in and fan-out, a minimum power dissipation, component values that are attainable with thin films, and maximum allowable circuit tolerances. Since power dissipation and ohms per square of the resistor material determine the physical size of resistors, it was necessary to consider only resistor values below 10,000 ohms to achieve a high degree of microminiaturization and reliability.

The selection of a transistor was determined by military environmental requirements and by the desire for an essentially planar packaging technique. A commercially-available silicon transistor was chosen as the most compatible device available because it is packaged in a microminiature hermetically-sealed can and has planar flat leads.

An electronic data processing system† was utilized to aid in the circuit design. The computer was programmed to consider all possible combinations of a *worst-case* end-of-life design and to print out the solutions to the various combinations which gave usable results. From these printouts, the circuit arrangement having the most appropriate combinations of resistors, resistor tolerances, and transistor specifications was utilized. Figure 1 shows the basic circuit derived from the computer program. The most important circuit design results were:

- (1)—Resistors:  $R_1 = 4000$  ohms;  $R_2 = 1000$  ohms
- (2)—Fan-in: 3; fan-out: 3
- (3)—One power supply:  $+6$  v  $\pm 4\%$
- (4)—Typical power dissipation: 40 mw
- (5)—Temperature operational range:  $0-100^\circ\text{C}$
- (6)—Transistor-silicon:  $B_{min}$  of 40

The variation in the thin-film resistance value is largely a function of the distribution of the evaporated resistance

\* The work reported in this paper was performed, in part, under U. S. Signal Corps Contract Number DA 36-039-sc-87246.

† IBM. \*\* Corning Glass.

material over a panel area as well as of panel-to-panel fabrication variations. Resistors in the same circuit normally have nearly identical values due to their close proximity. Although resistors in driving and driven circuits were permitted to have a  $\pm 15\%$  variation of the nominal value, the resistors within any one circuit were designed to only a total of 15% variation between them.

The topological layout of the circuit is shown in Figure 2. The resistors used are fabricated from a cermet material (a silicon-monoxide-chromium mixture) which has shown exceptional stability and uniformity under severe environmental conditions. Gold-plated copper lands are provided to solder the transistors onto the deposited circuit network. Overdrive capacitors to increase the circuit speed and to minimize the circuit delay were provided by a deposited copper plate covering one-half of the input resistor area. The use of  $10,000 \text{ \AA}$  of silicon monoxide as the dielectric were found to result in a distributed capacitance of approximately 40 pf.

The choice of the integrated panel design was influenced by: (1) Placing the circuit interconnection burden on the circuit panels and thereby minimizing back panel connections; (2) aiming for equipment packing densities exceeding 850,000 components/ft<sup>3</sup>; (3) meeting a wide range of military applications; (4) the size and cost of the throw-away package; and (5) the maximum area over which the required degree of control in the fabrication of film components can be attained. Figure 3 shows a cross section of the standard panel layout utilizing a 2.5" x 3.5" x .040" *pyrex*\*\* substrate containing 28 pairs or 56 identical *trl-NOR* circuits. Such logic arrangements as a 6-input *NOR* block, a trigger, shift-register stage, serial adder, as well as nonlogical drivers, have been derived by appropriate interconnection of the basic *trl-NOR* circuits. Between each row and column of the 28 circuit pairs, appropriate spacing has been reserved for four horizontal and six vertical 10-mil-wide intercircuit copper conductors (1.7 ohms/inch) spaced on 25-mil centers. The lower edge of the integrated film panel contains 44 silk-screened silver lands spaced on 75-mil centers suitable for insertion into specially-designed connectors.

To demonstrate the feasibility of fabricating an integrated film assembly, a logic test vehicle (integrated counter assembly) was designed; utilized was the 56 *trl-NOR* panel design shown in Figure 4. A 4-stage binary counter was selected as a representative example of computer logic and circuit interconnection complexity. Three panels of this type have been fabricated thus far and used to evaluate the electrical performance (Figure 5) of the individual film circuits, as well as the overall performance of the electronic assembly. The maximum *prf* of the *NOR* blocks is 2.5 Mc. The turn-on and turn-off delays of the basic *NOR* block are 40 nsec with rise and fall transition of 50 nsec. After a complement signal has been received, the delay through a binary trigger stage is 70- to 100-nsec. With the present degree of control achieved in the fabrication process, 224 cermet resistors are being deposited to

[Continued on page 106]

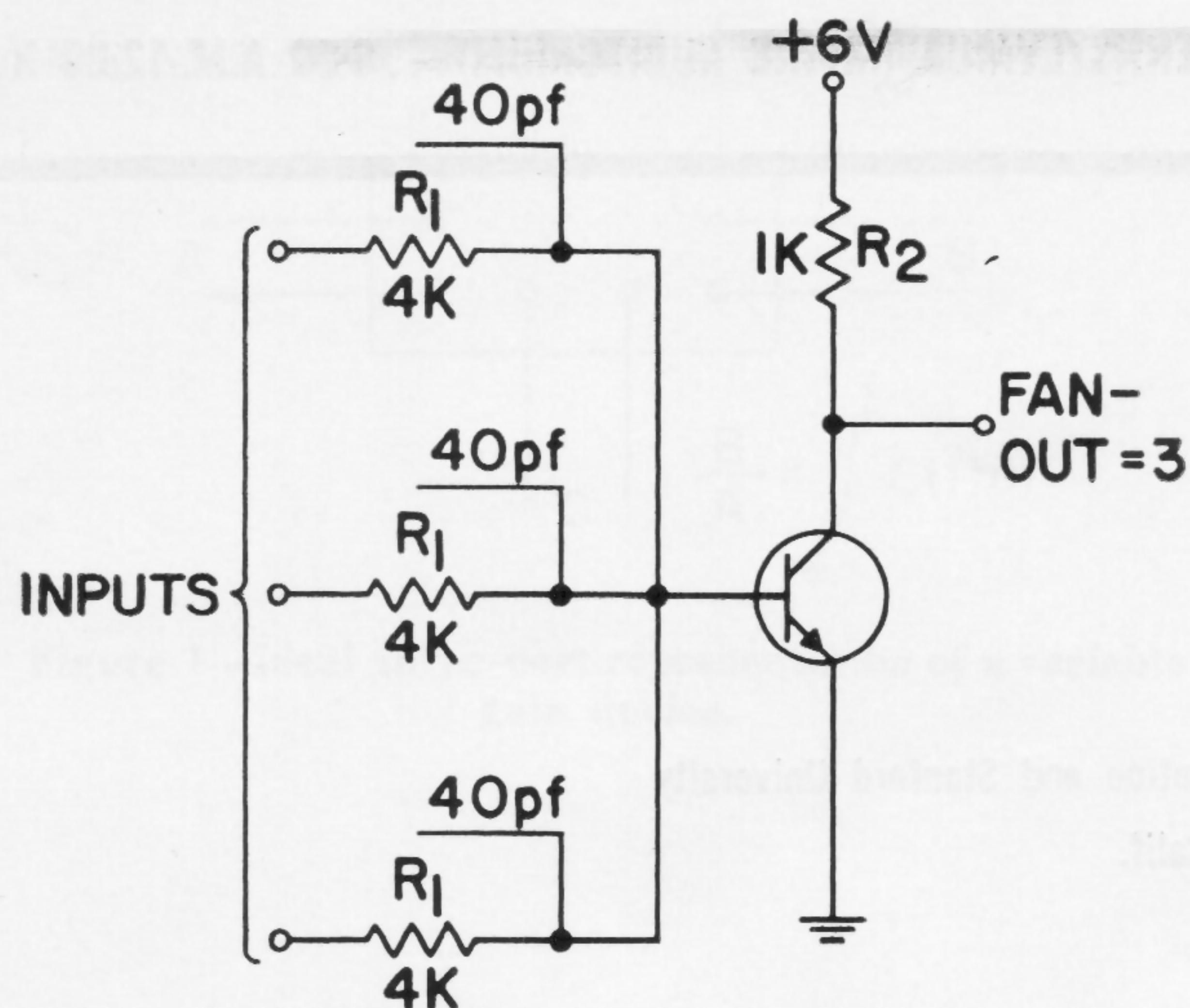


Figure 1—The *trl-NOR* basic circuit.

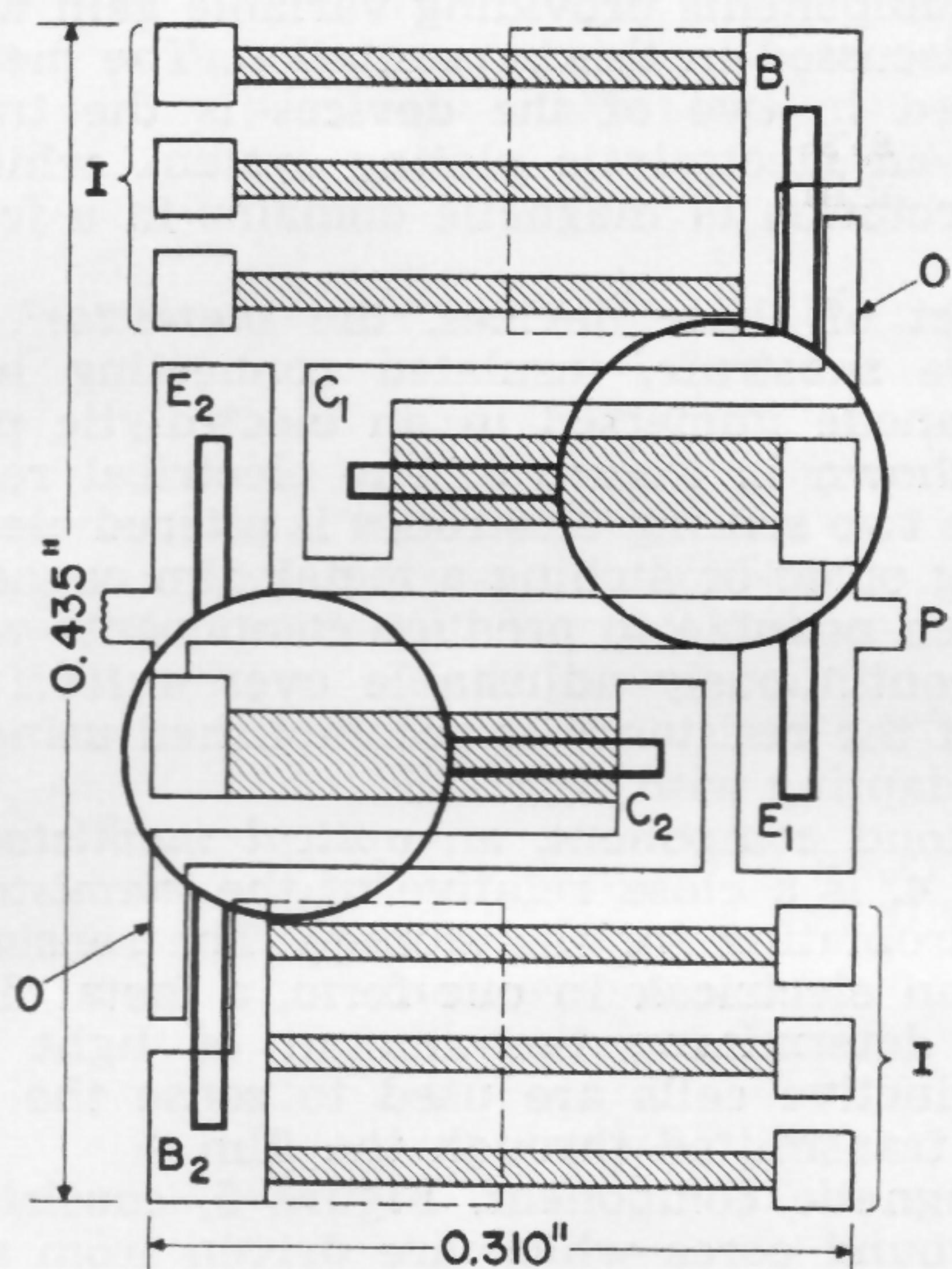


Figure 2—Topological layout of basic circuit. Two *trl-NOR* circuits are packaged within a .435" x .310" area. The resistor area is crosshatched, while the distributed overdrive capacitor area is dashed: *I* = inputs, *O* = outputs, and *P* = power and ground distribution.

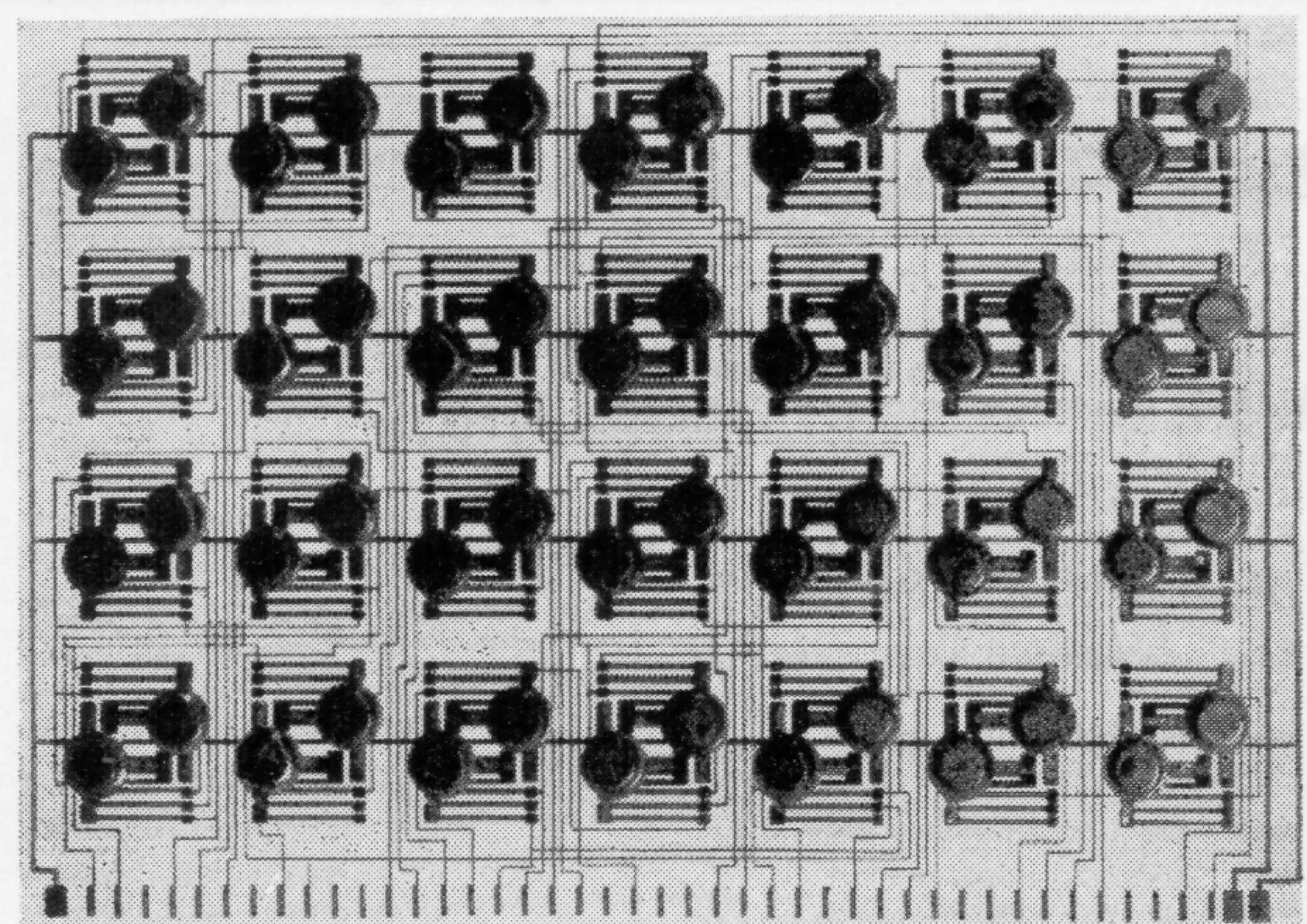
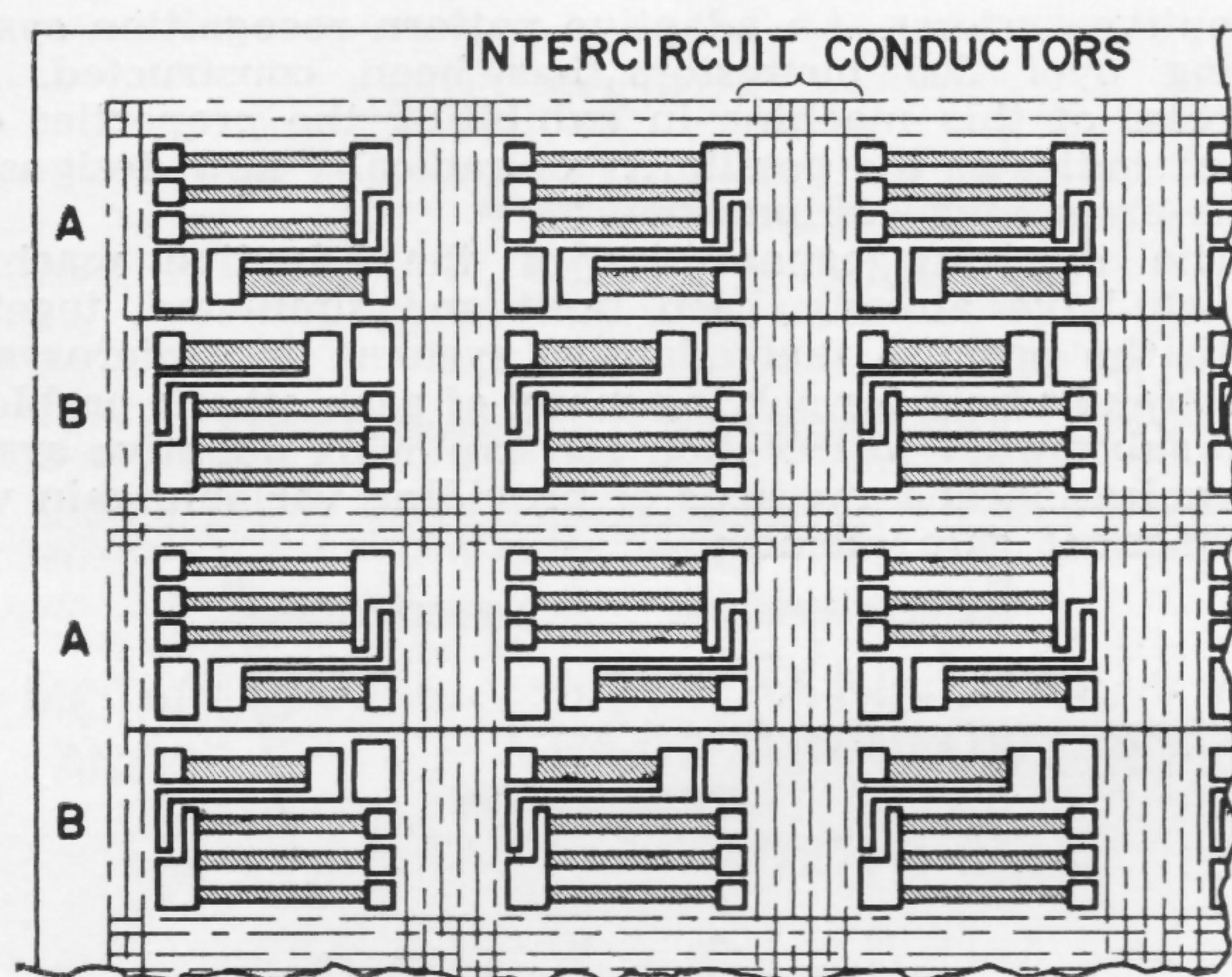


Figure 4—The integrated counter assembly, a 56-circuit panel, which contains a 4-stage binary counter, a master oscillator designed to run at either of two frequencies (1.25 and 2.5 Mc), and appropriate control features.

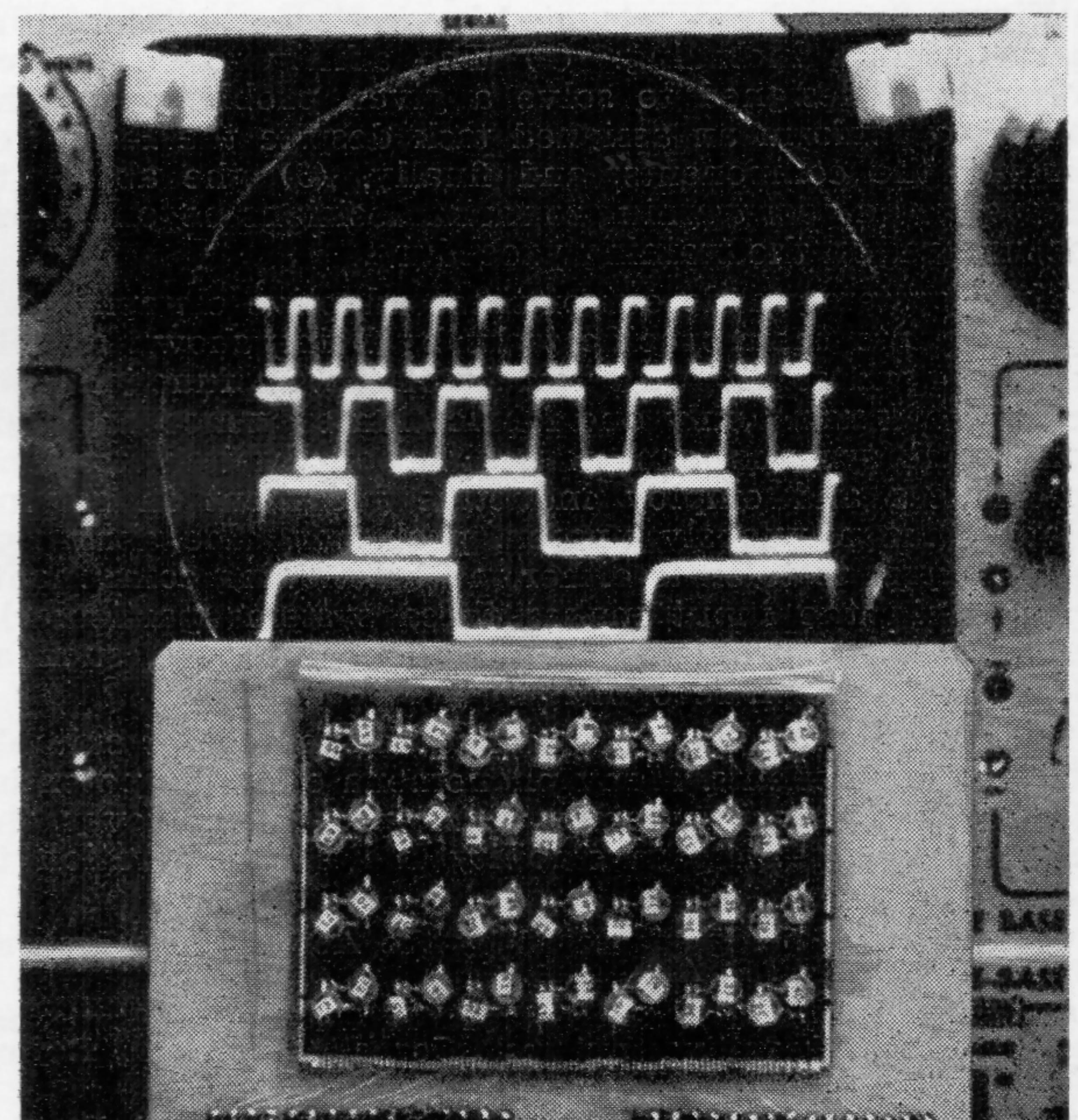


Figure 5—Thin-film assembly under test. The output waveforms of the 4-stage counter are displayed.

(Left)

Figure 3—Integrated thin-film panel with a partial view of a 2.5" x 3.5" x .040" substrate. Two of the four rows of circuit groups on the panel are shown. Each group consists of two thin-film circuits designated as *A* and *B*. Only one voltage supply (solid lines) was utilized to simplify the power distribution on the panel.

## SESSION IX: Functional Components

### FM 9.4: Components for Trainable Systems\*

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P. R. Low

IBM Corporation and Stanford University  
Stanford, Calif.

MANY INVESTIGATORS have examined the characteristics of networks of adaptive elements<sup>1,2,3</sup>. To realize these elements economically in large numbers, these studies have indicated the need for a new component. Such a component, Figure 1, can be described as having a variable gain with memory, in which the gain is constant in the absence of a control signal, but varies smoothly over a normalized range of  $\pm 1$  when a control signal is applied.

Given such components, an adaptive element<sup>4</sup>, as shown in Figure 2, can be constructed having several interesting characteristics, including: (1) The ability to be trained rather than designed to solve a given problem; (2) the ability to perform an assigned task despite the failure of some of the components; and finally, (3) the ability to generalize on past training to make decisions beyond those encountered in the training procedure.

Since systems made out of these adaptive elements can be trained to their specific tasks by being shown sample problems and solutions, a variety of system functions can be achieved using only one fabrication sequence. In addition, such systems can generalize on limited training experiences and employ inductive judgment in solving related, but previously unseen, problems. The ability of such systems to tolerate either malfunctioning components or noise in the input makes these systems particularly suited to solve problems of a statistical nature, such as speech and pattern recognition.

These properties have stimulated the search for suitable adaptive components. Many phenomena offer the potential of variable gain with memory<sup>5,6</sup>. At present, however, the required long-term gain stability limits consideration to

phenomena involving atomic translation or rotation. Purely electronic phenomena, with the possible exception of superconductivity, are thus excluded.

Three components providing variable gain with memory will be discussed in this presentation. The memory mechanism used in two of the devices is the translation of atoms in an electrolytic plating system, while the third uses the rotation of magnetic domains in a ferromagnetic material.

The first of these devices, the *memistor*<sup>7</sup>, consists of conductive substrate, insulated connecting leads, and a metallic anode immersed in an electrolytic plating solution, as shown in Figure 3. The electrical resistance between the two sensing electrodes is altered electrolytically by plating on to or etching a metal film connecting them. It has been possible to produce components whose resistance is continuously adjustable over a 100:1 range. The sensing of the resistance is accomplished using ac voltage and the adapting with dc.

The second component, an *optical memistor*, as shown in Figure 4, is a close relative of the *memistor* in that it uses electroplating for the storage. The sensing is optical rather than electrical. In one form, a metal film is measured by determining the amount of light transmitted. Photoconductive cells are used to sense the intensity of the light transmitted through the film.

The magnetic component, Figure 5, consists of a pair of tape-wound cores which are driven from an *rf* power source. The output winding is arranged so that the fundamental component of the *rf* voltage in it cancels out, leaving a second harmonic distortion voltage proportional to the remanent flux in the cores (in the directions shown). The remanent flux level can be altered by passing a direct current through the output winding. Due to an interaction between the dc adaptation current and the *rf* drive current, the rate of change of the remanent flux, with respect to the adaptation current, is quite constant and reversible, thus providing a smoothly variable gain with permanent memory.

The research program at Stanford University has been concerned with the development of useful and practical adaptive systems. An adaptive pattern recognition system using over 300 memistors has been constructed. The success of this machine in exhibiting the properties outlined indicates the possibility of radically new designs for data-processing equipment.

The inspiring capabilities of the adaptive machines which have already been built and simulated, together with the promise that adaptive systems and microsystem electronics hold for solving many of each other's problems, are substantial justification for exploring adaptive system organization and methods of providing variable gain with permanent gain memory.

\* This work is being sponsored by the Aeronautical Systems Division, ARDC, U. S. Air Force.

<sup>1</sup> Rosenblatt, F., "The Perceptron: A Theory of Statistical Separability in Cognitive Systems", Cornell Aero. Lab., Report VG-119-G-1, Buffalo; January, 1958.

<sup>2</sup> Mattson, R. L., "A Self-Organizing Logical System", Eastern Joint Computer Conference Convention Record; 1959.

<sup>3</sup> Widrow, B., Pierce, W. H., Angell, J. B., "Birth, Life, and Death in Microelectronic Systems", Stanford University Technical Report No. 1552-2/1851-1; May 30, 1961.

<sup>4</sup> Widrow, B., and Hoff, M. E., "Adaptive Switching Circuits", Stanford University Technical Report No. 1553-1; June 30, 1960.

<sup>5</sup> Brain, A. E., "The Simulation of Neural Elements by Electronic Networks Based on Multiaperture Magnetic Cores", Proc. IRE, p. 49-52; January, 1961.

<sup>6</sup> Hurd, R. M., and Lane, R. N., "Solion—Principles of Electrochemistry and Low-Power Electrochemical Devices", Technical Report, U. S. Naval Ordnance Laboratory, White Oak, Silver Spring, Md.

<sup>7</sup> Widrow, B., "An Adaptive 'Adaline' Neuron Using Chemical 'Memistors'", Stanford University Technical Report No. 1553-2; October 17, 1960.

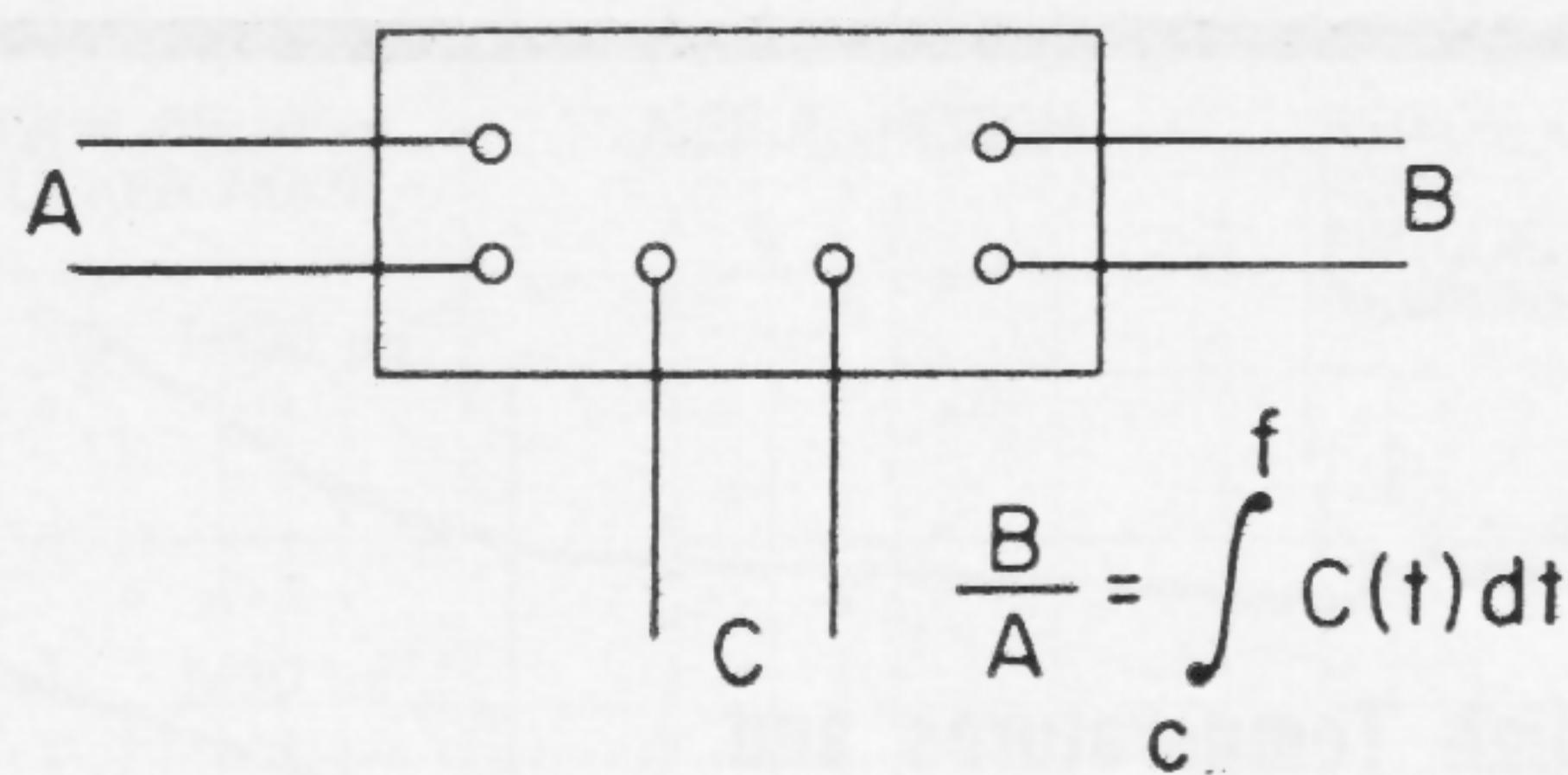


Figure 1—Ideal three-port representation of a variable gain device.

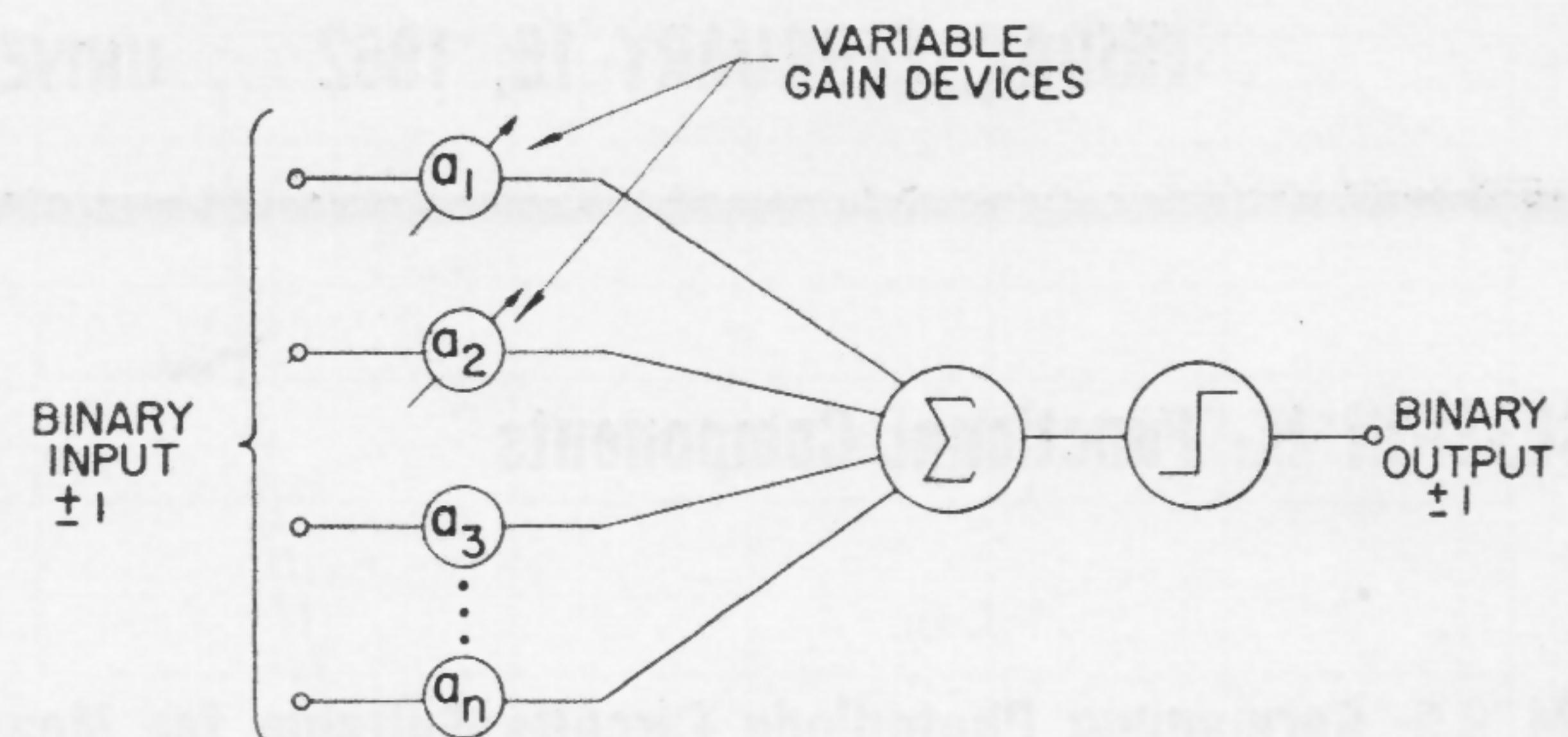


Figure 2—Single adaline adaptive element.

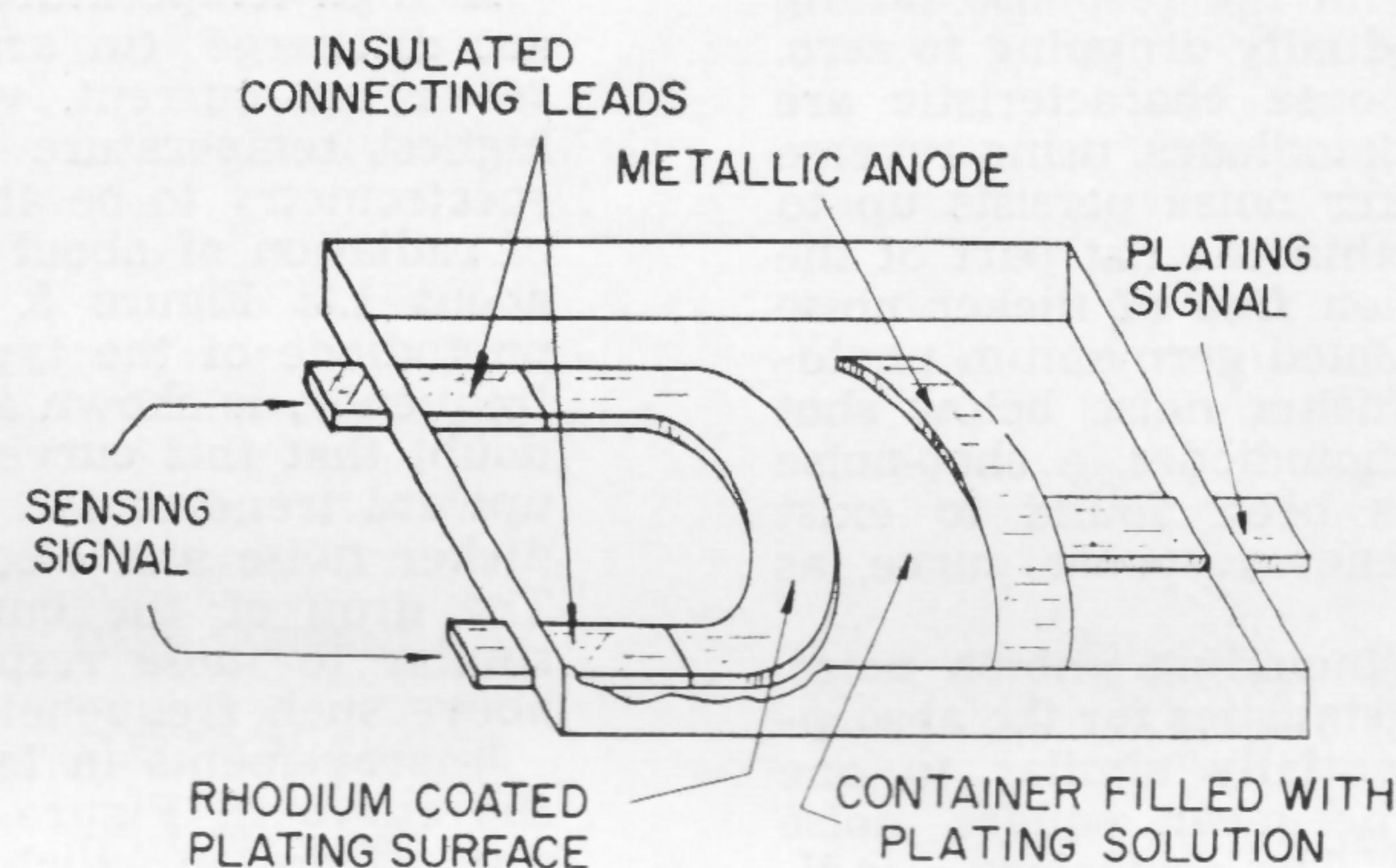


Figure 3—The memistor.

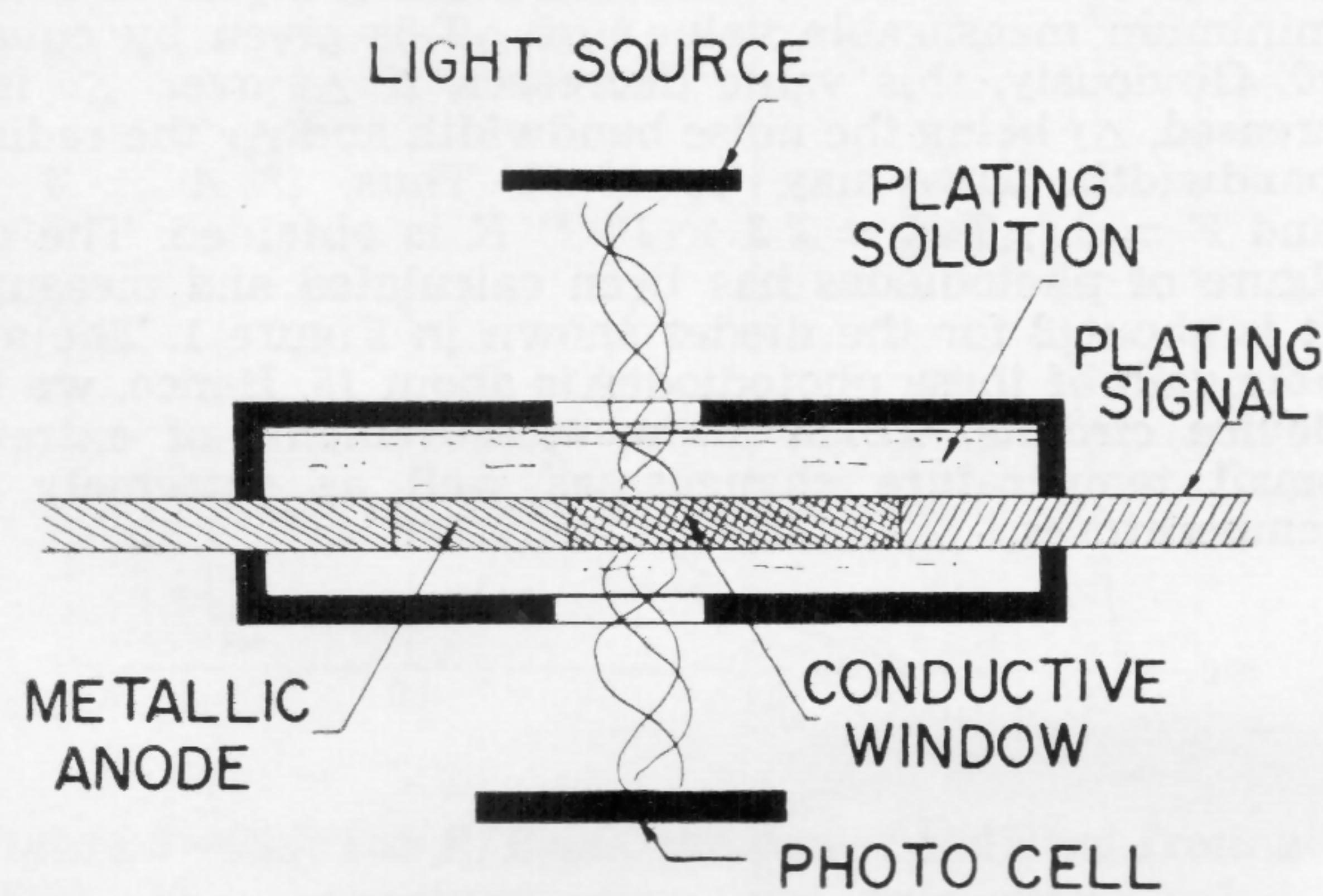


Figure 4—Optical memistor.

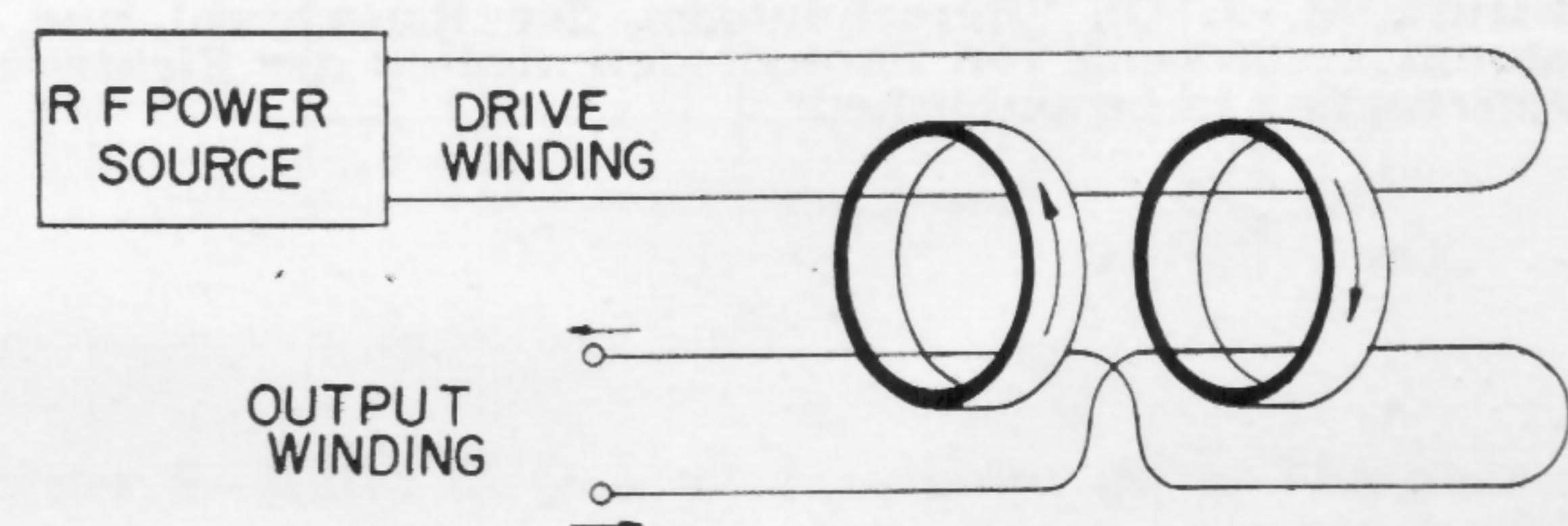


Figure 5—A magnetic adaptive component.

## SESSION IX: Functional Components

## FM 9.5: Germanium Photodiode Circuits Suitable for Measuring Extremely High Temperatures and Extremely Small Temperature Changes

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Swiss Federal Institute of Technology  
Zurich, Switzerland

THE FREQUENCY RESPONSE of germanium and silicon types of *pn* photodiodes, when measured by modulated radiation, has been found to be identical, with the response falling off between 10 and 20 kc, and gradually dropping to zero. The physical causes of this response characteristic are only partly understood. In most photodiodes, using reverse bias, at currents of 20-60  $\mu$ a, flicker noise persists up to frequencies above 10 kc. Thus, within the flat part of the frequency response curve, no region free of flicker noise may be found. However, some selected germanium photodiode types disclosed a drop in flicker noise below shot noise at about 1-2 kc. In these photodiodes, a shot-noise region, showing white noise, has been found to exist within the flat part of the frequency response curve, as shown in Figure 1.

A noise theory of photodiodes, including photon noise, has been evolved using Boltzmann statistics for the absorption process. This theory is essentially similar to one offered by A. van der Ziel<sup>5</sup>. The mean square noise current is presented in equation 1. The coefficient  $a$  indicates the mean number of electrons per photon impinging on the photodiode. The quantities  $x$  and  $\mu$  are related to the radiation source, supposedly a black body. Equation 1 has been well confirmed experimentally<sup>1,3</sup> within the shot-noise region of the photodiodes.

At values of  $x$ , which are small with respect to unity, the quantity  $\mu$  is approximately equal to  $kT/h\nu$ . Hence, in this case, the quantity  $\gamma$  according to equation 2 becomes approximately equal to  $a kT/h\nu$ . Thus, the photodiode noise according to equation 1 becomes approximately proportional to the radiation temperature  $T$ . The region,

where this approximation<sup>1,2,4</sup> holds good, may be seen from Figure 3.

A high-temperature radiation source, consisting of an arc discharge (in argon) at an atmospheric pressure at 200  $a$  arc current, was developed for our studies. The highest temperature in the discharge was estimated by spectrometry to be about 20,000° K. At a mean frequency of radiation of about  $2 \times 10^{14}$  cps it was found that  $\gamma$  is about 1.3; Figure 3. A measured curve<sup>†</sup> of  $\gamma$  with a photodiode of the type shown in Figure 1, dependent on frequency, is shown in Figure 4. There seems to be little doubt that this curve confirms the foregoing theory. The upward trend of the curve below 8 kc is due, in part, to flicker noise and also to noise caused by arc instability. The drop of the curve above 20 kc is due to reasons similar to those responsible for the drop of the curves above such frequencies shown in Figure 1.

Improvements in techniques might decrease the rise of the curve in Figure 4 below 8 kc. By the use of two photodiodes on which the radiation from the arc impinges, the noise caused by its instability, being coherent, may be blotted out. This result was obtained in preliminary measurements<sup>††</sup>. Hotter arcs now being prepared will lead to higher values of  $\mu$  and  $\gamma$ . The theory resulting in equation 1 is based on the statistics of Boltzmann. If the statistics of S. N. Bose are applied, the factor  $\gamma$  in equation 1 must be replaced by  $\mu$ . Information in Figure 4 serves as experimental evidence that the former statistics are valid.

The mean power at a mean frequency  $\nu$ , emitted by an aperture of relatively small area  $A$  in the enclosure of a black-body radiation space of temperature  $T$  appears in equation 5. Here  $\Delta\nu$  is the bandwidth at a mean frequency  $\nu$ . Computing equations 6 and 7 and solving for  $\Delta T$  equation 8 is obtained. The universal function  $Q$  of  $\nu$  and  $T$  is shown in Figure 6. Its minimum value  $Q_{min}$  occurs at  $x = 3.83$  and is equal to  $3.66 \times 10^{-3}$  K-meter. The formula for  $Q$  is in equation 9. The noise-figure  $F$  of the photodiode can be defined as the ratio of available noise power to available signal power at the output, divided by the equivalent ratio at the input. Using a photodiode, the minimum measurable value<sup>4</sup> of  $\Delta T$  is given by equation 10. Obviously, this value decreases, if  $\Delta f$  over  $\Delta\nu$  is decreased,  $\Delta f$  being the noise bandwidth and  $\Delta\nu$  the radiation bandwidth. This may be  $10^{-13}$ . Thus, if  $A = 1 \text{ mm}^2$  and  $F = 2$ ,  $\Delta T_{min} = 2.3 \times 10^{-6}$  K is obtained. The noise figure of photodiodes has been calculated and measured<sup>6</sup>. It is about 2 for the diodes shown in Figure 1. The available gain of these photodiodes is about 15. Hence, we have device circuits, which allow measurements of extremely small temperature changes, as well as extremely high temperatures.

<sup>†</sup> Curve prepared by Werner Gubler.<sup>††</sup> Measurements made by Werner Gubler.<sup>1</sup> Spescha, G., "Experimentelle Untersuchungen ber über spontane Photonenschwankungen," Thesis, Swiss Federal Institute of Technology; 1959.<sup>2</sup> Spescha, G., and Strutt, M. J. O., "Theoretische Ueberlegungen zur Experimentellen Bestimmung der Spontanen Photonenschwankungen," *Helvetica Physica Acta*, vol. 133, p. 53-68; 1960.<sup>3</sup> Spescha, G., and Strutt, M. J. O., "Experimentelle Bestimmung der Spontanen Photonenschwankungen," *Helvetica Physica Acta*, vol. 133, p. 69-88; 1960.<sup>4</sup> Strutt, M. J. O., "Ueber die kleinste messbare Temperaturänderung," *Archiv der Elektrischen Uebertragung*, vol. 15, p. 355-358; 1961.<sup>5</sup> van der Ziel, A., "Noise," Prentice-Hall, p. 112; 1954.<sup>6</sup> Strutt, M. J. O., "Berechnungen der Rauschzahl und der Leistungsverstärkung von Photodioden," *Archiv der Elektrischen Uebertragung*; to be published.

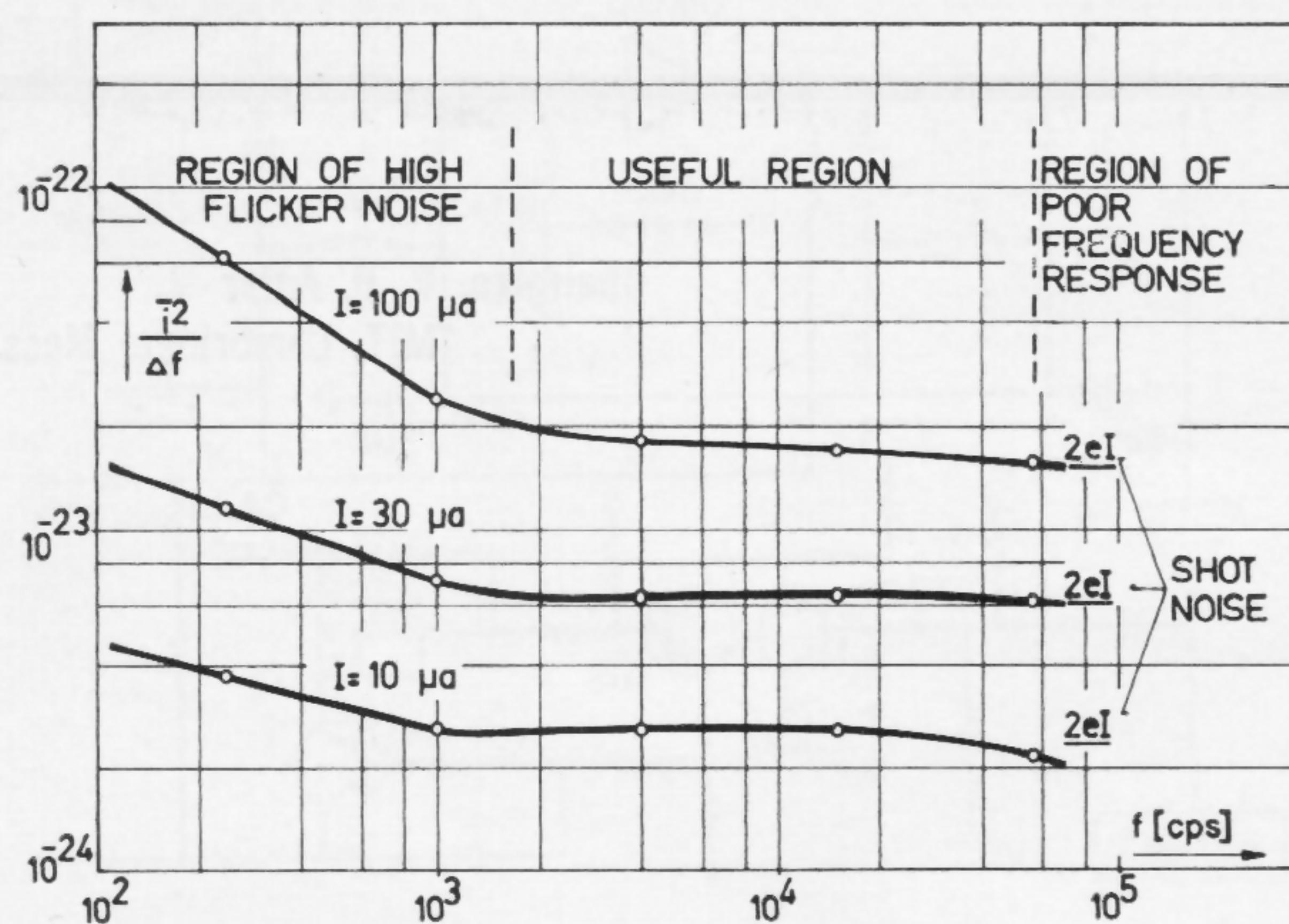


Figure 1—Mean square noise current for a selected germanium photodiode. The useful region is bounded by flicker noise and falling frequency response.

$$(1) \quad \bar{I}^2 = 2e(I - I_0)\gamma\Delta f + 2eI_0\Delta f$$

$$(2) \quad \gamma = 1 + \alpha(\mu - 1)$$

$$(3) \quad \mu = \frac{\exp(x)}{\exp(x) - 1}$$

$$(4) \quad x = \frac{h\nu}{kT}$$

I = MEAN DC CURRENT

$I_0$  = DARK CURRENT

$\Delta f$  = NOISE BAND WIDTH

e = ELECTRON CHARGE

h = PLANCK'S CONSTANT

T = TEMPERATURE

k = BOLTZMANN'S CONSTANT

$\alpha$  = QUANTUM EFF.

$\nu$  = RADIATION FREQUENCY

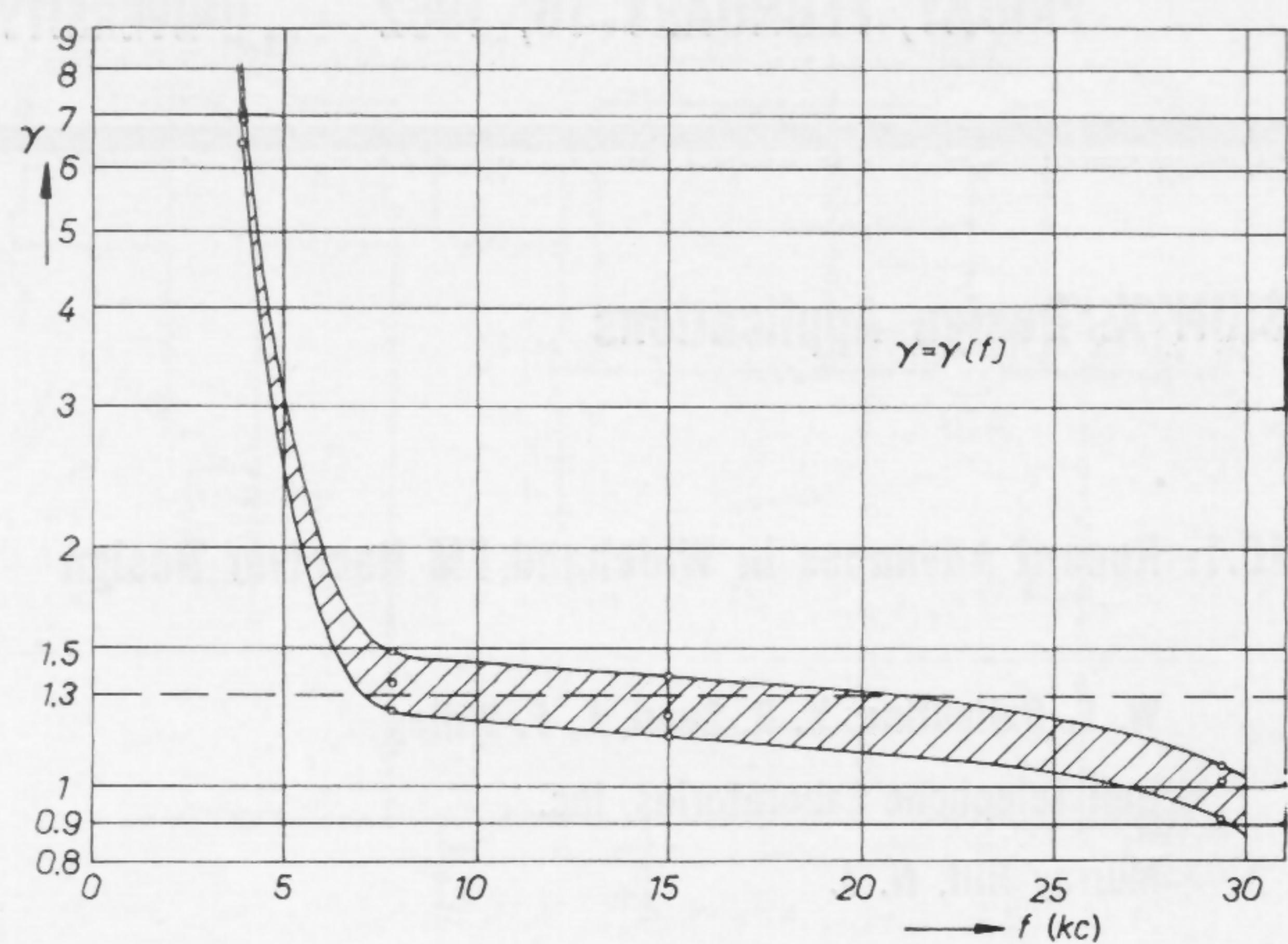


Figure 4—Experimental curve of  $\nu$  (vertical), dependent on frequency at a radiation temperature of about  $20,000^\circ K$ .

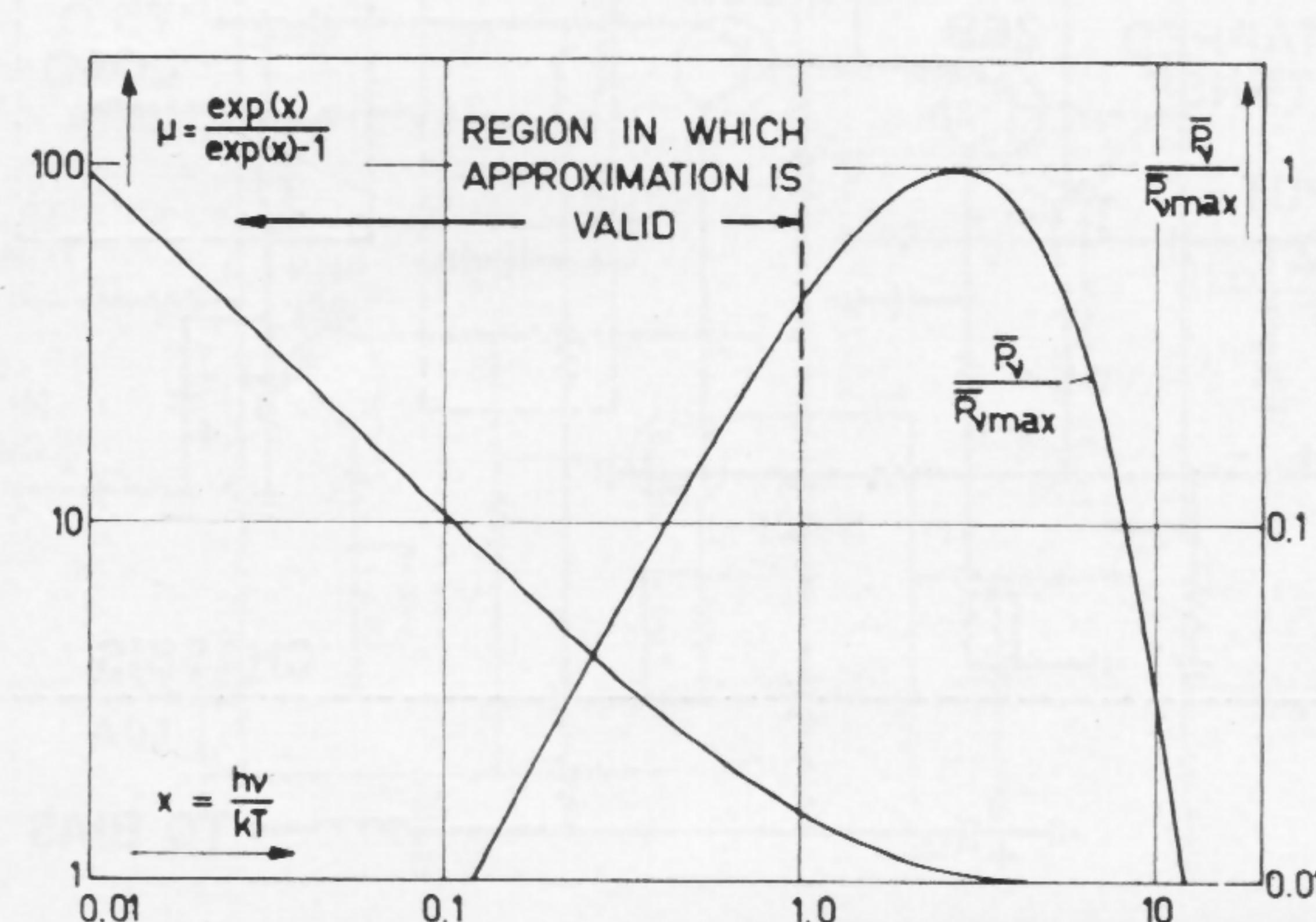


Figure 3—Plot for  $P/P_{\nu_{max}}$ , the power radiated from a black body aperture over its maximum value, dependent on  $x = h\nu/kT$ , where  $\mu$  is dependent upon  $x$ .

$$(5) \quad \bar{P}_Y = \frac{2A\pi h\nu^3\Delta\nu}{c^2(\exp x - 1)}$$

$$(6) \quad \frac{\Delta\bar{P}_Y}{\Delta T} \approx \frac{d\bar{P}_Y}{dT} = \bar{P}_Y \mu \frac{x}{T}$$

$$(7) \quad \Delta\bar{P}_Y = \sqrt{(\Delta\bar{P}_Y)^2}$$

$$(8) \quad \Delta T = Q(\nu, T) \sqrt{\frac{\Delta f}{A\Delta\nu}}$$

$$(9) \quad Q = \frac{2hc}{k\sqrt{\pi}} \frac{\sinh(\frac{x}{2})}{x^2}$$

$$(10) \quad \Delta T_{\min} = Q_{\min} F \sqrt{\frac{\Delta f}{A\Delta\nu}}$$

c = VELOCITY OF LIGHT A = AREA

F = NOISE FIGURE

Figure 5—Equations that lead to the minimum observable value of temperature change.

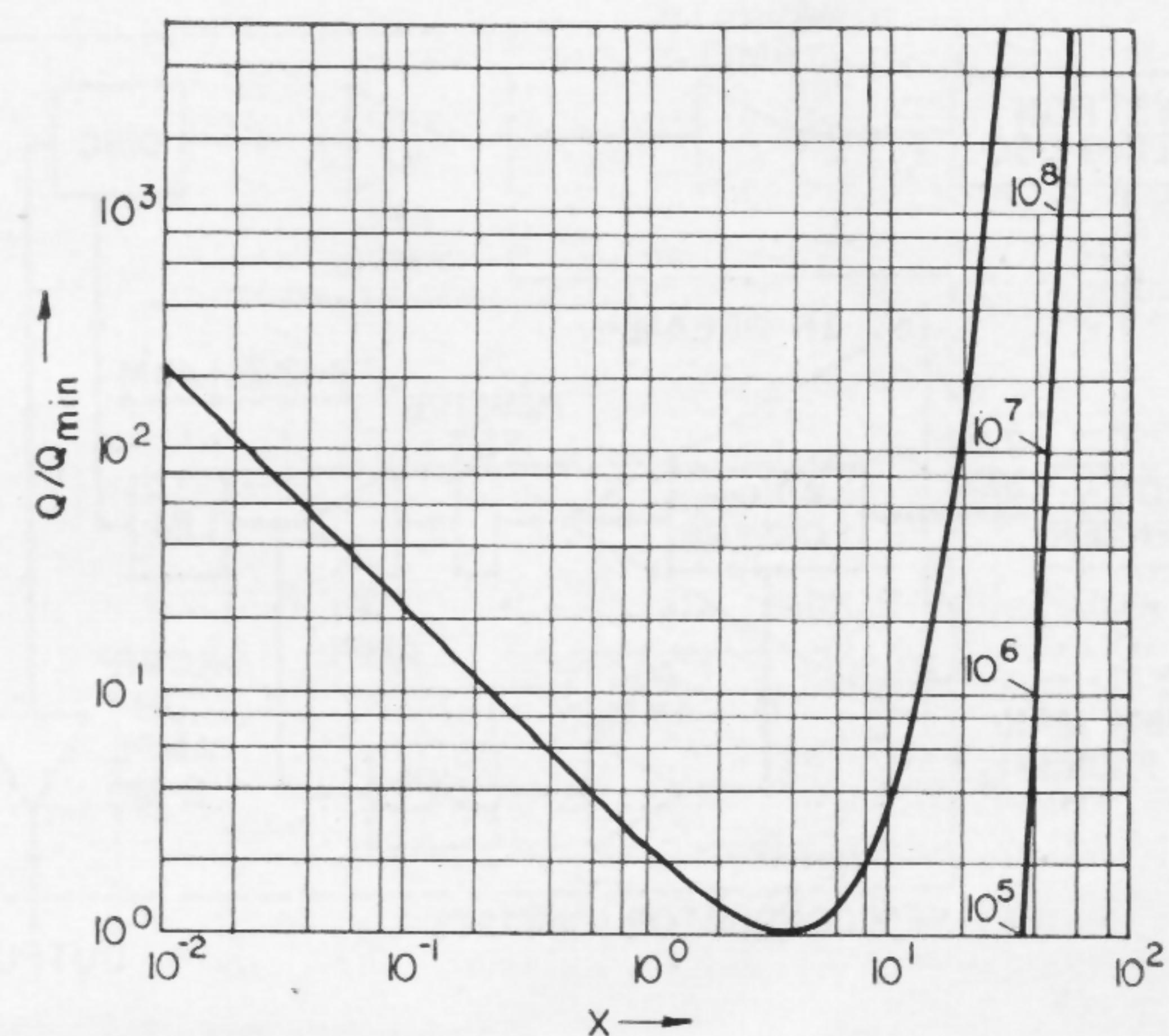


Figure 6—Ratio  $Q/Q_{\min}$  as dependent on  $x$ . The value  $Q_{\min}$  occurs at  $x = 3.83$  and is equal to  $3.66 \times 10^3$  K-meter.

## SESSION X: Design Applications

Chairman: R. B. Adler

MIT, Cambridge, Mass.

### FM 10.1: Recent Advances in Wideband FM Receiver Design

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Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

NEW CIRCUIT IDEAS have made possible the development of a solid-state FM receiver for a microwave radio system\*. The receiver (Figure 1) consists of a 70-Mc if amplifier with a 20-Mc bandwidth, 105-db gain, and 60-db of agc. It also contains a limiter, discriminator, and a baseband amplifier. The operating temperature range is  $-20^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$ .

The transistor if amplifier stages have been designed for bandwidth considerably wider than the required 20 Mc centered at 70 Mc. (Most of these are common-base stages with ferrite-core transformer interstages.) The overall if characteristic is fixed by a single, centrally-located passive bandpass filter. As a result, delay distortion has been minimized and the 105-db gain amplifier can be readily aligned flat to within  $\pm 1$  db over the if band.

A circuit known as a doublet (Figure 2) is used as the low-noise input if stage. It consists of two untuned common-emitter stages followed by a constant-resistance high-pass filter. The if band lies just below the filter cutoff.

By means of electronically-controlled if attenuators (Figure 3) 60-db of agc have been achieved. The control loop includes an if detector, a low-drift dc amplifier, and a novel biasing system for the attenuator diodes. When

\* Used in a short-wave microwave system, this receiver will be described in greater detail in a forthcoming *BSTJ* article; about May, 1962.

<sup>1</sup> Ruthroff, C. L., "Amplitude Modulation Suppression in FM Systems", *BSTJ*; July, 1958.

<sup>2</sup> *BSTJ*, p. 1604; November, 1961.

the current in lead K is zero, corresponding to a medium-loss condition, a  $-1.8\text{-v}$  dc bias is evenly distributed across six diodes. In this condition, the diode dynamic impedances are about 140 ohms, resulting in network impedance levels of about 75 ohms. These levels remain roughly the same over the full loss range.

The if output stage (Figure 4) consists of two transistors connected in parallel. The normal output set level is  $+15$  dbm into 100 ohms (or  $+12$  dbm into the limiter, which has a 200-ohm input impedance).

Requiring only two point-contact silicon diodes and a few linear passive components, the remodulation-type limiter (Figure 5) is, nevertheless, as effective as two or three conventional series or shunt limiters connected in tandem.

The output of the balanced discriminator (Figure 6) occupies the frequency region from 200 cps to 6 Mc and is applied to a low-distortion feedback amplifier, the receiver baseband amplifier; Figure 7.

The transmitter baseband amplifier (Figure 8) drives the transmitting klystrons in the radio system, amplifying the applied voltage by a factor of about 30. It uses an unusual arrangement of transistors and has even broader bandwidth and lower distortion at full output than the receiver baseband amplifier.

The overall receiver amplitude linearity is 2% at  $25^{\circ}\text{C}$ . The intermodulation distortion is 15 db less than in a comparable vacuum-tube receiver.

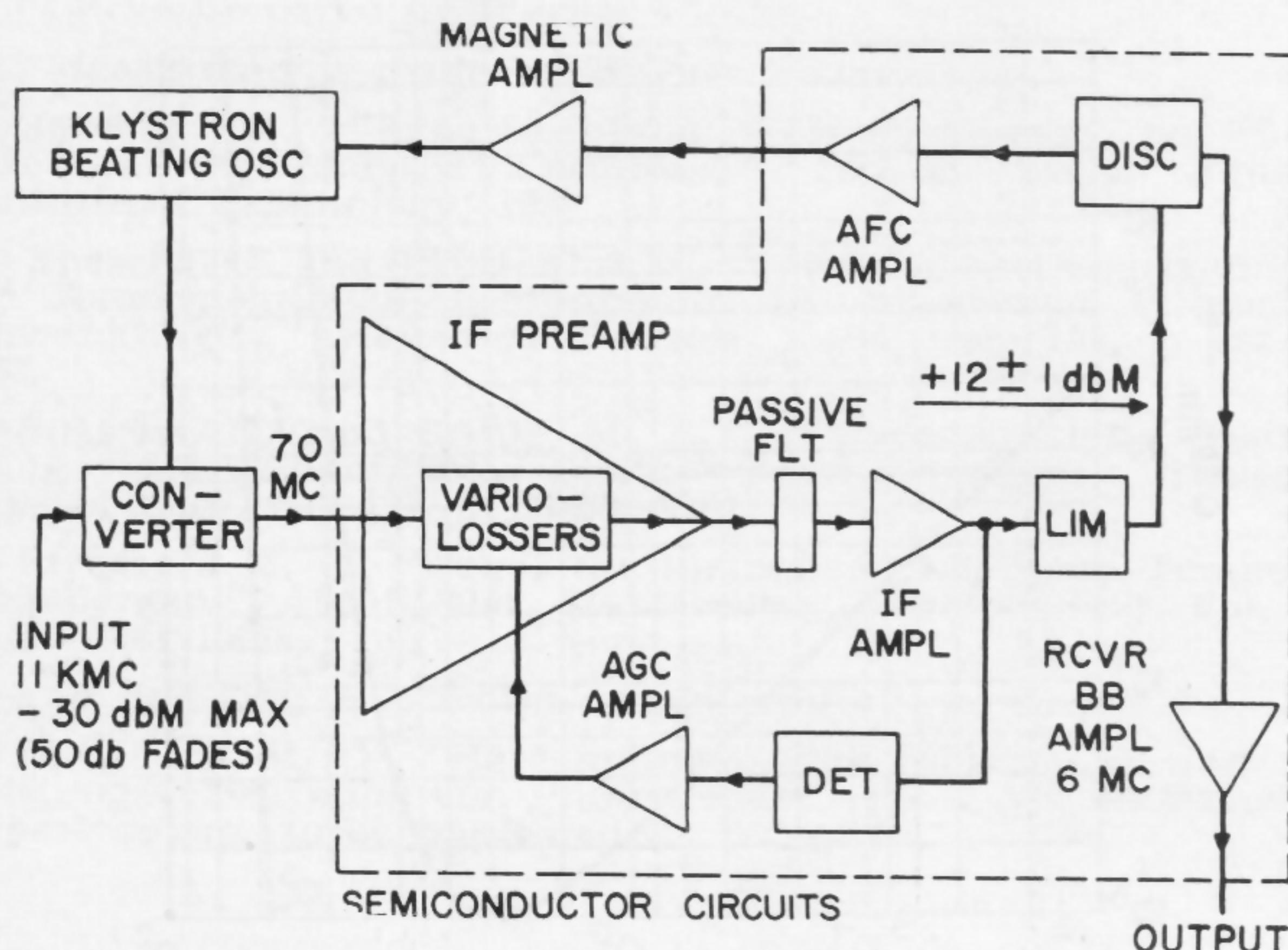


Figure 1—Block diagram of FM receiver for a microwave radio system. The only vacuum tubes in this system are the transmitting and local-oscillator klystrons.

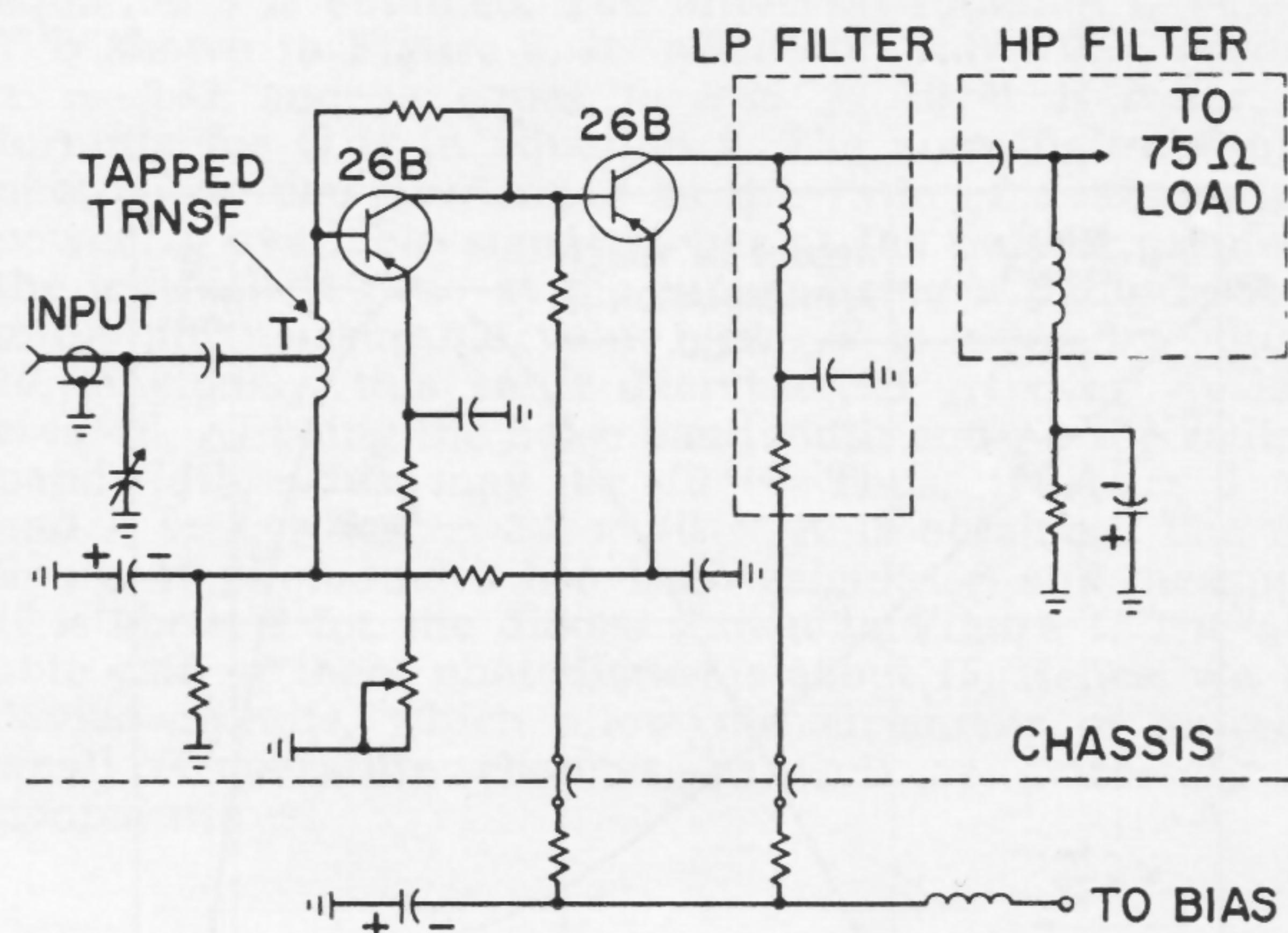


Figure 2—Low-noise input circuit (*doublet*) which has a noise figure of 6 db and provides an input return loss greater than 20 db over the if band.

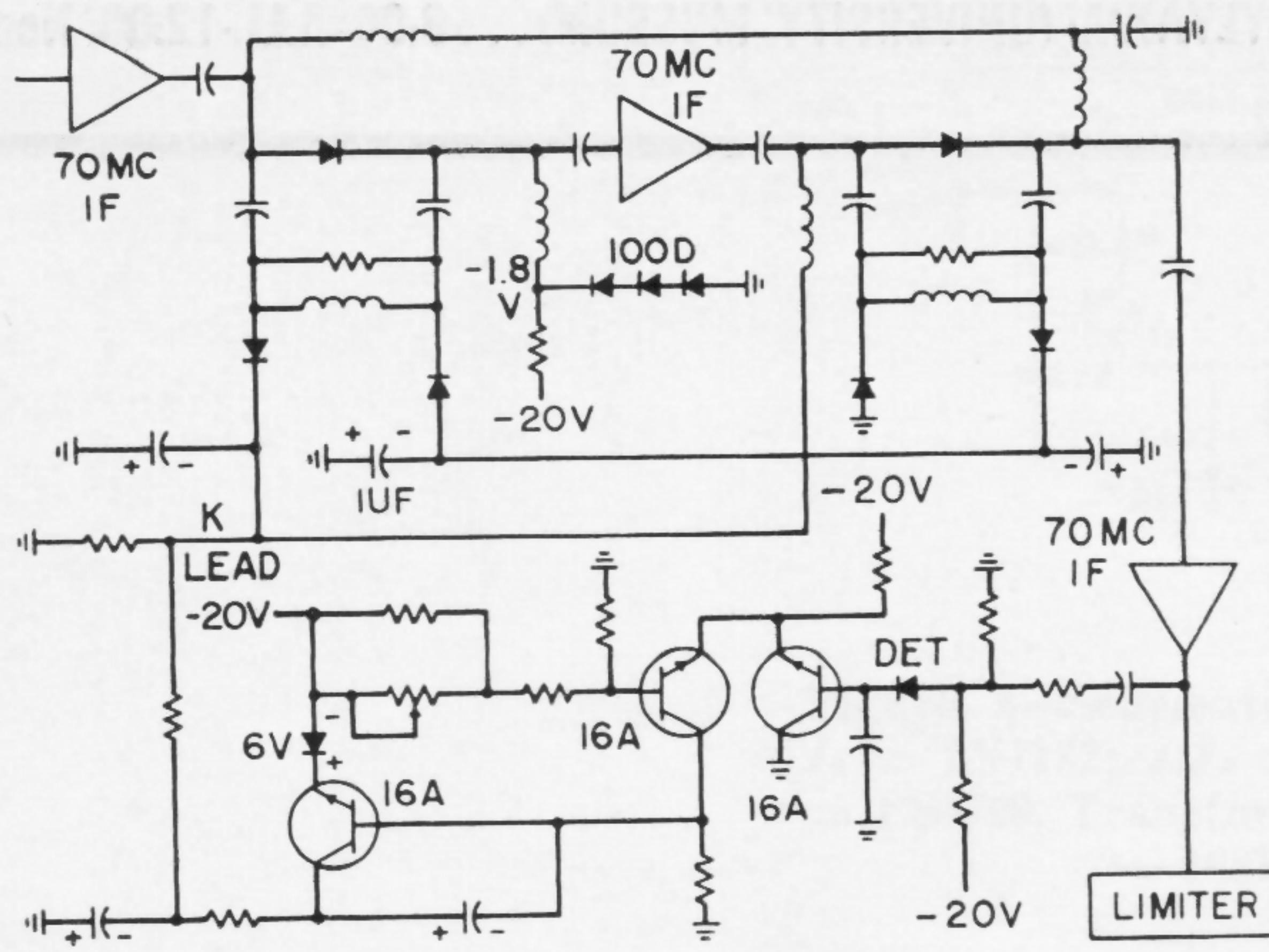


Figure 3—The *agc* circuitry. The *variolossers*, using *pi* networks of germanium point-contact diodes, maintain low-impedance levels over a loss range of 30-db per section.

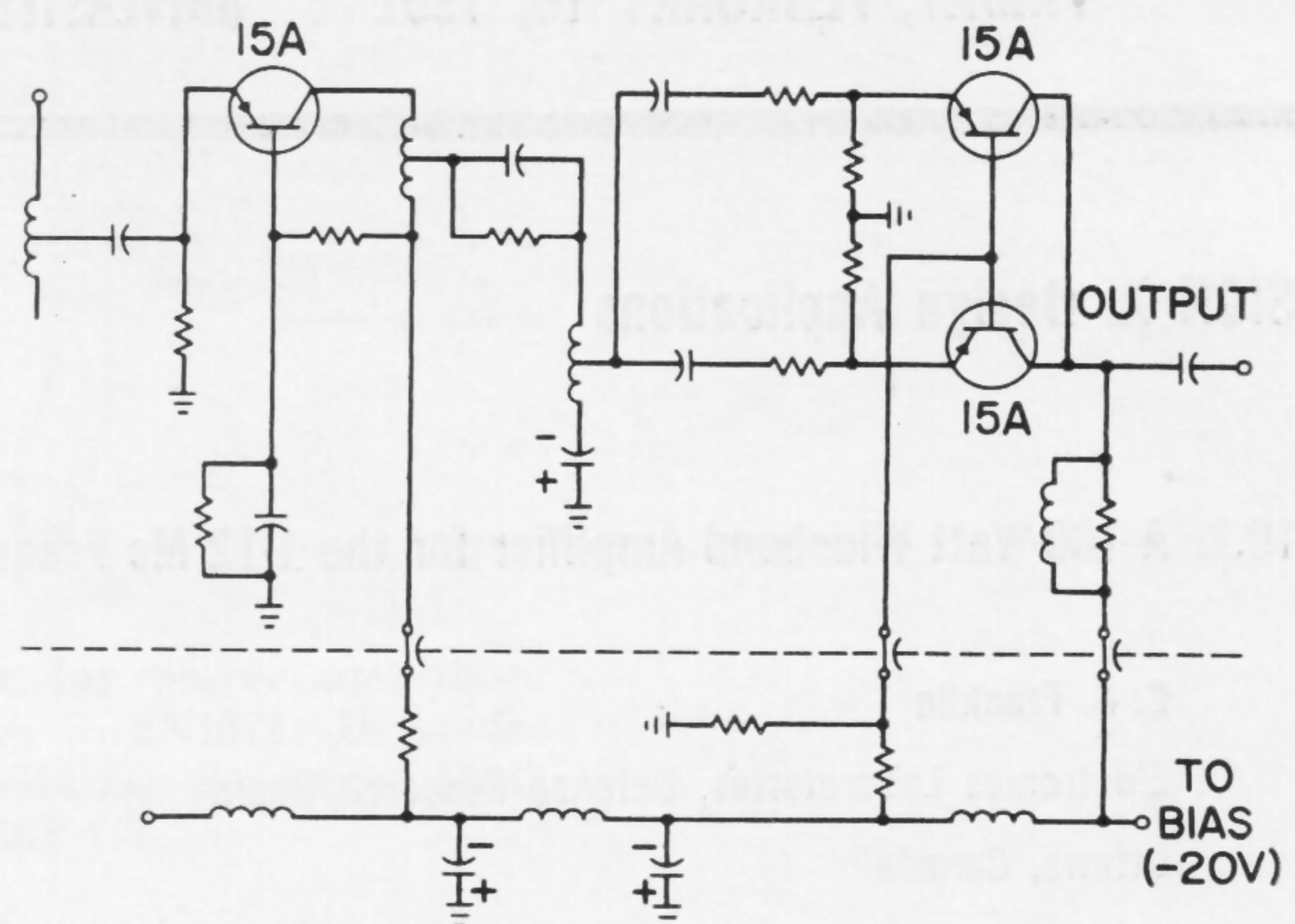


Figure 4—Output stages of *if* amplifier. The last interstage, designed to minimize AM to PM conversion, yields a 4:1 current stepup, compared to 2:1 at the other interstages.

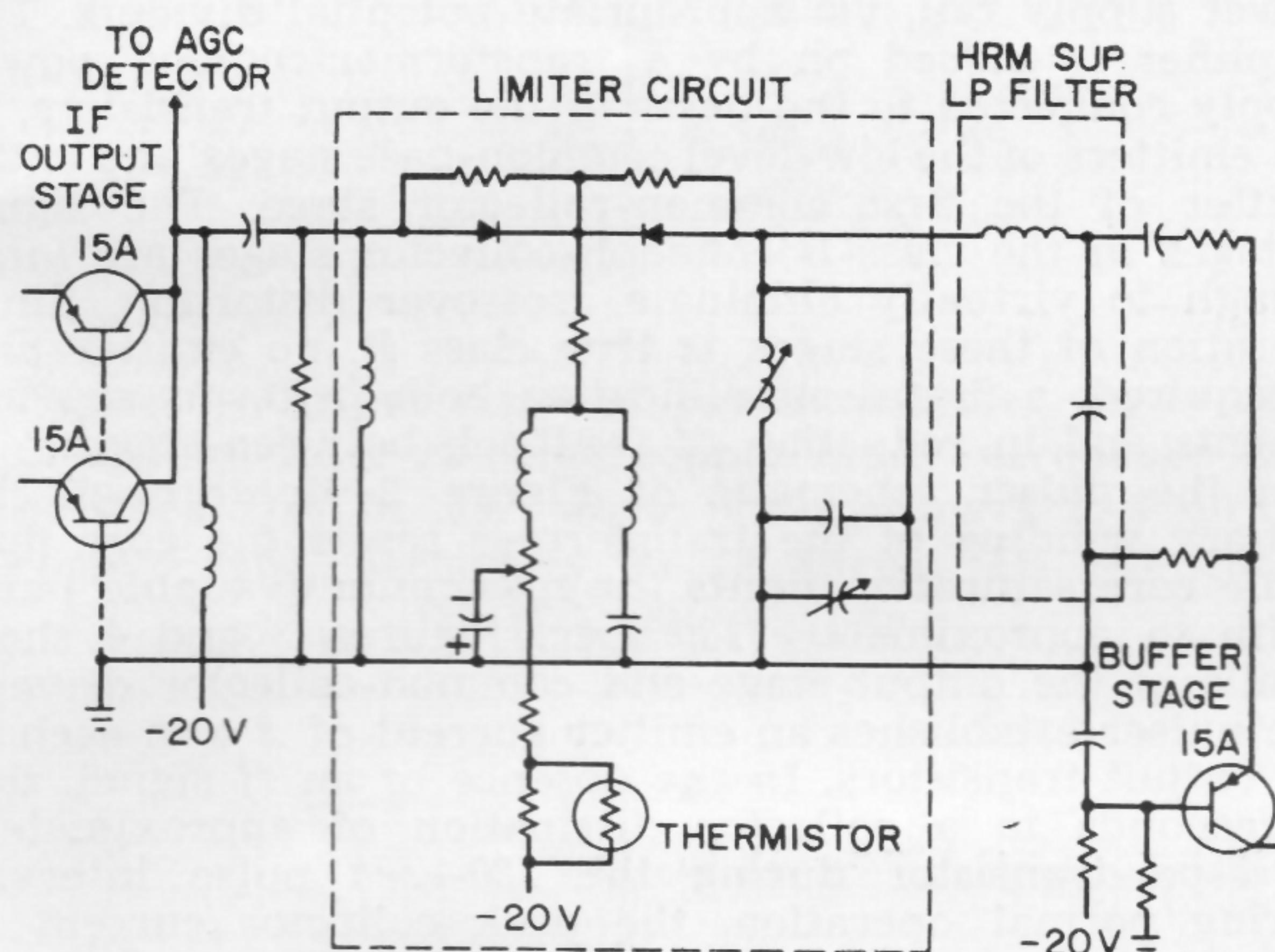


Figure 5—Remodulation-type limiter<sup>1</sup>.

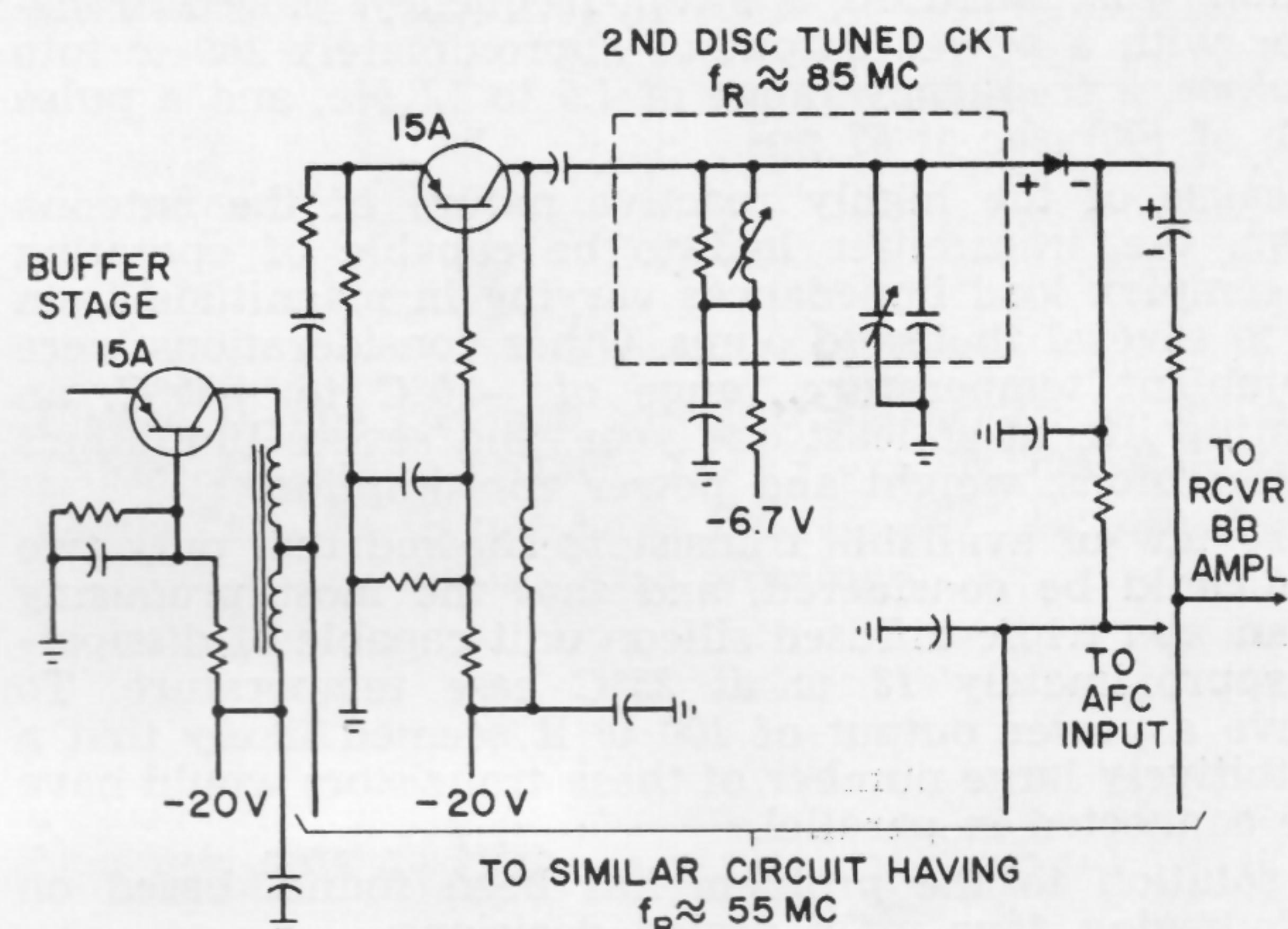


Figure 6—Triple-tuned balanced discriminator<sup>2</sup>. Slope at center of *S* curve supplies 25  $\mu$ a/Mc to *RCVR BB AMPL*. The first tuned circuit is shown in Figure 5.

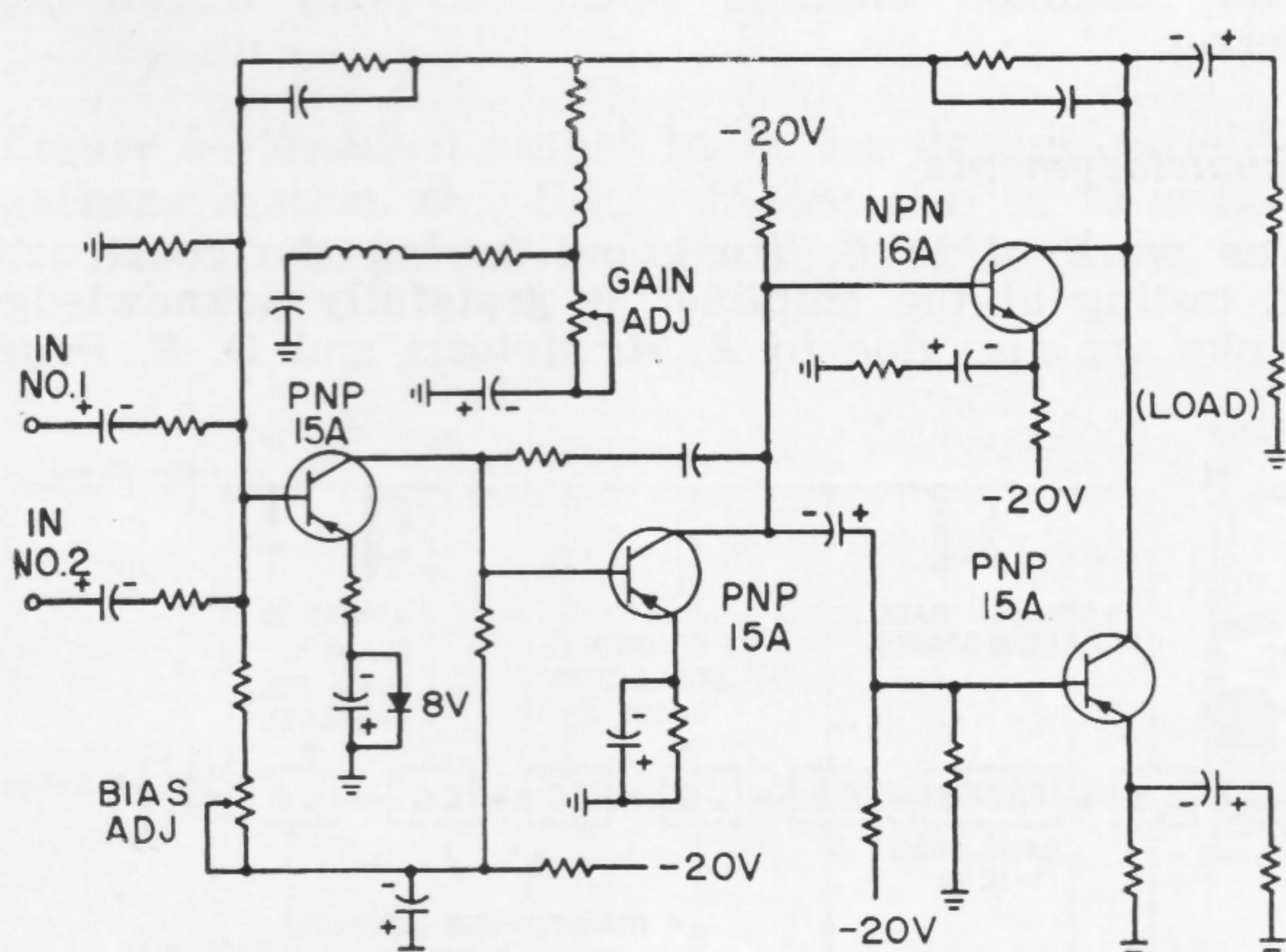


Figure 7—Receiver baseband amplifier. Gain flat to  $\pm .15$  db from 200 cps to 6 Mc and adjustable over a 6-db range. Distortion products  $\leq -40$  dbf at +10-db output level into load.

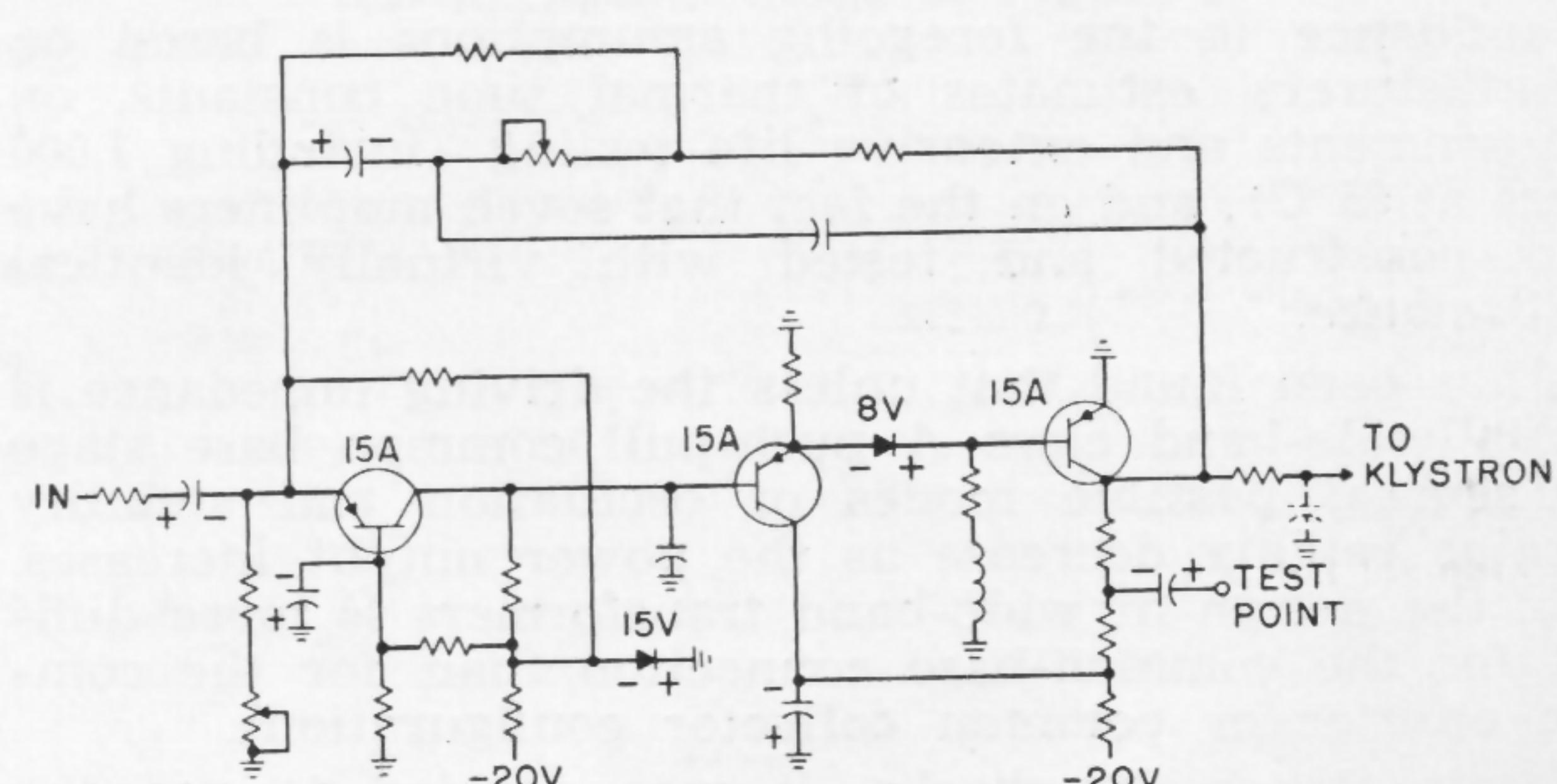


Figure 8—Transmitter baseband amplifier. Gain is flat to  $\pm .1$  db from 200 cps to 6 Mc and adjustable over an 8-db range. Distortion products  $\leq -46$  dbf at  $\pm 4$ -v peak output.

## SESSION X: Design Applications

## FM 10.2: A 100-Watt Wideband Amplifier for the 1-12 Mc Frequency Range

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THE GENERATION of pulses of rf, at power levels considerably greater than the steady-state ratings of available transistors, has become an important design objective in space electronics.

In developing an ionospheric earth satellite a design solution was found in a swept-frequency pulsed transmitter with a power output of approximately 100 w into 400 ohms, a frequency range of 1.5 to 12 Mc, and a pulse width of 100  $\mu$ sec at 67 pps.

Because of the highly reactive nature of the antenna system, the transmitter had to be capable of operating into complex load impedances varying in magnitude from zero to several thousand ohms. Other considerations were an ambient temperature range of  $-10^{\circ}\text{C}$  to  $+65^{\circ}\text{C}$ , an operating life of at least one year, and severe limitations on dimensions, weight and power consumption.

A review of available transistors showed that only two types could be considered, and that the most promising was an *n*p*n* triple-diffused silicon unit capable of dissipating approximately 12 w at  $25^{\circ}\text{C}$  case temperature. To achieve a power output of 100 w it seemed likely that a prohibitively large number of these transistors would have to be connected in parallel.

A solution to the problem has been found, based on the following four main design decisions:

(1)—A collector thermal time-constant of the 12-w silicon power transistor  $\approx 600 \mu$ sec or greater.

(2)—For the common base connection, it should be possible to operate the transistor safely using a collector supply voltage equal to half the manufacturer's peak  $V_{cbo}$  rating. This is because collector current  $I_c$  is a slowly varying function of collector voltage  $V_c$  and is based on measurements on over 100 power transistors.

(3)—The high-frequency parameters of the power transistor should not be seriously degraded when the peak collector dissipation is 4 to 5 times the maximum allowable steady-state figure.

(4)—The use of tape windings in ferrite pot cores, permitting a solution of the difficult wideband transformer problems encountered in high level stages.

Confidence in the foregoing assumptions is based on manufacturers' estimates of thermal time constants, on measurements and extensive life testing (including 1,000 hours at  $85^{\circ}\text{C}$ ), and on the fact that seven amplifiers have been constructed and tested with virtually identical performance.

It has been found that unless the driving impedance is low, a wide-band class A push-pull common base stage has several possible modes of oscillation and stability margins rapidly decrease as the power output increases. Also, the design of wide-band transformers is more difficult for the common-base connection than for the common emitter or common collector configurations.

Despite these drawbacks, it was decided to use the common base connection in the output stage since—

(1)—The maximum allowable collector voltage, for class-A operation, is higher than for the common emitter or common collector connections, (2)—the output capacitance is lower than for the common emitter connection, and (3)—there is no serious transistor protection problem

when the load impedance falls to zero. A common collector stage is particularly poor in this respect.

The stability requirements were satisfied by using a low-impedance drive obtained from a cascade of class-B common-collector stages. The design of this driver chain proved more difficult than expected and called for considerable care in choice of transistor types, transformer turns ratios, and transformer winding configurations.

Figure 1 shows the block schematic for the power amplifier. All collector voltages are derived from a single power supply rail, via appropriate potential dividers. The amplifier is pulsed on by a transformer-coupled power supply connected to the bases of the output transistors, to the emitters of the low-level common-base stages, and to the emitter of the first common-collector stage. The signal voltages in the class-B common-collector stages are large enough to virtually eliminate crossover distortion. Since operation of these stages is true class B, no emitter bias is required; a useful simplification both in terms of components and in reduction of feedback between stages.

In the pulser schematic of Figure 2, dc through the tertiary winding of the transformer resets the core flux, while core saturation limits the maximum available pulse width to approximately 180  $\mu$ sec. Figures 3 and 4 show details of the output stage and common-collector drivers. The pulser establishes an emitter current of .8 a in each of the output transistors. In the absence of an rf signal, this corresponds to a collector dissipation of approximately 30 w-per-transistor during the 120- $\mu$ sec pulse interval. During normal operation, the peak collector current in each of the output transistors is  $\approx 1.6$  a. Figure 5 shows the additional circuitry needed for reliable operation into a highly reactive antenna system. The zener diode *DA*1 limits the maximum voltage at the collectors of *J*<sub>15</sub> to *J*<sub>22</sub>, while diodes *D*<sub>15</sub> and *D*<sub>16</sub>, serve as peak rectifiers to prevent capacitance across the zener from shunting the output load.

When the amplifier is gated off, thermal noise which is approximately 14 db above *KTB*, appears at the output terminals. This noise is attenuated by diodes *D*<sub>17</sub> to *D*<sub>20</sub> to permit common antenna operation with a low noise receiver.

## Acknowledgments

The work of *P. E. Townsend* during the construction and testing of the amplifier is gratefully acknowledged. Thanks are also due to *A. R. Molozzi* and *D. F. Page*.

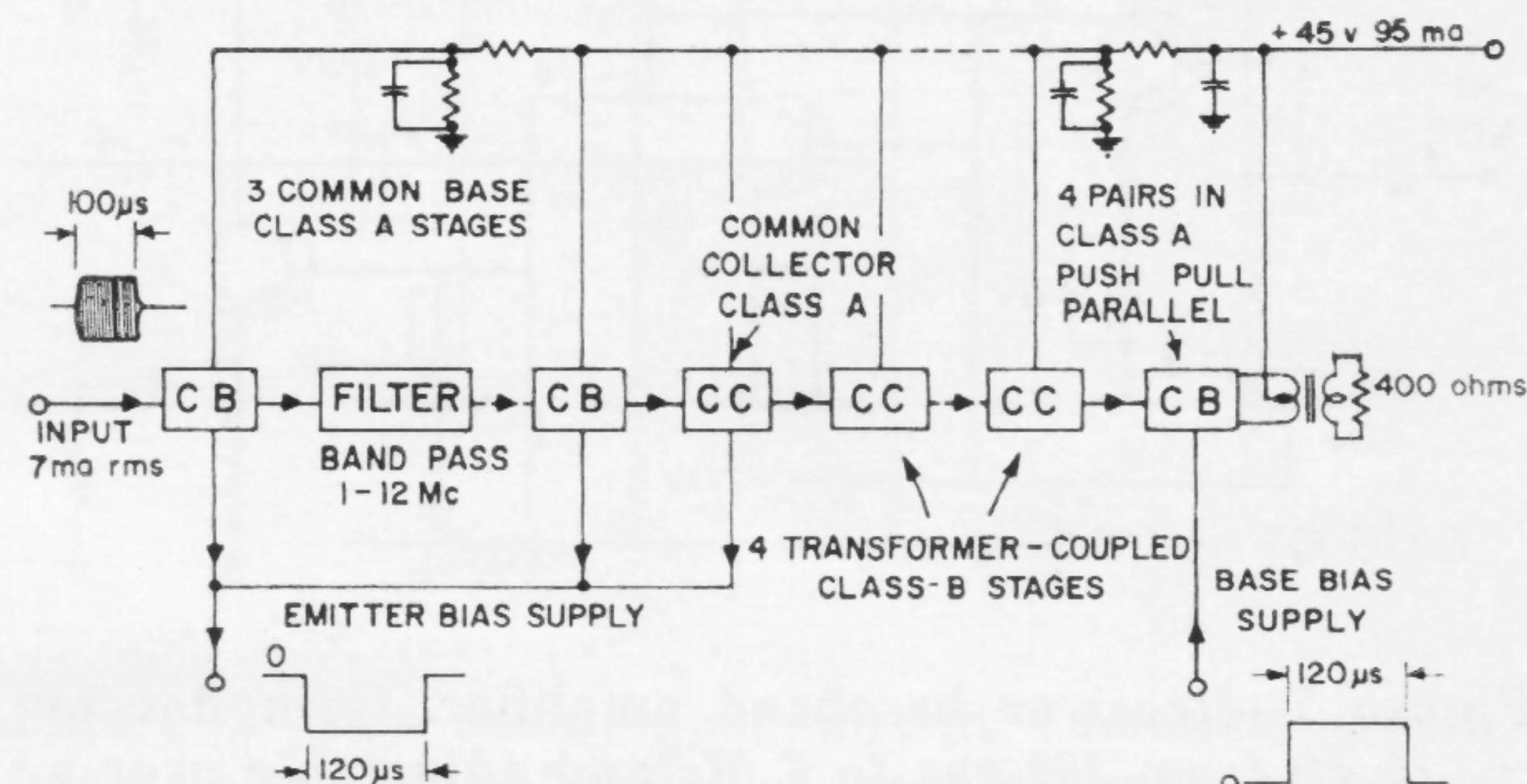


Figure 1—Block schematic of 100-w power amplifier.

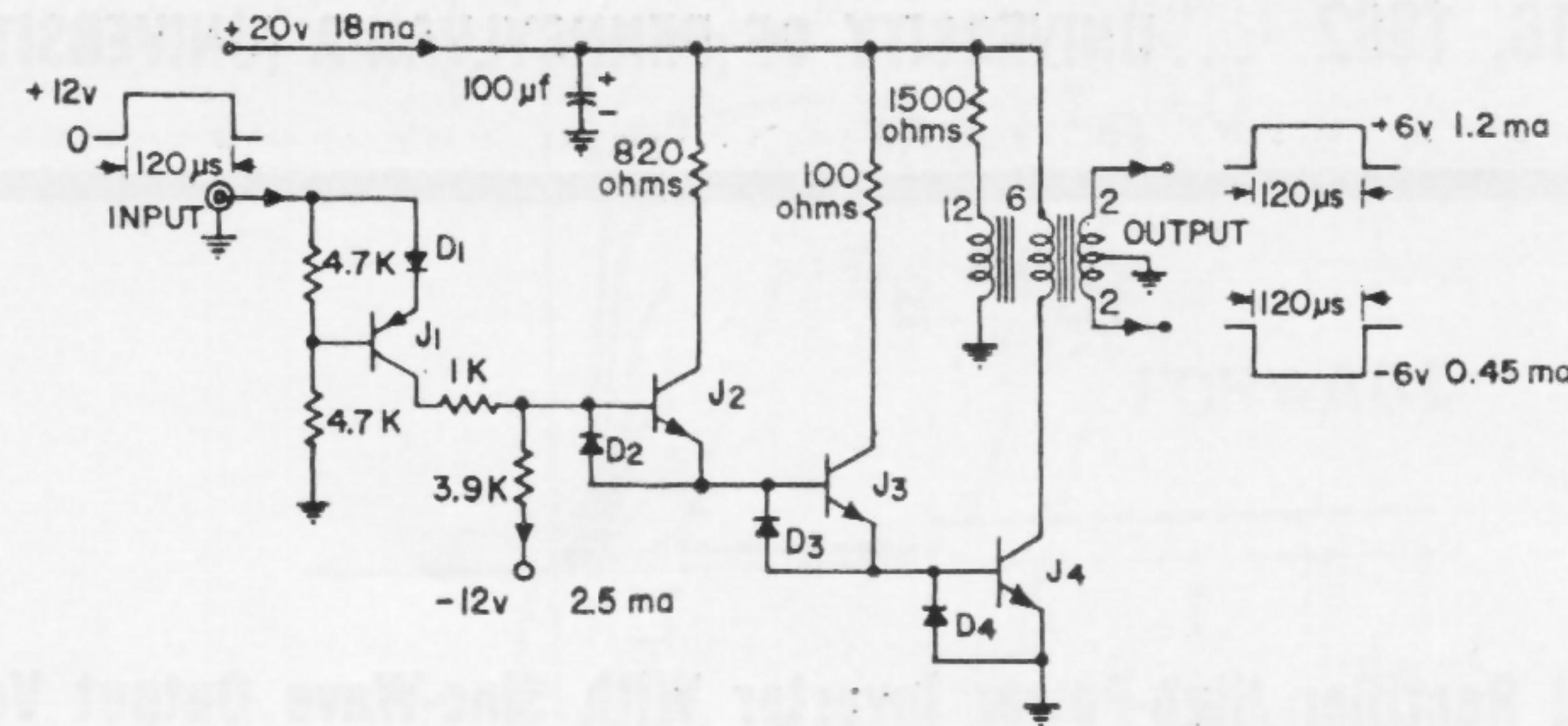


Figure 2—Schematic of pulser for power amplifier.  $J_1 = 2N1132$ ;  $J_2, J_3 = 2N1613$ ;  $J_4 = 2N1072$ ;  $D_1 - D_4 = PS4720$ . Transformer is a Deltamax core type 5651, 168T, 84T and 56T CT.

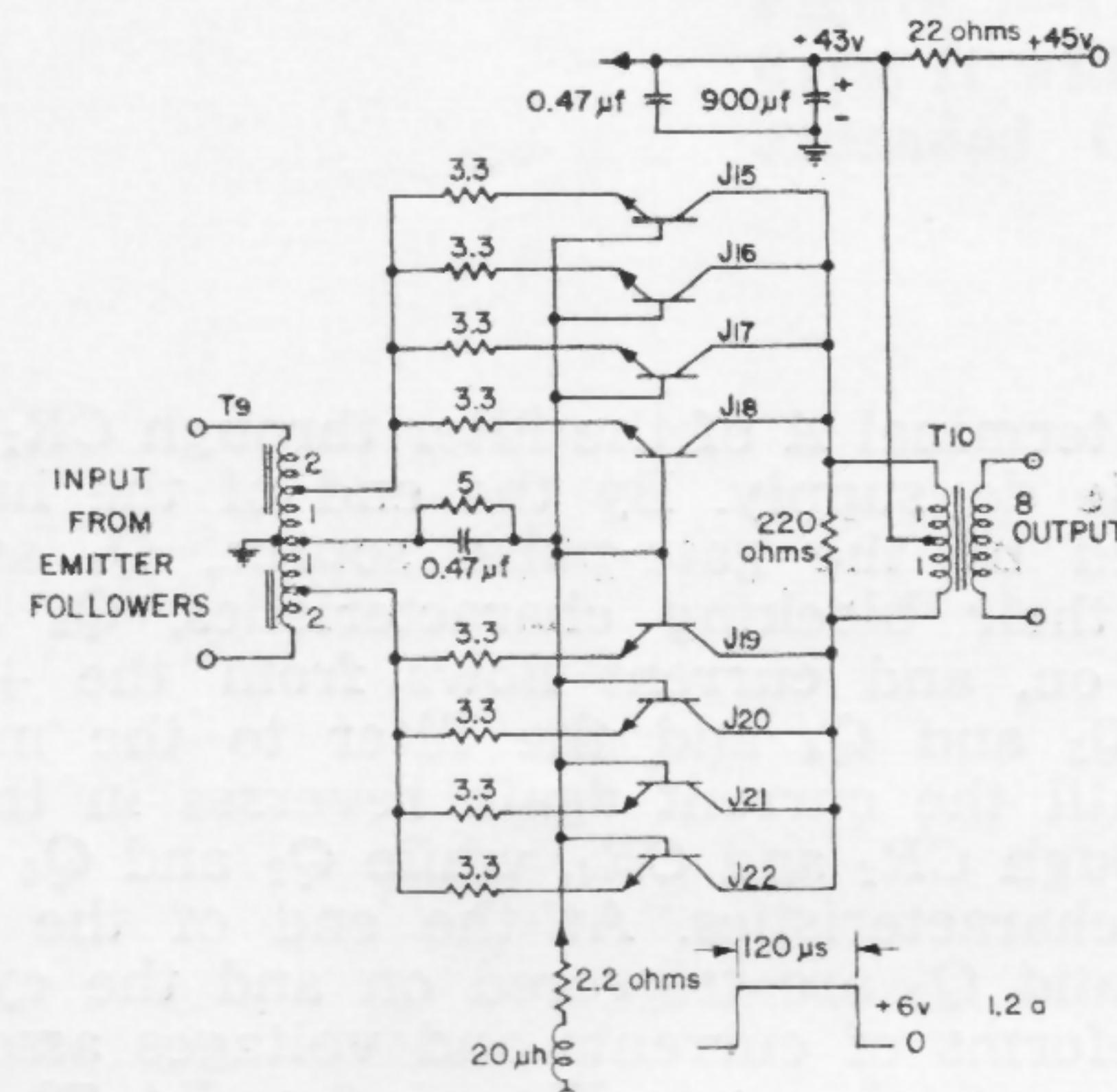


Figure 3—Output stage of power amplifier.  $J_{15} - J_{22} = 2N1709$ .  $T_9 = 18$  turns copper tape. Ferroxcube 4B pot core, D25/16, .007" air gap.  $T_{10}$  primary = 6 turns copper tape, secondary = 24 turns; 4B pot core D25/17.5, .001" air gap.

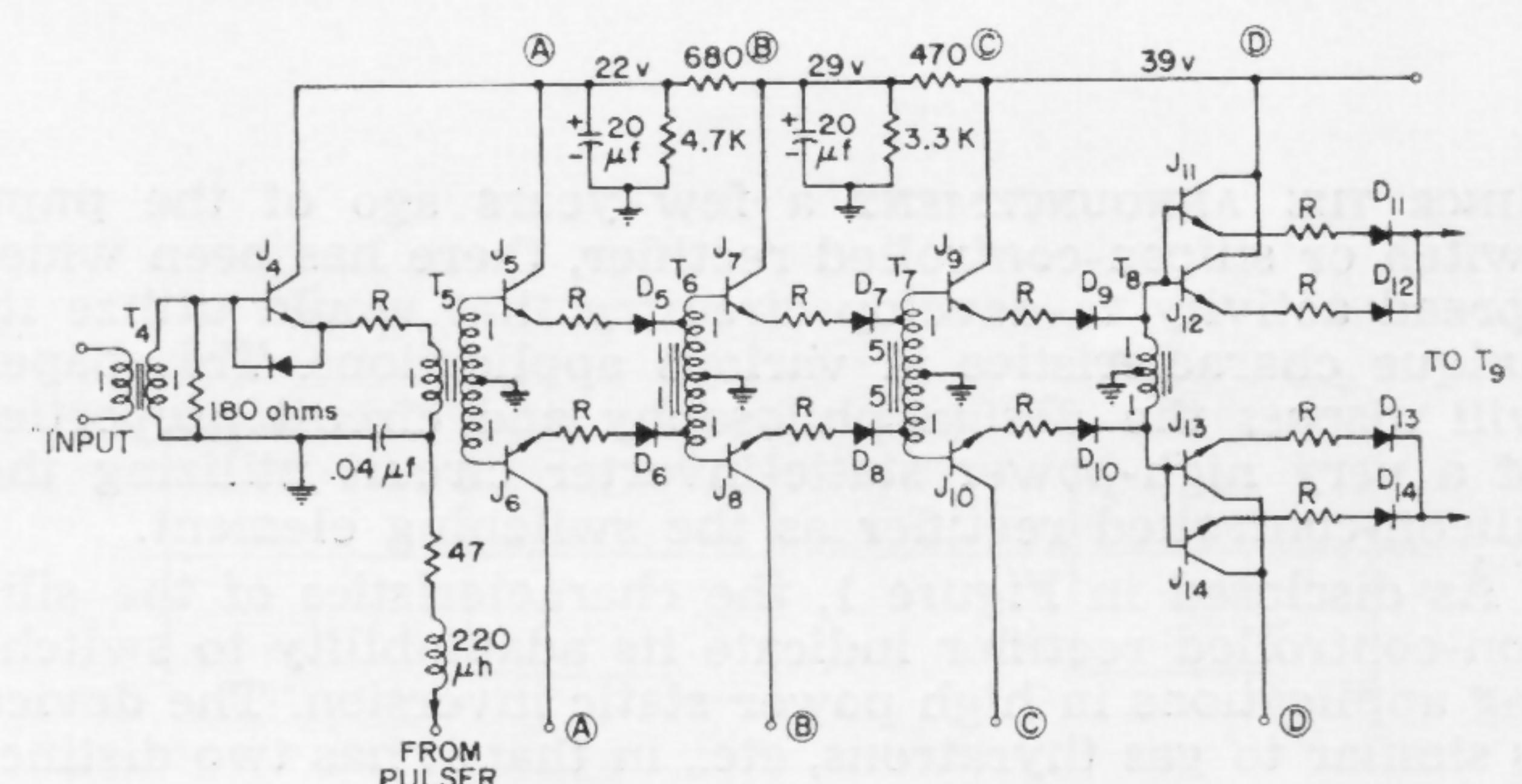


Figure 4—The common collector driver.  $D_5 - D_{14} = 1N928$ ;  $J_4 - J_8 = 2N1506$ ;  $J_9 - J_{14} = 2N1709$ .  $R = 3.3$  ohms.  $T_5 - T_8$  4B pot cores D25/16, .007" air gap, and bifilar wire windings.

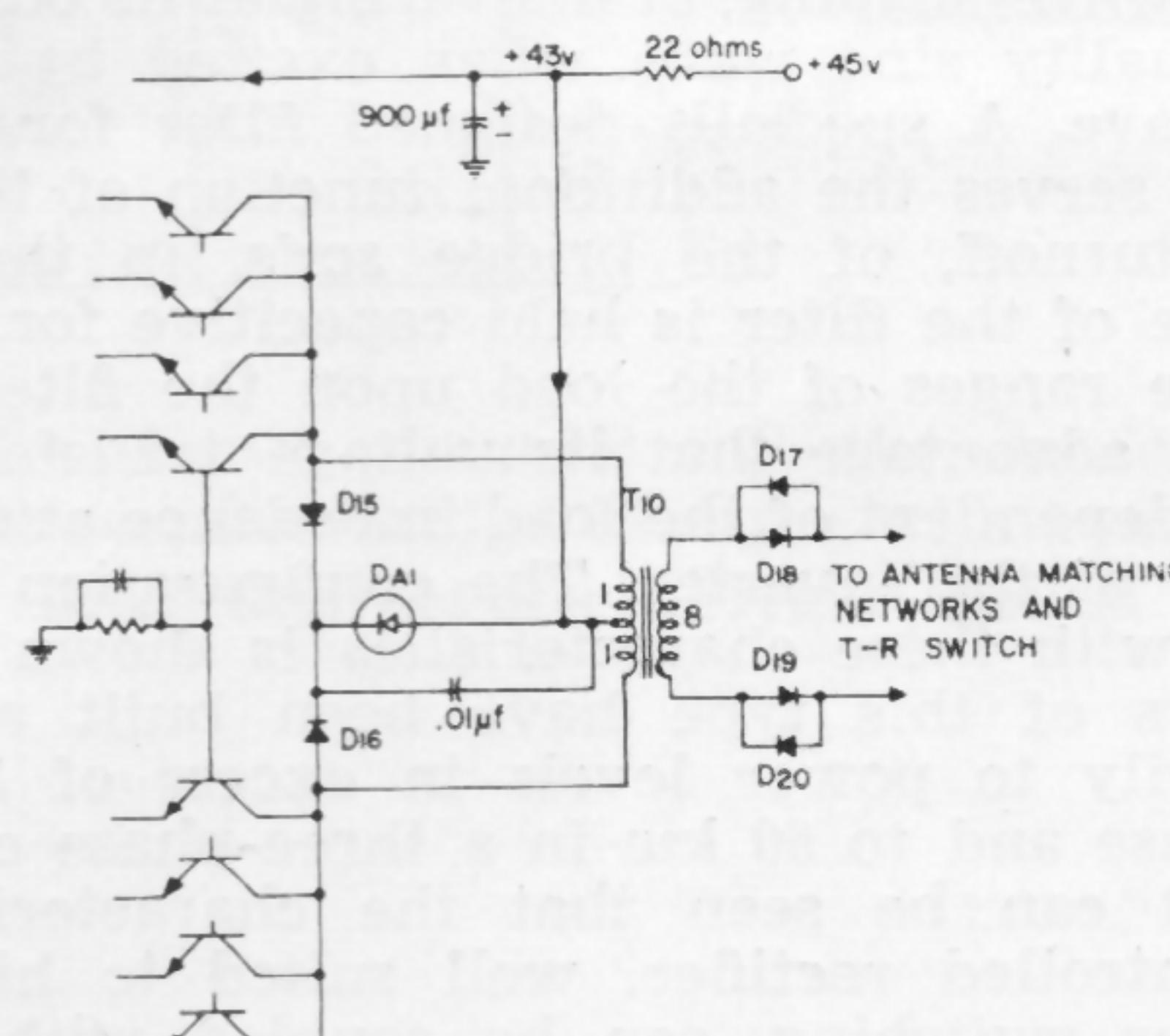


Figure 5—Modified output stage for driving satellite antenna system.  $D_{15}, D_{16} = IN538$ ;  $DA_1 = 20$ -w 45-v zener;  $D_{17} - D_{20} = 1N928$ .

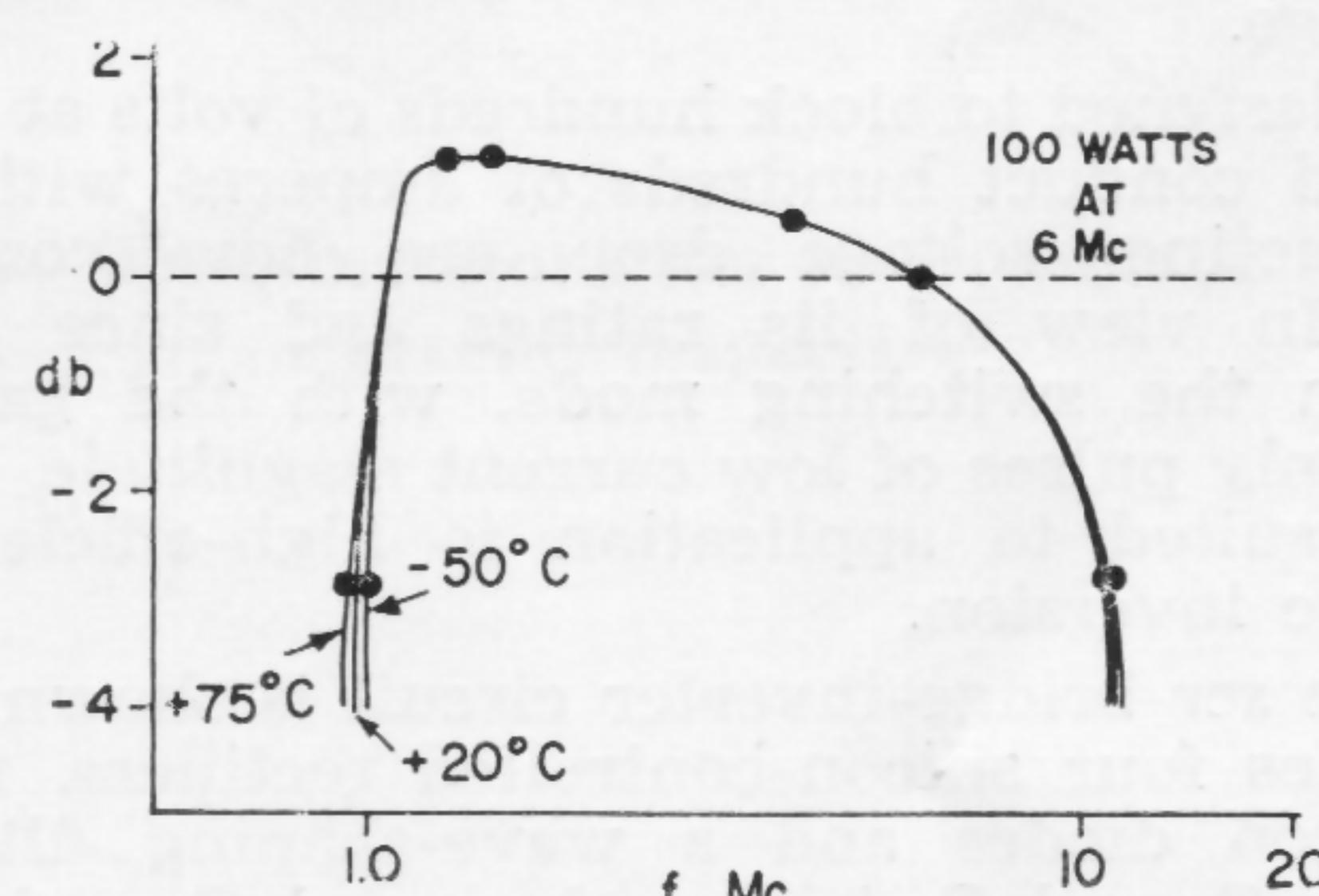


Figure 6—Amplifier power output versus frequency at  $+75^\circ C$ ,  $+25^\circ C$  and  $-50^\circ C$ . Curves refer to an amplifier having output stage of Figure 3.

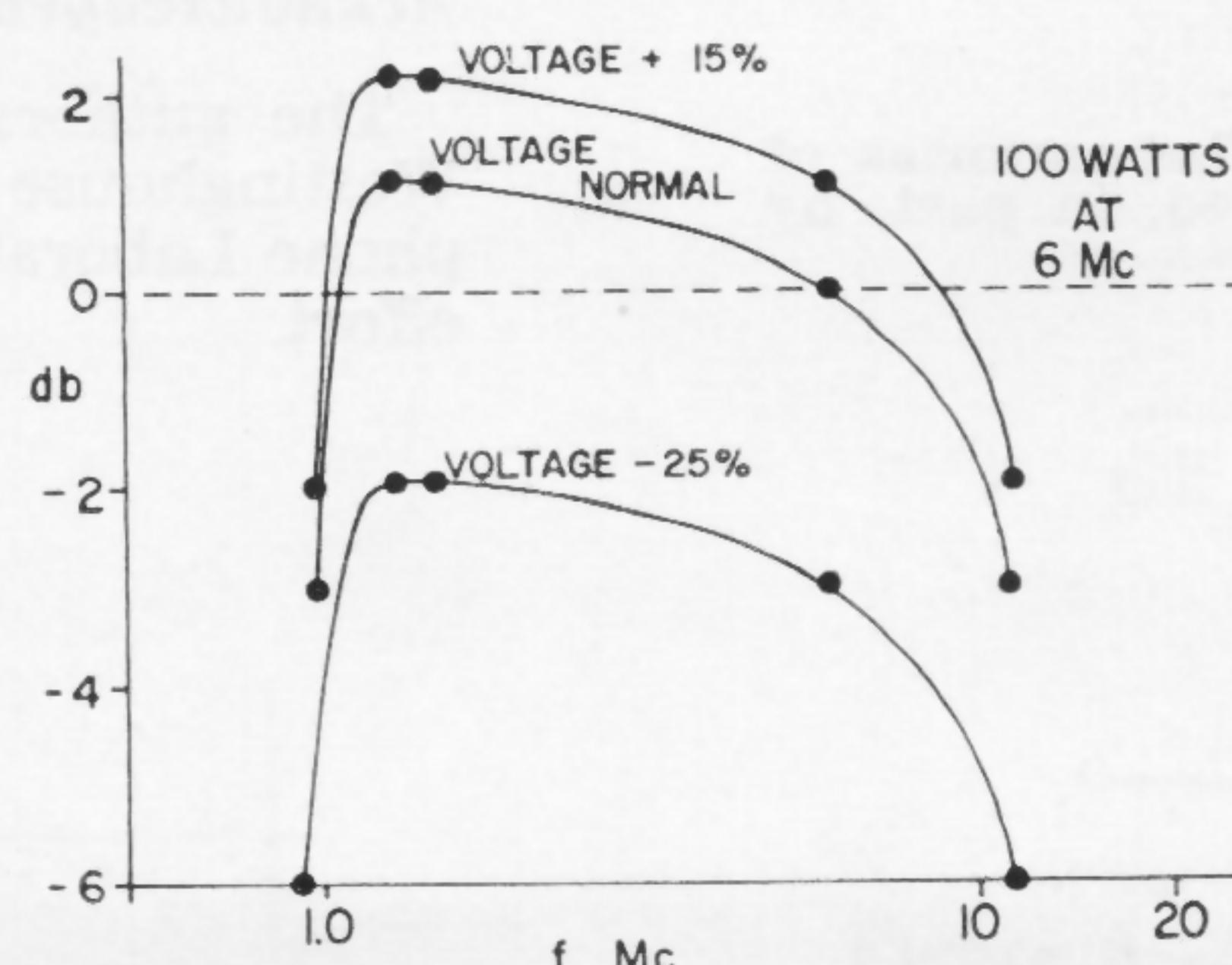


Figure 7—Amplifier power output versus frequency when all power supply voltages are 15% high, normal, and 25% low.

## SESSION X: Design Applications

### FM 10.3: A Unique Silicon-Controlled Rectifier High-Power Inverter With Sine-Wave Output Voltage\*

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SINCE THE ANNOUNCEMENT a few years ago of the *pnpn* switch or silicon-controlled rectifier, there has been widespread activity to develop circuitry that would utilize its unique characteristics in various applications. This paper will discuss the design philosophy and circuit properties of a very high-power static-inverter circuit utilizing the silicon-controlled rectifier as the switching element.

As disclosed in Figure 1, the characteristics of the silicon-controlled rectifier indicate its adaptability to switching applications in high power static inversion. The device is similar to gas thyratrons, etc., in that it has two distinct forward modes, a blocking mode and a conducting mode. It may be triggered into the forward conducting mode from the forward blocking mode by application of a positive pulse to the gate-cathode junction. The device will remain in the forward conducting mode until the anode current is reduced to a very low value or reversed for a time sufficient to regain its forward-blocking characteristics. It cannot normally be returned to its forward-blocking state by control of the gate terminal. Thus, a mechanism must be included in the inverter to turn off conducting *scr*'s when desired. The device exhibits a blocking characteristic when subjected to an applied reverse voltage.

Devices designed to block hundreds of volts at low anode current and conduct hundreds of amperes with low forward-conducting voltage drop are now commercially available. In view of its ratings and since it can be operated in the switching mode, with the gate control requiring only pulses of low current magnitude, the device is ideally suited to application to high-efficiency high-power static inversion.

The basic *scr* bridge-inverter circuit is shown in Figure 2. It includes four silicon-controlled rectifiers, four high-power silicon diodes and a wave-shaping filter. If we assume *scr*'s  $Q_1$  and  $Q_3$  triggered on and  $Q_2$  and  $Q_4$  blocking, current flows from the positive dc supply through  $Q_1$  to terminal A of the wave-shaping filter and from terminal B of the filter through  $Q_3$  to the - dc supply. After a period of time, determined by the nature of the filter, the filter current reverses and flows from the minus of the dc supply through  $CR_3$  to terminal B of the filter

and from terminal A of the filter through  $CR_1$  to the positive of the dc supply. By the end of the half cycle, as determined by the gate-pulse source,  $Q_1$  and  $Q_3$  have regained their blocking characteristics,  $Q_2$  and  $Q_4$  are triggered on, and current flows from the + dc supply through  $Q_2$  and  $Q_4$  and the filter to the minus of the supply until the current again reverses in the filter and flows through  $CR_2$  and  $CR_4$ , while  $Q_2$  and  $Q_4$  regain their blocking characteristics. At the end of the second half cycle  $Q_1$  and  $Q_2$  are triggered on and the cycle repeats. The waveforms of currents and voltages associated with the inverter are shown in Figures 3 and 4. Thus, the function of the *scr*'s then, is to connect the dc supply to the filter with opposite polarity during alternate half cycles, i.e., to provide a square wave of voltage to the filter input terminals. The function of the reverse-current diodes is to provide a path for the reactive component of current in the filter input due to the reactive nature of the input impedance of the filter, as presented to the inverter bridge.

The filter serves multiple purposes. Its obvious function is that of wave-shaping, of delivering at its output terminal a high quality sine wave when excited by the inverter square wave. A specially-designed filter for inverter applications serves the additional function of the commutation, or turnoff, of the bridge *scr*'s, in that the input impedance of the filter is held capacitive for all expected impedance ranges of the load upon the filter. It has the additional advantage that its voltage transfer function is ideally independent of the load impedance at the operating frequency of the inverter. The configuration of one class of filters with these characteristics is shown in Figure 5.

Inverters of this type have been built and operated satisfactorily to power levels in excess of 20 kw for a single phase and to 60 kw in a three-phase configuration.

Thus, it can be seen that the characteristics of the silicon-controlled rectifier, well suited to high-efficiency high-power switching, can be coupled with the unique characteristics of a specially-designed reactive element filter to provide an efficient, simple, reliable high-power static inverter, with an inherent *scr* turn-off mechanism and a high quality sine-wave output voltage.

#### Acknowledgement

The authors are indebted to R. W. Lucky, formerly of Westinghouse Electric Corporation, and now at Bell Telephone Laboratories, for his significant contributions to this effort.

\* This work, performed at the New Products Laboratories of Westinghouse Electric Corporation, was supported, in part, by the Department of the Navy—Bureau of Ships.

<sup>1</sup> Formerly with Westinghouse Electric Corp.

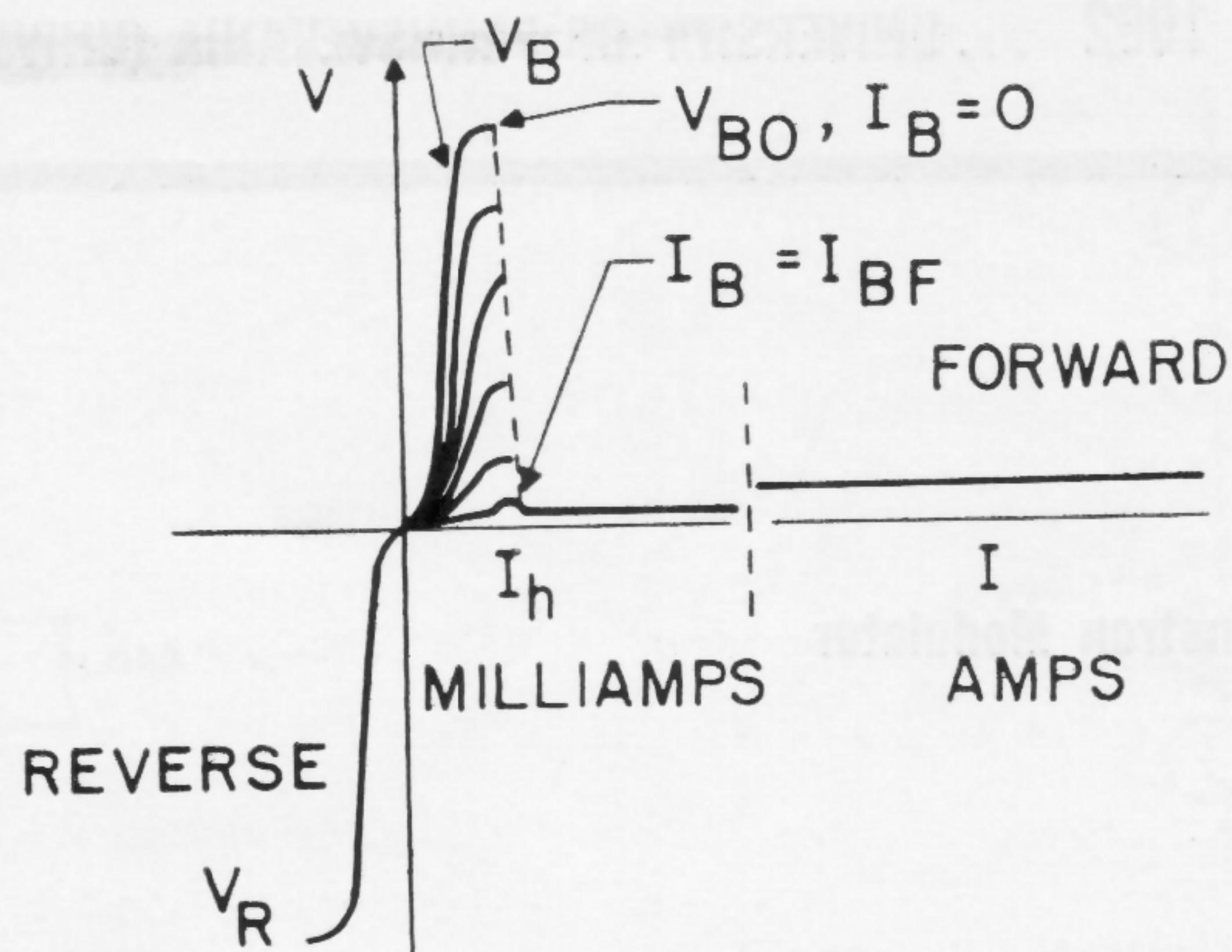


Figure 1—Characteristics of silicon-controlled rectifiers. It will be noted that the low current region is expanded for clarity in displaying the switching regions.

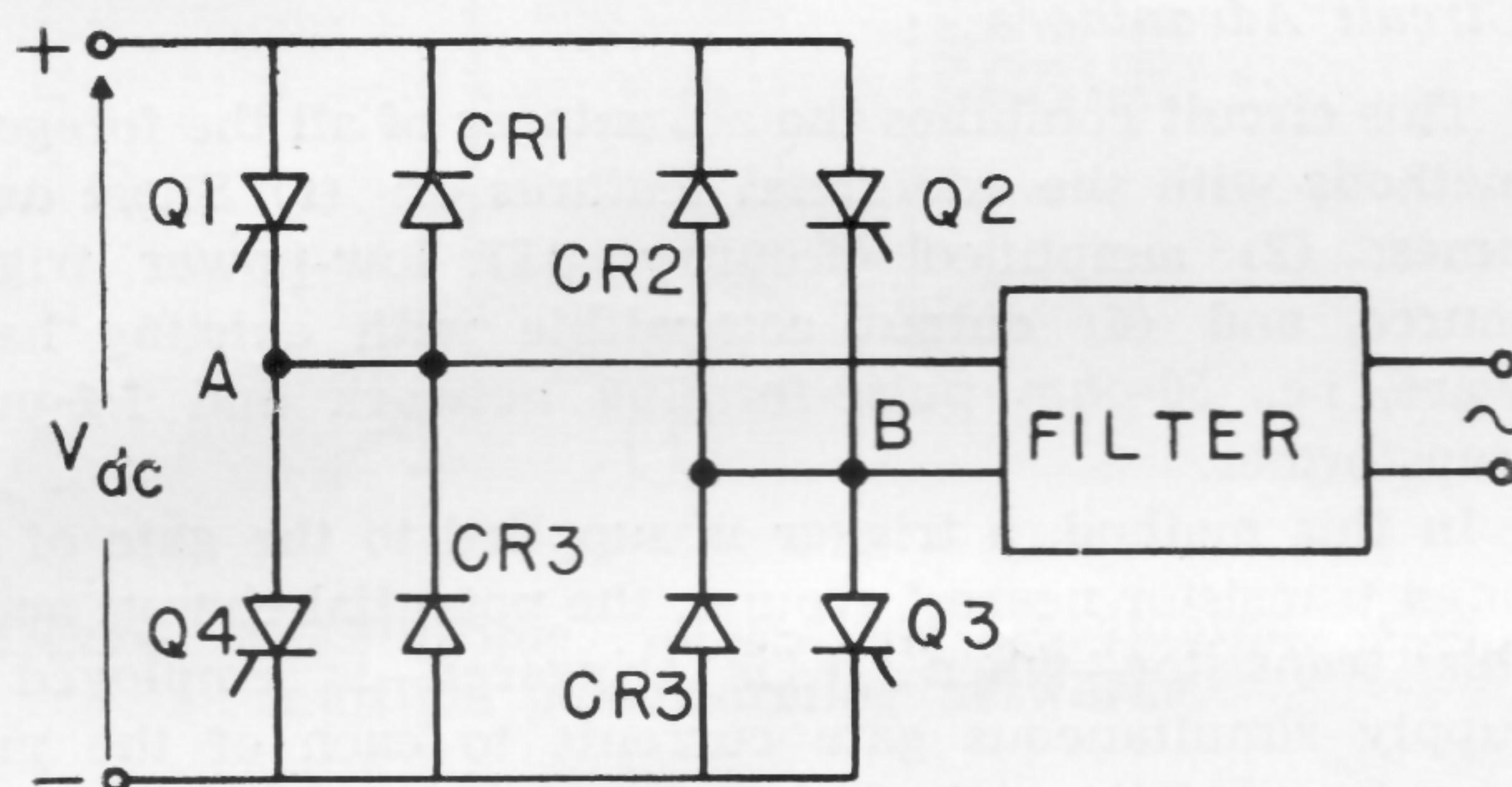


Figure 2—Circuit diagram of the basic silicon-controlled rectifier bridge inverter with commuting filter and reverse current diodes.

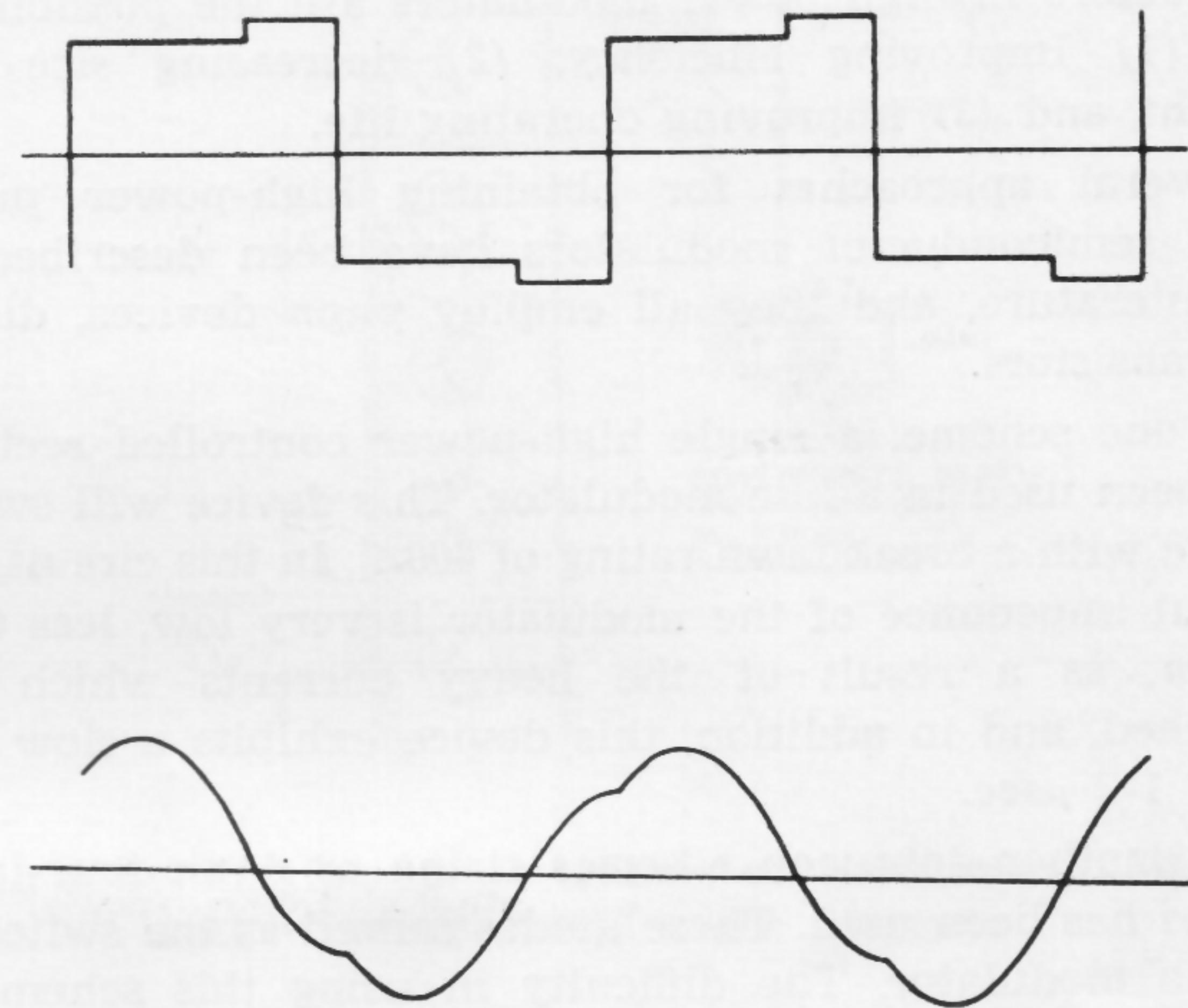


Figure 3—Waveforms of filter input voltage and input current, respectively.

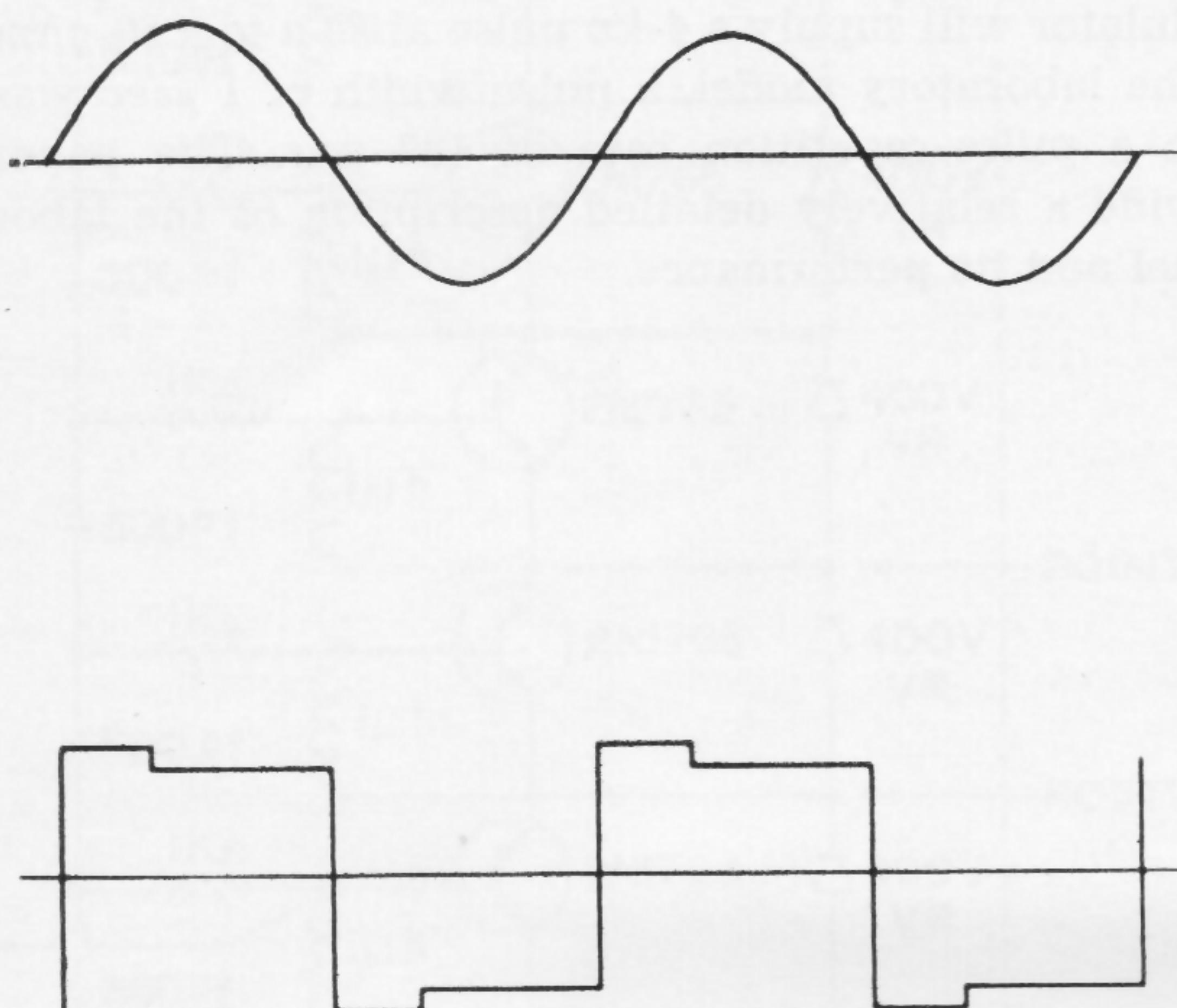


Figure 4—Waveforms of filter input voltage and filter output voltage, respectively.

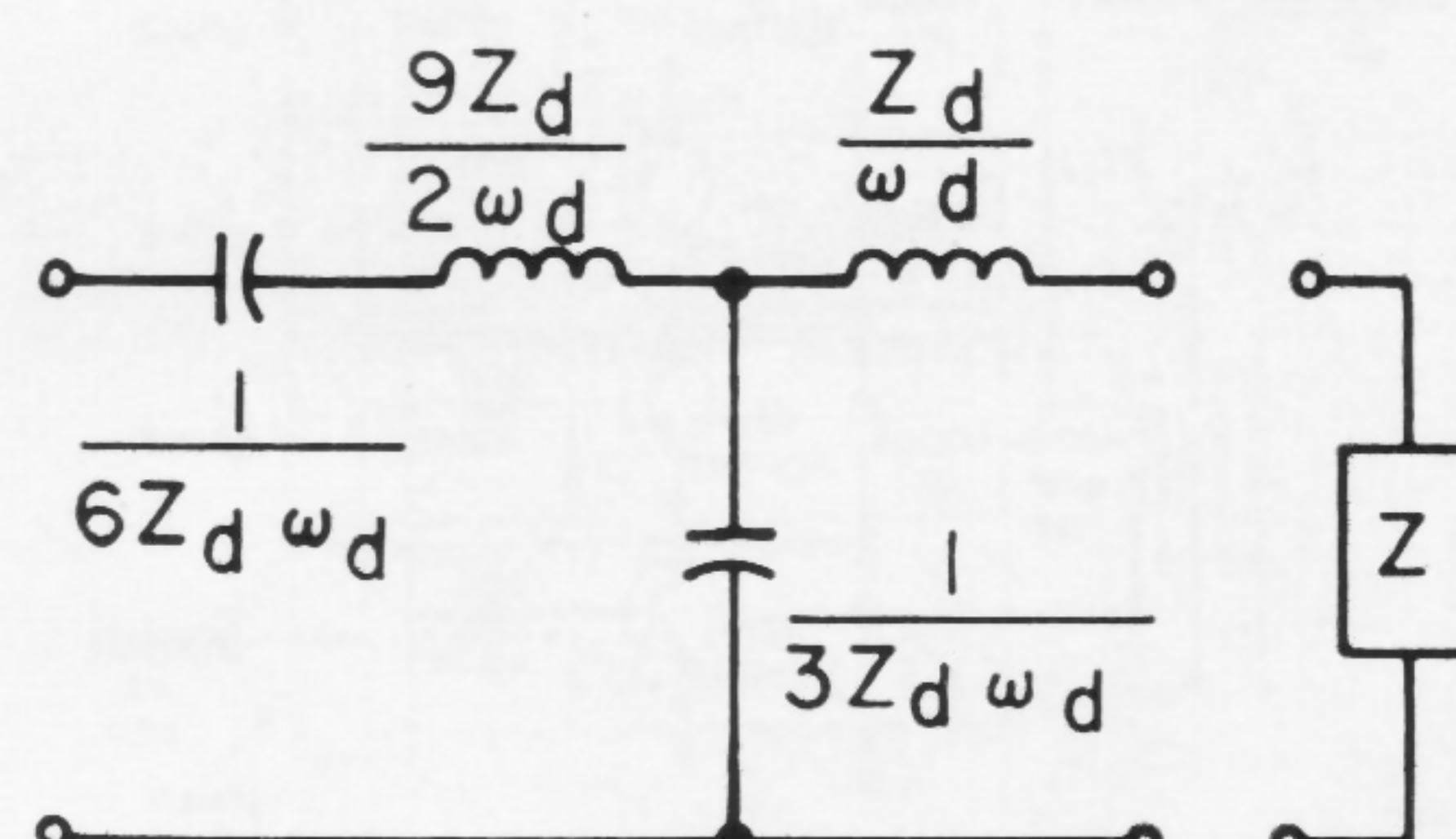


Figure 5—An example of one of the class of four-element commuting filters for inverter applications. Values are in *henries* and *farads*, and are in terms of the filter-design impedance and the inverter-operating frequency.

## SESSION X: Design Applications

### FM 10.4: A 300-kw Semiconductor Magnetron Modulator

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UNTIL RECENTLY the applications of semiconductors have largely been limited to low-power, low-voltage circuits. The primary motives for exploring the use of semiconductors in high power modulators are the possibilities of: (1) Improving efficiency, (2) decreasing size and weight, and (3) improving operating life.

Several approaches for obtaining high-power pulses from semiconductor modulators have been described in the literature, and they all employ *pnpn* devices, diodes or transistors.

In one scheme, a single high-power controlled rectifier has been used in a line modulator. This device will switch 1500  $a$  with a breakdown rating of 400 v. In this circuit, the output impedance of the modulator is very low, less than 1-ohm, as a result of the heavy currents which are switched, and in addition, this device exhibits a slow rise time, 1-2  $\mu$ sec.

In another approach a series string of *pnpn* four-layer diodes has been used. These diodes served as the switch in a line modulator. The difficulty in using this scheme is the large signal required to trigger the string of *pnpn* diodes and the long delay times between the trigger and the output current pulse. The four-layer diodes are suitably fast for magnetron modulator service.

Still another approach makes use of *pnpn* transistor switches in a series string in a line modulator. In this circuit, a multiwinding transformer supplies gate current to each *pnpn* transistor in the string. This method is suitable for two or three devices in series; however, if more than three are required in series, the task of supplying gate current is very difficult.

A method of using the *pnpn* transistors in a string with gate current supplied to a limited number of devices in

<sup>‡</sup> W. E. Type 2N1765.

the string, with the remaining devices switching when breakdown is exceeded, has also been successfully used; however, the delay time has been found to be excessive.

This paper will describe a modulator which is suitable for supplying pulse powers in excess of 300 kw for magnetrons and other applications. The semiconductor used is a *pnpn* transistor switch<sup>‡</sup> capable of switching currents of 80  $a$  in less than 100 nsec.

#### Circuit Advantages

This circuit combines the advantages of all the foregoing methods with the additional features of: (1) Short delay times; (2) simplified circuitry; (3) low-power trigger source, and (4) output compatible with existing hardware, i.e., 50-ohm pulse-forming network and 1:4-pulse transformer.

In this method, a trigger is supplied to the gate of the *pnpn* transistor nearest ground; the potential change across this transistor—when it is triggered—is employed to supply simultaneous gate currents to each of the *pnpn* transistors in the string.

The voltage across each *pnpn* transistor in off-state is stabilized by the use of a voltage-regulator diode across each device. This voltage-regulator diode also performs the function of transferring the change in potential of the *pnpn* transistor nearest ground to the *n* emitter of each *pnpn* transistor in the string, which causes current to be supplied simultaneously to each gate in the string.

Preliminary results with a laboratory model indicate a series string of twenty *pnpn* transistor switches<sup>‡</sup> in a line modulator will supply a 4-kv pulse at 80  $a$  to a 50-ohm load. In the laboratory model, a pulse width of 1  $\mu$ sec was used with a pulse-repetition rate of 100 pps. The paper will provide a relatively detailed description of the laboratory model and its performance.

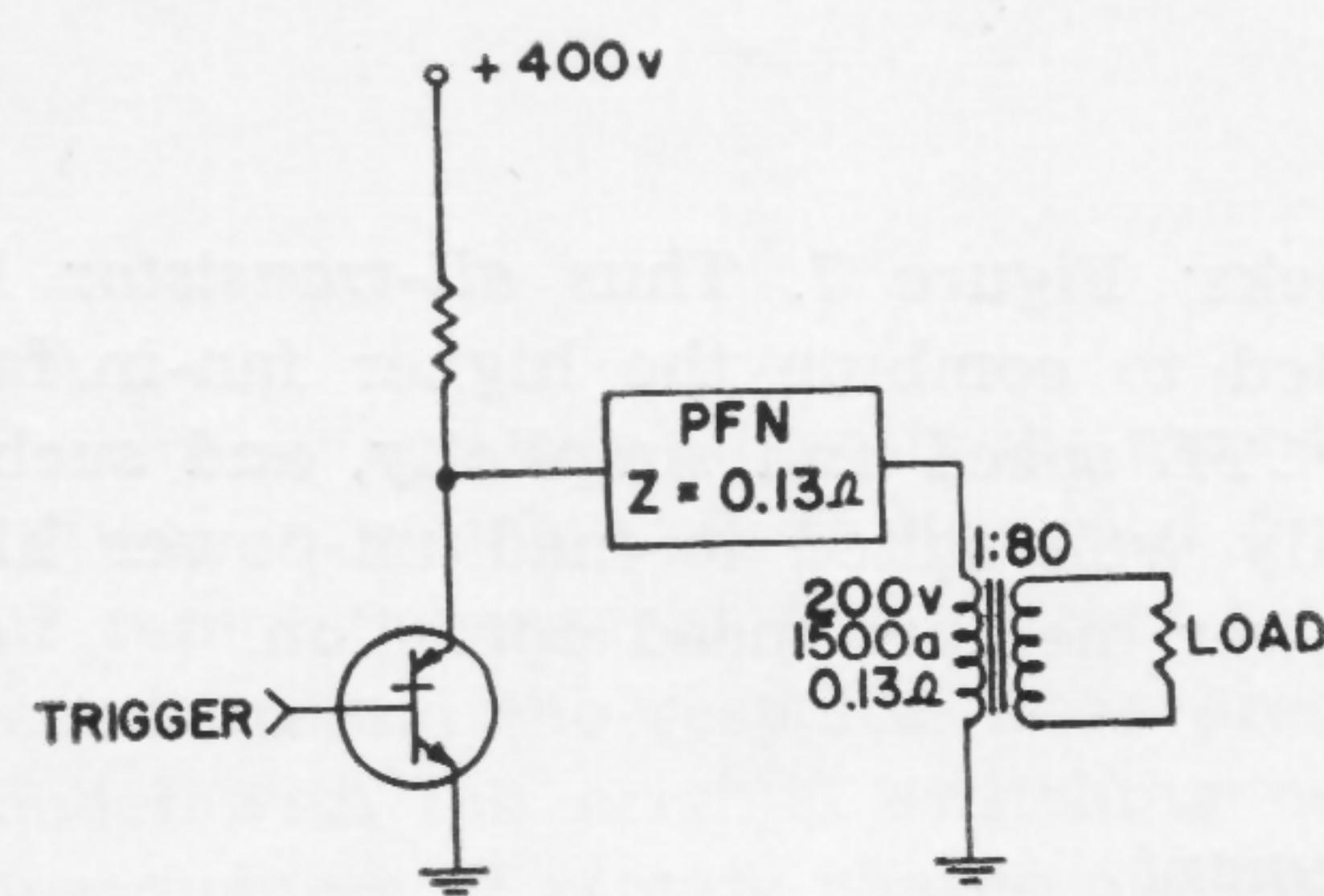


Figure 1—Simple line-type modulator using a single *pnpn* transistor.

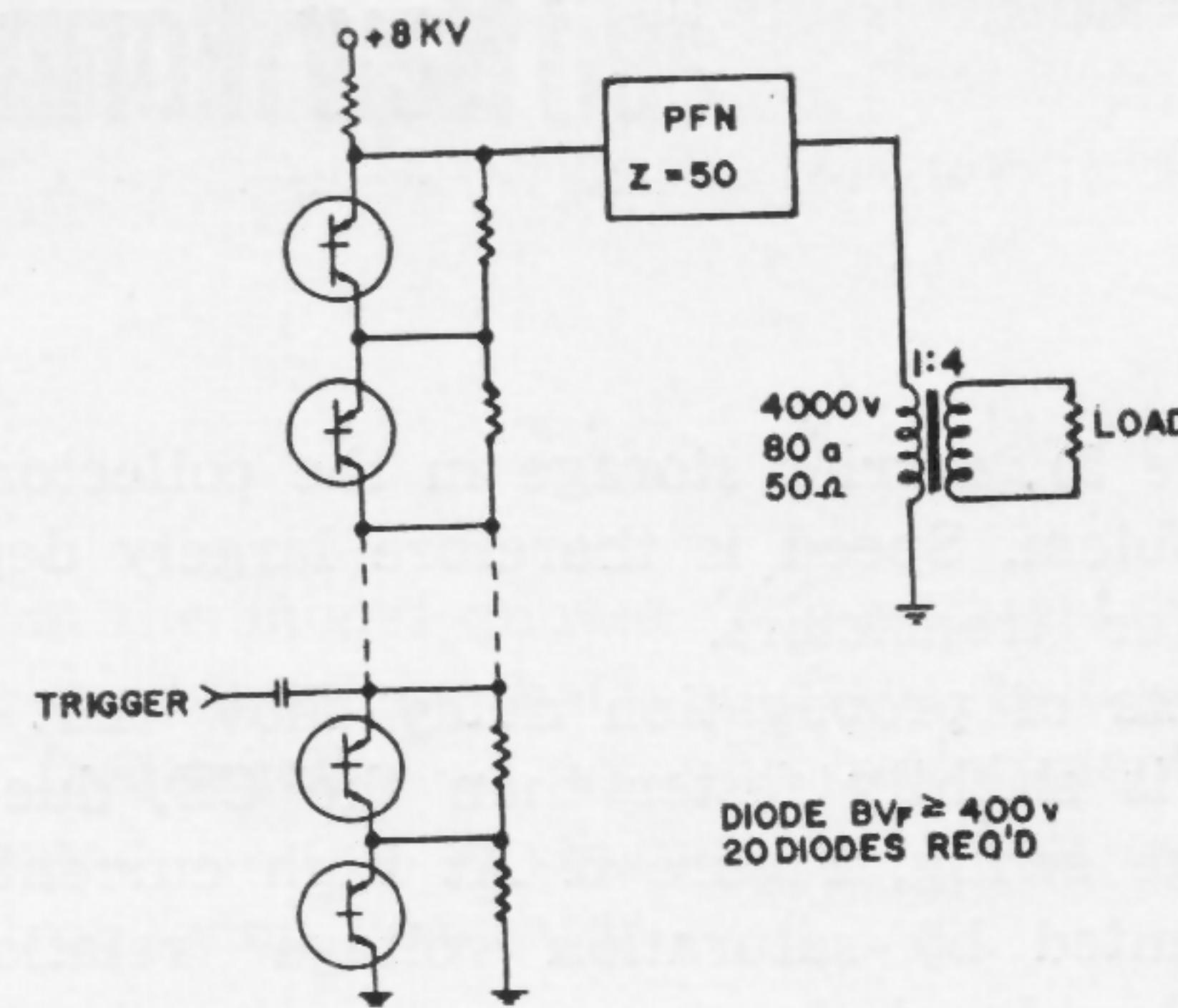


Figure 2—Multiple *pnpn*-diode modulator with a single pulse-forming network.

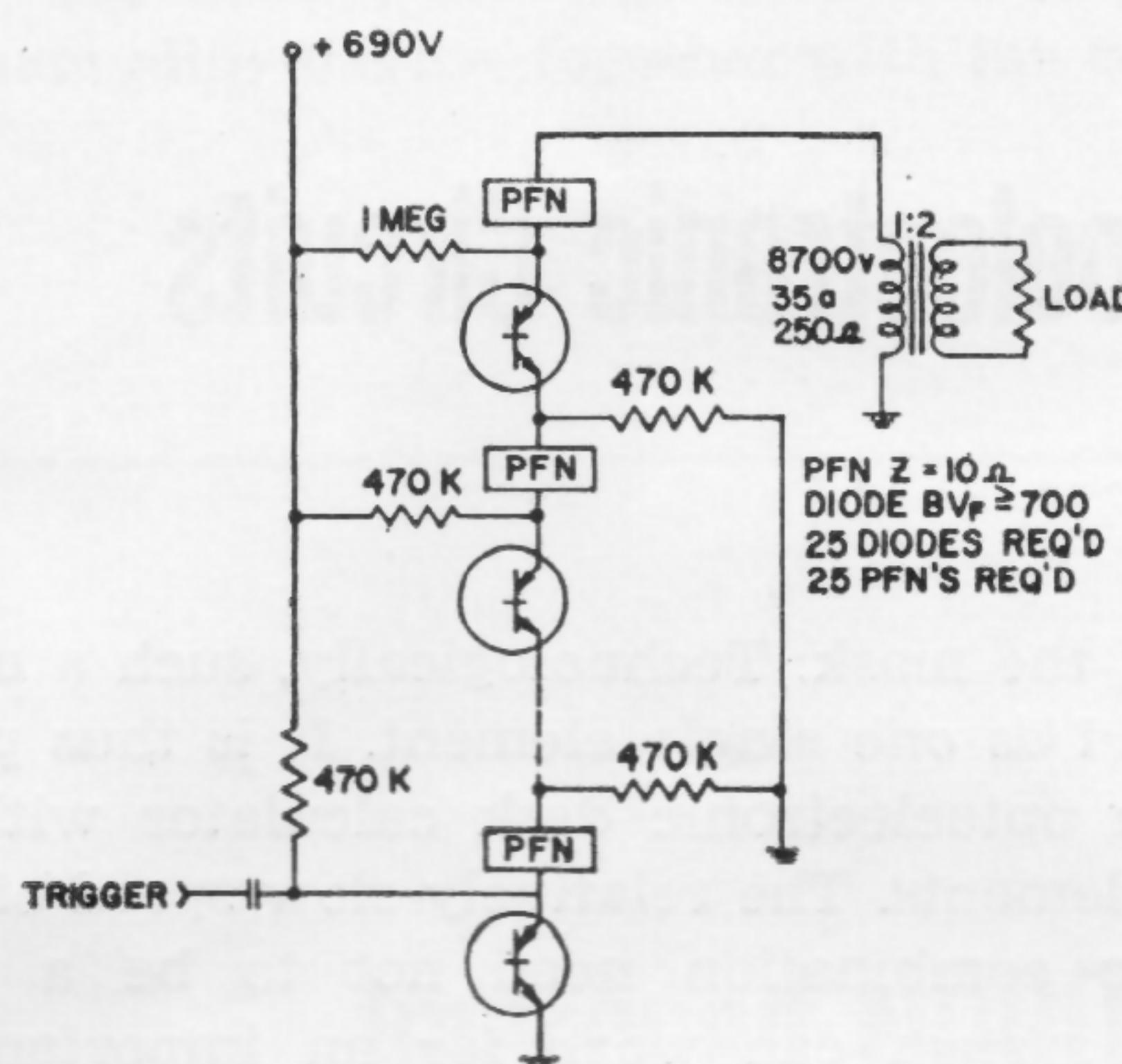


Figure 3—Multiple *pnpn*-diode modulator with multiple pulse-forming networks.

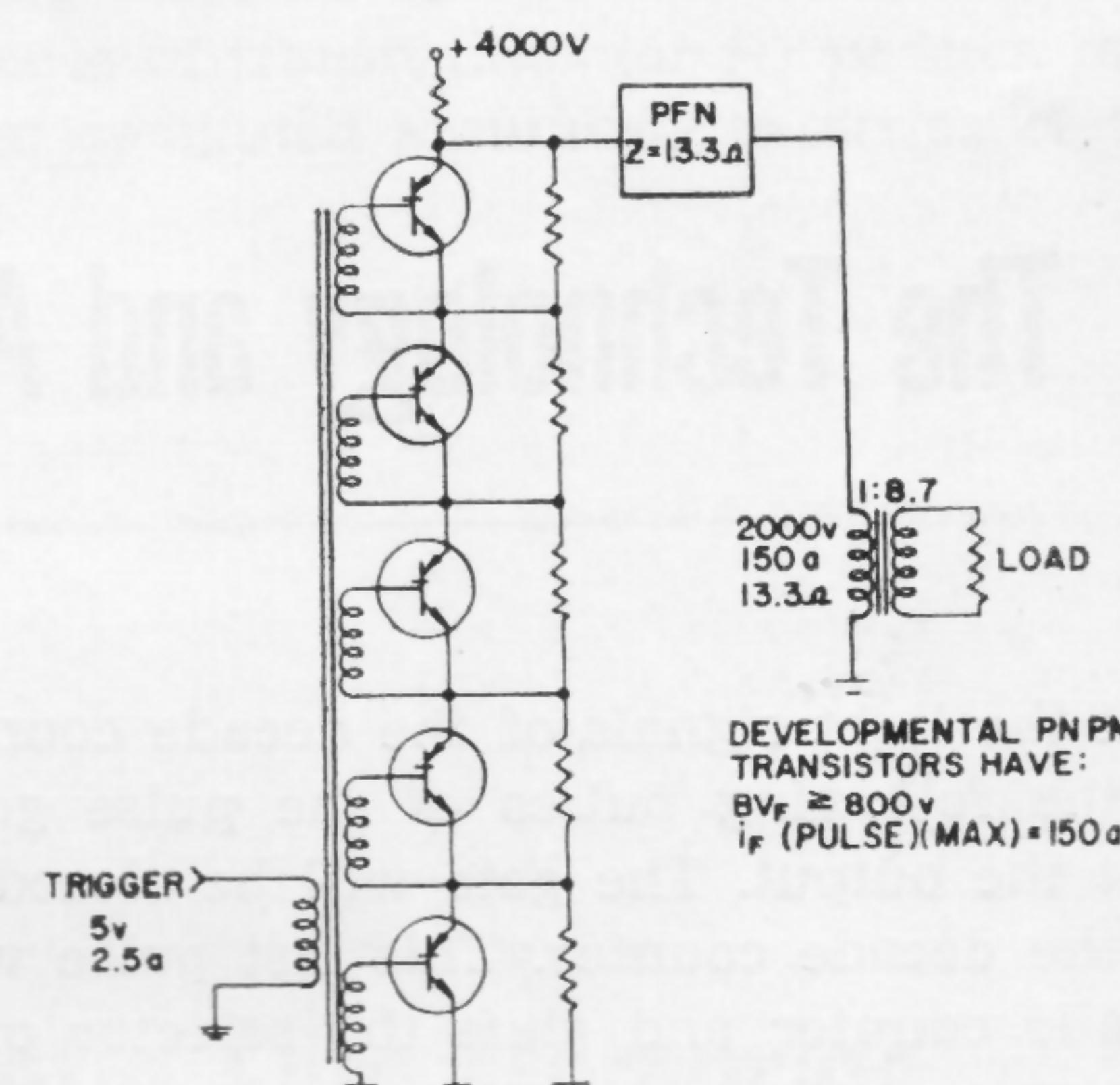


Figure 4—Multiple *pnpn*-transistor modulator using multiwinding transformer trigger.

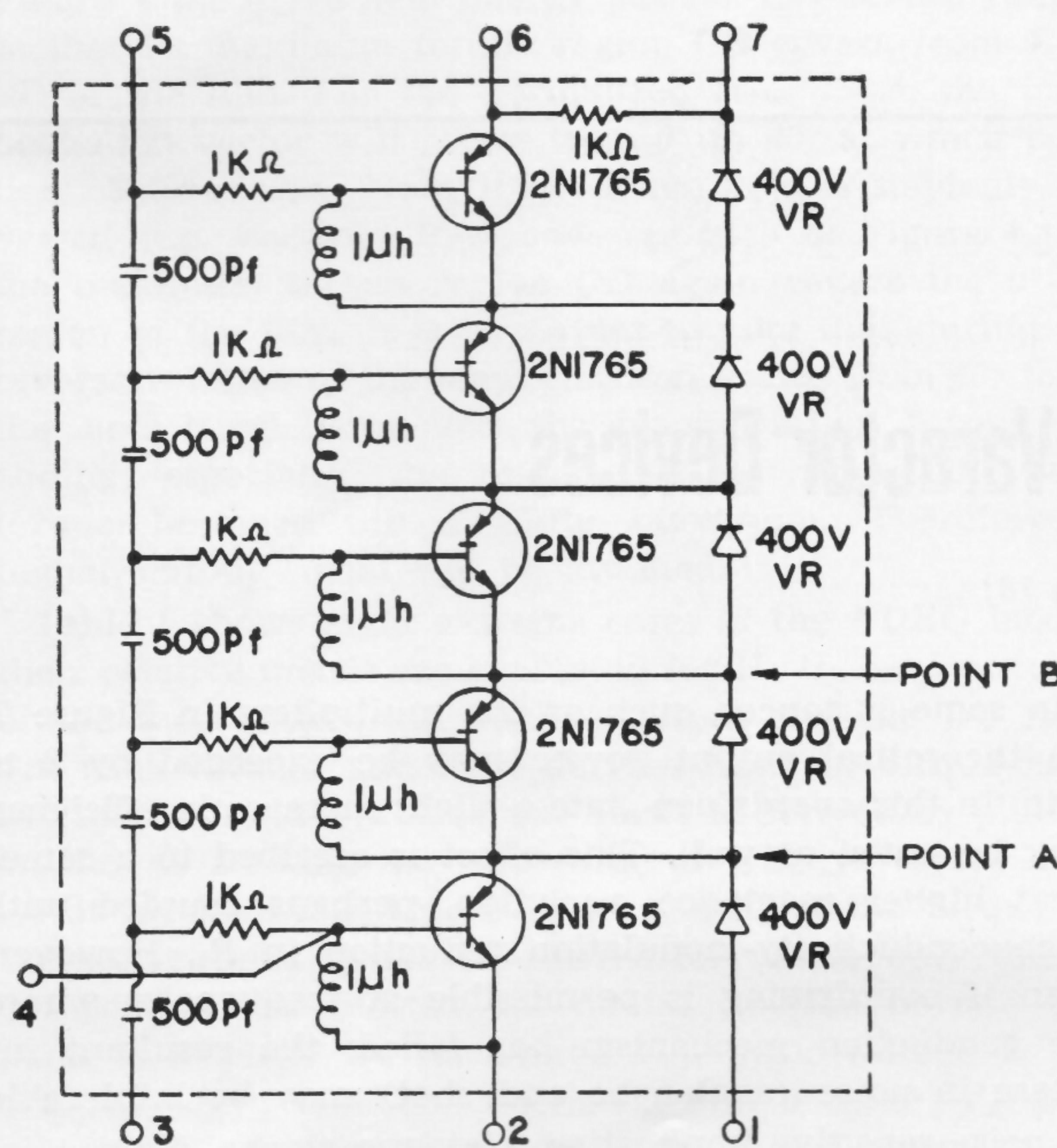


Figure 5—Basic 2000-v switch module using multiple *pnpn* transistor switches‡.

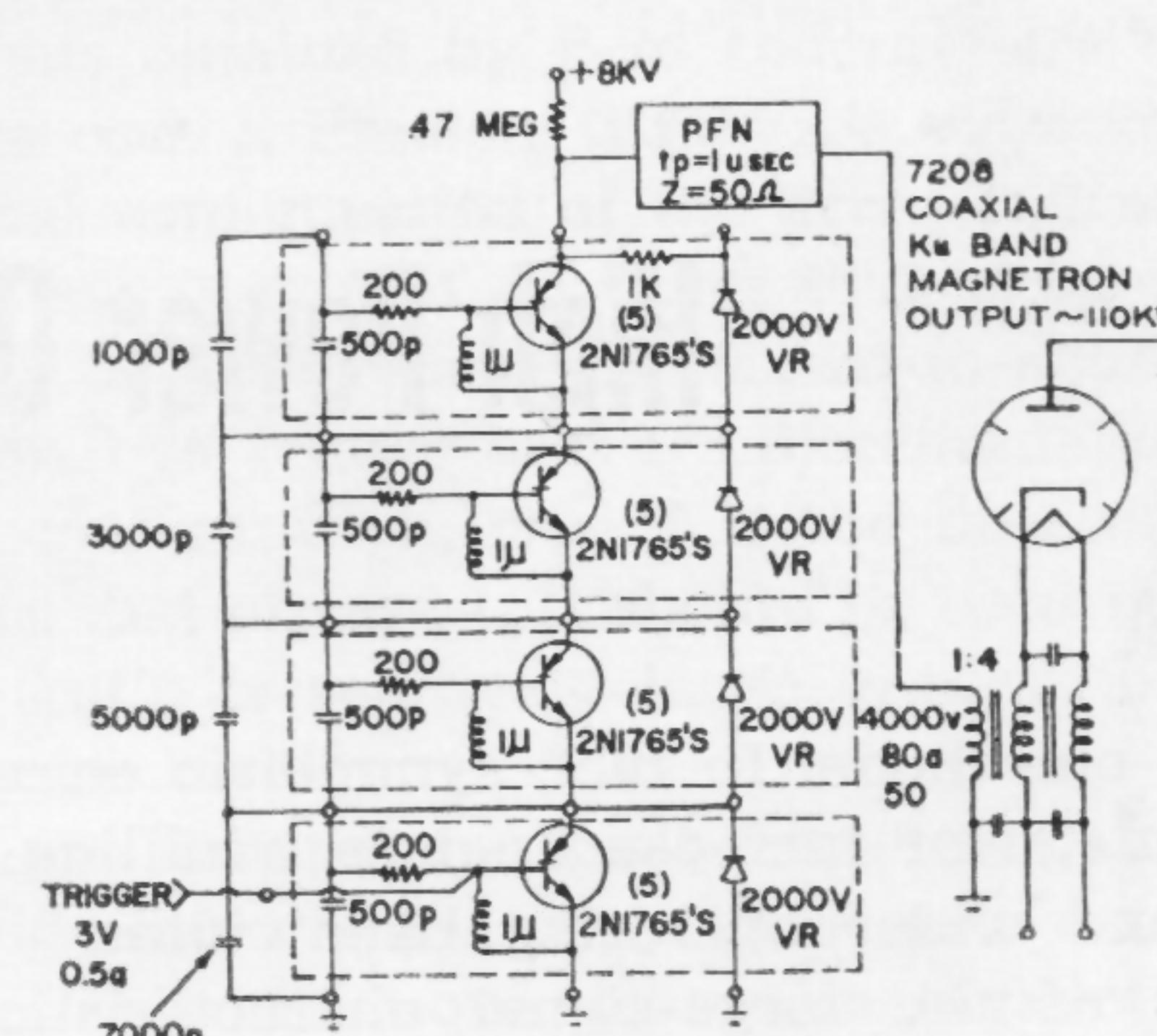


Figure 6—Developmental 300-kw semiconductor modulator using multiple *pnpn* transistor switches‡.

# New Forms of All-Transistor Logic

[Continued from page 10]

switch (Figure 5), carrier storage in the collector region causes no problem. Speed is therefore largely dependent on the inverter transistors.

Measurements of propagation delay show that the CC configuration is slightly faster than the CE, due to the smaller voltage swing; Figure 6. At high current levels, fan-out is limited by saturation voltage (relation 1 of Figure 4), at low levels by normal current gain (relation 2 of Figure 4).

A 30-Mc shift register was demonstrated using the TTL

building blocks; Figure 7. Thus *all-transistor* logic has been expanded to combine the higher fan-in/fan-out of DTL with DCTL speed and simplicity, and such systems are as equally well suited to medium-power high-speed as to low-power medium-speed operation.

## Acknowledgement

Acknowledgment is gratefully made of the contributions of Robert Norman and Donald Farina.

# The Technology and Application of Optoelectronic Circuits

[Continued from page 14]

coincidence of the light signals of the decade counter and the decoder the following pulses of the pulse generator will appear at the output. The gate will be closed by the last pulse of the decade counter. This last pulse will also reset the decade counter and shift the selector over one position.

Another example of a logic circuit is the multiplication matrix illustrated in Figure 6. In Figures 7 and 8 the electrode patterns of the el and pc layers are shown. The matrix is obtained by placing the el and pc layers upon each other with an appropriate mask in between. A multiplication matrix can be converted into an adding matrix

by changing the mask. Technologically, such a matrix can be considered as one single element. It is thus possible to construct an optoelectronic desk calculator with a small number of elements. The relatively slow speed of response of the el-pc combination need not to be a limitation because the system can work for an important part in parallel. Multiplication of two decimal numbers of ten digits can be made in the order of a second.

## Acknowledgement

The author is grateful to F. M. Beeftink, University of Utrecht, for his important contributions to this paper.

# High Power Operation of Varactor Devices

[Continued from page 18]

as that set by one diode. In fact, symmetric circuits have a triple advantage of increased power handling, simpler construction and wider operating bandwidths.

An analysis of the large-signal characteristics of an abrupt-junction upper-sideband upconverter indicates that the device will be linear over a wide range of input power, provided the pump current remains sensibly constant<sup>4</sup>. The dynamic range under these conditions is described in Figure 8, together with the maximum output power and a comparison with an experimental amplifier.

In some instances, such as the multipliers in Figure 7, the theoretical output power may be exceeded by 2 to 6 db. In this overdriven state a slight increase in efficiency may be noted as well. This effect is ascribed to a somewhat higher reactance variation, perhaps coupled with some conductivity-modulation reduction in  $R_s$ . However, even if overdriving is permissible at frequencies where the conduction mechanism has failed, the resultant increase in noise (avalanche and shot) may be intolerable in noise-sensitive applications (atomic clocks, etc.).

# Charge Definition of Transistor Properties

[Continued from page 30]

form quite closely and also suggests the modified switching network given in which  $C_2R_2$  is provided for removal, or supply, of remote charge at the correct rate. Turnoff is then speeded up and the response is as predicted by the simple model with the original switching network.

The consequences of remote charge are also evident for some devices in measurements aimed at deriving physical parameters, e.g., basewidth from transit time. With sinusoidal excitation, the bridge of Figure 4b may be used for determination of base transit time (equal to  $C_r$  on adjustment for null), if the device is effectively one-dimensional. Remote charge results in the deduced transit time ( $C_r$ ) being both artificially large and frequency dependent. Use of the modified model of Figure 3 enables the effect of remote charge to be discounted and a more physically meaningful transit time to be deduced. Figure 6 shows the frequency dependence of  $C_r$  as measured for a particular uniform base alloy device, together with the corresponding

data from the model quoted. The parameters of the model may be evaluated by balancing the bridge of Figure 4b at two frequencies, or by null adjustment of the more complicated bridge of Figure 4d when excited with a sweep-frequency generator.

It should be noted that the charge/current linearity of the transistor models discussed is in some devices grossly violated at high currents owing to interaction between depletion layer and base region charge, in addition to high level injection effects. In certain drift transistors such interaction is very great for currents above a critical value: Space charge due to current flow through a reverse-biased collector-depletion layer causes shift and narrowing of this layer, thus widening the base and consequently increasing the base charge and transit time. High current dependence of transit time (or  $f_T$ ) of such drift transistors has been computed accurately in terms of this effect.

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## Improved NDRO Modes for Magnetic Film Memories

[Continued from page 44]

way to produce more useful torque is in need. Based on this reasoning, a *field reversal mode* is created. In *a* of Figure 4 the drive field energy pattern has been arranged so that its maximum torque region *CD* covers from  $0^\circ$  to  $60^\circ$  of the film. For the normalized  $H_{120^\circ} = .5$ , the magnetization vector will rotate from  $0^\circ$  to  $40^\circ$  at which position  $\partial E_t / \partial \theta = 0_{min}$ . Now, if the drive field is suddenly reversed (i.e., becomes  $H_{300^\circ}$ ), we see in *b* of Figure 4 that the maximum torque region *CD* again covers the  $0^\circ$ - $60^\circ$  region of the film. It is important to note that during the reverse rotation of the magnetization vector from  $40^\circ$  to  $0^\circ$ , the anisotropy slope and the magnetization torque are adding; especially, the region, *AF*, is where the total torque becomes the absolute maximum. Therefore, a higher output signal can be attained.

Table I shows eight extreme cases of the NDRO modes; their relative merits are evaluated for  $H_\theta / H_K = .5$  in terms of the theoretical peak voltage output and the  $1/0$  ratio. The peak voltage values are derived from the torque curve of Figures 5 and 6. The torque curve is derived by plotting on the  $\Delta\theta/2$  radial line the value of  $\Delta E_t / \Delta \theta$  versus  $\theta$  for  $\Delta\theta$  at  $10^\circ$  intervals. Curve 1 of Figure 5 is the torque for the conventional transverse drive for which only the  $0^\circ$ - $30^\circ$  portion was plotted, for no information beyond that point is needed. We now have  $V_{S11}$  peak voltage  $\approx .150$  arbitrary units from the *x*-axis (i.e., the  $0^\circ$  axis);  $V_{S1}$  peak voltage  $\approx .023$  arbitrary unit from the *y*-axis (i.e., the

$90^\circ$  axis). Curve 2 shows the torque for the cases by *field reversal*. The torque curves for the angular drive cases are shown in Figure 6.

Case I of Table I represents transverse drive with the drive and sense lines orthogonally located. It is taken as the reference for comparison because this is the most commonly used condition, though it is not optimum. When other cases are compared against it, we see that generally the outputs obtained by *field reversal* are better than the reference case 1. Finally, it may be concluded that for the orthogonal configuration of the drive and sense lines, case 2, which has a gain of 6.5 times that of case 1, is the best. It should be used when the signal-to-noise ratio is relatively small to realize best  $1/0$  discrimination. And for the parallel configuration, case 8 is the best since the gain is 14.8 times that of case 1. It should be used when the signal-to-noise ratio is relatively large to elevate the signal out of the noise level.

Films are inherently small-signal devices. Costly high-gain, wide-band sense amplifiers are needed in a film memory. This technique, to obtain higher output without extra hardware, should be very useful.

### Acknowledgement

The author wishes to thank B. I. Bertleson and L. R. Adams for their encouragement, and H. Chang and W. L. Shevel for the fruitful discussions.

# Tunnel-Diode Balanced-Pair Switching Characteristics

[Continued from page 54]

repetition-rate range. A tabulation of empirically determined fan power as a function of frequency appears in

Peak Current	Repetition Rate	Fan Power	Coupling Resistor
5 ma	150-Mc	4	300 ohms
50 ma	150-Mc	4	50 ohms
50 ma	750-Mc	2	50 ohms
50 ma	1,200-Mc	1	50 ohms

Table I

Table I. Waveforms of the 150-Mc circuits are shown in Figure 5.

Two scale-of-two counters and two three-bit end-around shift registers were constructed using 50-ma tunnel-diode balanced-pair circuits energized by three-phase sinusoidal power supplies. The counters were operated at 150- and 450-Mc repetition rates. The shift registers were operated at 150-Mc. The packaging technique involved is illustrated in Figure 6.

# An Extremely Low-Noise 6-Gc Nondegenerate Parametric Amplifier

[Continued from page 60]

sideband noise figure of the mixer and if amplifier was 7.5 db, the measured result is very close to the expected value. The bandwidth is limited mainly by the idler circuit: The amplifier can be tuned over 260 Mc simply by tuning either the pump frequency or the idler circuit.

To operate the amplifier at liquid nitrogen temperature, with less refined diodes, the amplifier was completely readjusted at room temperature so that it would tune at  $-1\text{ v}$  of bias when its temperature was lowered to  $77^\circ\text{K}$ ; however, with recent diodes, this readjustment has been eliminated, since the amplifier can be retuned by minor adjustment of the trimmers in the idler and pump circuits. The measured overall noise temperature was less than  $60^\circ\text{K}$ ; of this more than  $20^\circ\text{K}$  was contributed by the circulator and the mixer. Since the performance of the

amplifier was temperature sensitive, its temperature had to be maintained constant to within  $10^\circ\text{K}$ . The pump power used was 5.5 mw at 23 Gc to achieve a gain of 20 db and a system noise temperature of  $60^\circ\text{K}$ .

So far five room temperature amplifiers and four liquid nitrogen units have been built; in each case the performance was close to that described.

## Acknowledgments

The author wishes to express his appreciation to S. Plauski who made many of the measurements and amplifier adjustments, to N. C. Vanderwal who supplied the gallium arsenide diodes, and to R. G. Voss who completed the mechanical designs.

# Sensitive Tunnel-Diode Pressure Transducers

[Continued from page 74]

flat portion of the current-voltage characteristic of the diode. In this case, there is no sudden jump since the curve is continuous.

Figure 5 shows plots of the voltage across an experimental silicon tunnel diode versus pressure. Curves A to E were obtained by varying bias currents and shunt resistor  $R_s$ . If the magnitude of the shunt resistor is made nearly equal to the negative resistance of the diode, the sensitivity to pressure of the device is large indeed. For example, when hydrostatic pressure was applied directly to a silicon diode, it was possible to get a 2.5-mv signal for a pressure change of 10 psi. This may be compared to a signal 1000 times smaller if the diode is operated simply in the positive resistance region. It is also possible to change the region of elevated sensitivity as desired by applying an appropriate bias current. However, when  $R_s$  exceeds the value of the negative resistance of the diode, switching takes place<sup>6</sup>. This switching is evidenced by curve E. The position of curve E can be

shifted to other pressure ranges also by applying a different bias current.

Germanium diodes, when stabilized, give a current-voltage characteristic as shown in Figure 6. It is important to notice that the peak current decreases with increasing pressure, whereas it increases for Si diodes. The per cent changes also differ. For a 20,000-psi hydrostatic pressure change, the peak current in a Si diode rises by 2.5%, whereas for Ge, it decreases by 15%. The diode-resistor combination characteristics for a germanium diode are shown in Figure 7. GaAs and GaSb diodes are even more sensitive to pressure. The changes in peak current for those diodes, in the above pressure range, were found to be 20% and 39%, respectively. Data of Figure 2 show a sensitivity about 50 times that of commercially available load cells.

It has been shown that adjustment of circuit parameters, i.e., shunt resistance and current through the tunnel diode-resistor combination, makes it possible to obtain extraordinarily sensitive and versatile pressure transducers with controllable sensitivity and pressure ranges.

# Circuit Design and Parameters in Thin-Film Technology

[Continued from page 90]

$\pm 5\%$  of the nominal value. This will allow the utilization of greater fan-out factors or lower beta transistors in these thin-film panels. The uniformity of circuit performance as well as the absence of any evidence of interlayer feed-

back effects in the dense packing arrangement indicate the potential of the integrated panel approach. A 1200-transistor data-flow model incorporating 25 of the film circuit panels is under development.







## Notes

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## SCOPE OF CONFERENCE

THE 1962 INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE features ten daytime sessions at the University of Pennsylvania (Irvine Auditorium and University Museum) devoted to broad advances in the field of solid-state device applications and circuits.

FORTY-SIX papers will be presented. Subject areas include logic, microwave parametric circuits, new devices and device characterization, memory, high-speed switching, low-noise amplification, tunnel-diode applications, digital transmission, functional components, and design applications.

THE FORMAL OPENING of the conference includes an invited address on active homogeneous semiconductor devices.

ELEVEN INFORMAL SESSIONS, conducted by international leaders in the solid-state field, will be held on Wednesday and Thursday evenings in the Sheraton Hotel to provide registrants an opportunity to discuss the latest developments in the art.

AMONG THE TOPICS on the agenda are distributed logic, interconnection problems, microwave power sources, magnetic thin-film memories, noisemanship, and charge-control characterization of semiconductor devices. Additional discussion periods cover nanosecond circuitry, optical masers, thin-film magnetic and superconductive techniques in future computers, low-level signal processing, and high-power high-speed switching.

## Conference DIGEST OF TECHNICAL PAPERS

ADDITIONAL COPIES of the DIGEST OF TECHNICAL PAPERS, priced at \$5.00 per copy, may be obtained from H. G. Sparks, The Moore School of Electrical Engineering, University of Pennsylvania, 200 South 33 St., Philadelphia 4, Pa. Remittance (payable in U. S. currency) should be made to the order of: Solid-State Circuits Conference.

## Conference-Informal Session Locations

THE CONFERENCE is being held on the campus of the University of Pennsylvania in the Irvine Auditorium and in the University Museum.

IRVINE AUDITORIUM is located at the northwest corner of 34th and Spruce Streets; the University Museum is just east of the southeast corner of 34th and Spruce Streets, Philadelphia, Pennsylvania.

THE INFORMAL Wednesday-Thursday evening sessions will be held in the Sheraton Hotel, 1725 Pennsylvania Boulevard, in central Philadelphia. Central Philadelphia can be reached by bus route 42; the 30th Street station of the Pennsylvania Railroad is less than a mile from the University Campus.

## Luncheons . . . Open-House Cocktail Hours

LUNCHEONS on Wednesday and Thursday will be served to a limited number in the University Museum, University of Pennsylvania.

OPEN-HOUSE COCKTAIL HOURS will be held on Wednesday and Thursday evenings (6:00-7:30 P.M.) on the Grand Ballroom Balcony of the Sheraton Hotel.

## Conference Fees

Registration—	
Member AIEE or IRE:	\$12.00
Non-Member:	14.00
Wednesday Lunch:	3.50
Thursday Lunch:	3.50

Full-time students will be registered free-of-charge for all technical sessions.

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Irvine Auditorium	University Museum	Irvine Auditorium	University Museum	Irvine Auditorium	University Museum
9:00 A.M.-11:45 A.M.		9:00 A.M.-12:00 Noon		9:00 A.M.-12:00 Noon	
SESSION I Logic	SESSION II Microwave Parametric Circuits	SESSION V High-Speed Switching	SESSION VI Low Noise Amplification	SESSION IX Functional Components	SESSION X Design Applications
University Museum LUNCH: 12:00 Noon-1:15 P.M.	Irvine Auditorium FORMAL OPENING: 1:45-2:45 P.M.	University Museum LUNCH: 12:00 Noon-1:15 P.M.	University Museum LUNCH: 12:00 Noon-1:15 P.M.	University Museum LUNCH: 12:00 Noon-1:15 P.M.	University Museum LUNCH: 12:00 Noon-1:15 P.M.
Morning Sessions		Afternoon Sessions		Evening Sessions	
West Ballroom	Pennsylvania East	West Ballroom	Pennsylvania West	Pennsylvania East	Pennsylvania West
WE 1: Distributed Logic	WE 4: Magnetic Thin-Film Memories	TE 7: Nanosecond Circuity	TE 9: Thin-Film Magnetic and Superconductive Techniques in Future Computers	TE 10: Low-Level Signal Processes	TE 11: High-Power, High-Speed Switching
East Ballroom—Assembly	Independence-Constitution	East Ballroom-Assembly			
WE 2: Interconnection Problem	WE 5: Noisemanship	TE 8: Optical Masers			
Pennsylvania West	Delaware Valley				
WE 3: Microwave Power Sources	WE 6: Charge-Control Characterization of Semiconductor Devices				

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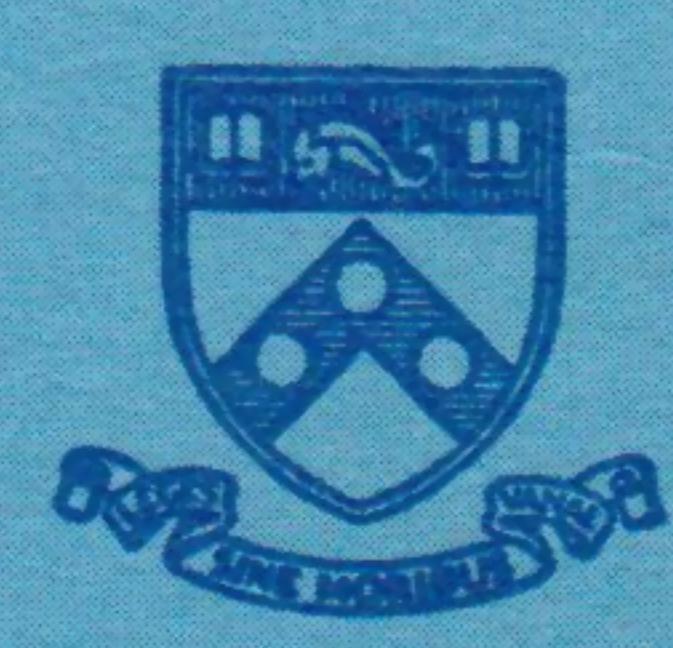
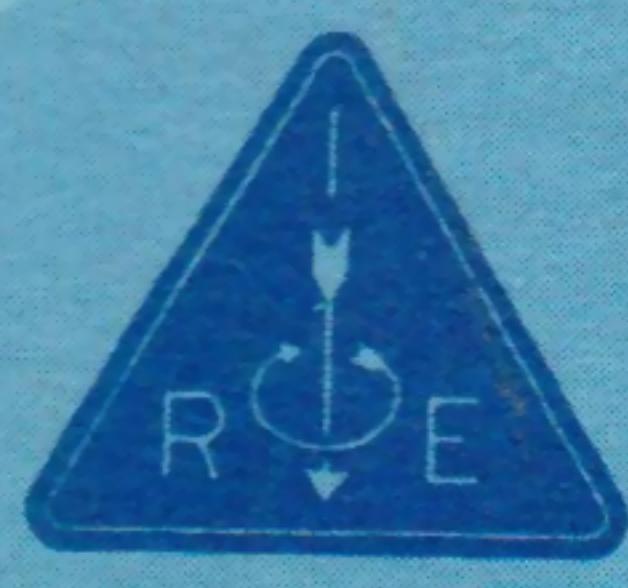
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